Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

Application Note

Part No.	AN41919A
Package Code No.	⁎QFN044-P-0606D

Semiconductor Business Group
Industrial Devices Company
Panasonic Corporation

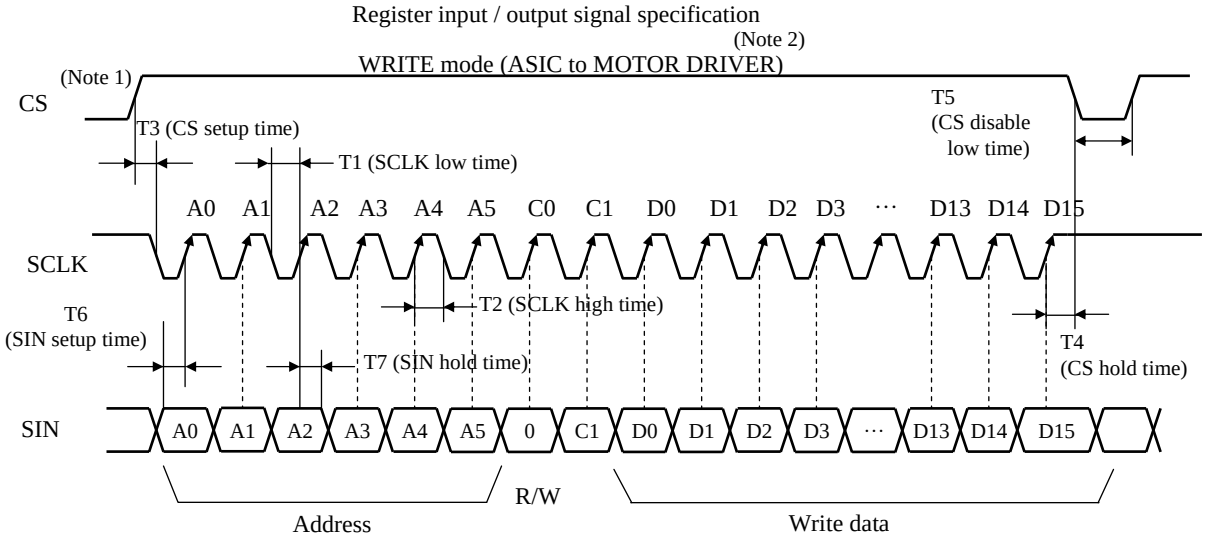
Established by	Applied by	Checked by	Prepared by
			A.Chigira

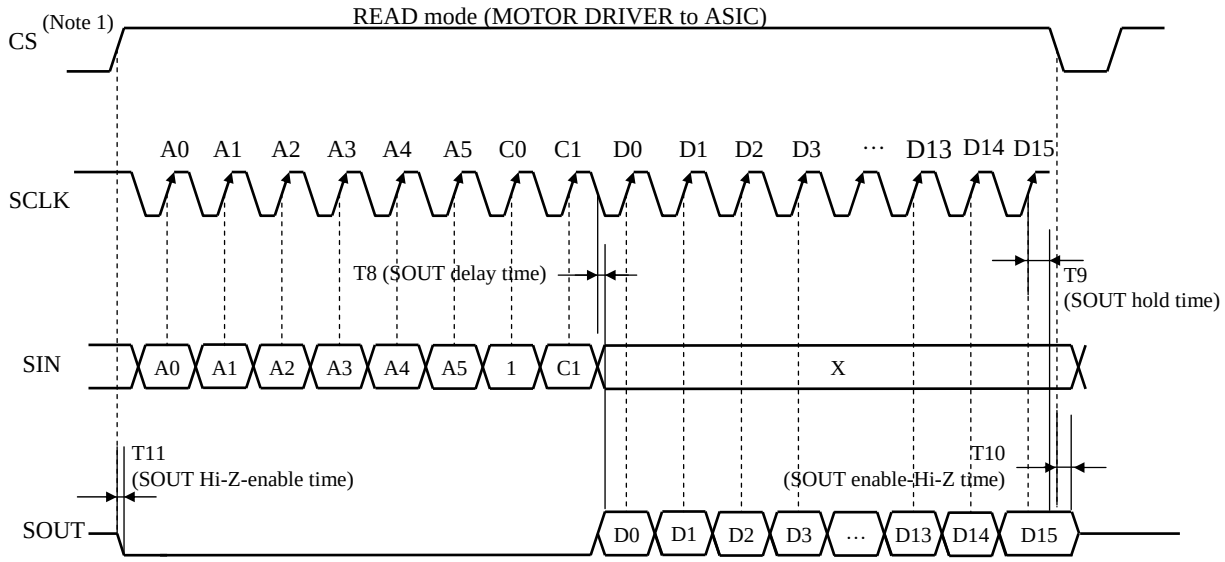
Contents

Serial Interface

■ Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.





Note 1) CS default value of each cycle (Write / Read mode) starts from Low-level.
Note 2) It is necessary to input the system clock OSCIN at write mode.

■Electrical Characteristics (Reference values for design) at VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Reference values			Unit
				Min	Typ	Max	
S1	Serial clock	Sclock	—	1	—	5	MHz
S2	SCLK low time	T1	—	100	—	—	ns
S3	SCLK high time	T2	—	100	—	—	ns
S4	CS setup time	T3	—	60	—	—	ns
S5	CS hold time	T4	—	60	—	—	ns
S6	CS disable low time	T5	—	100	—	—	ns
S7	SIN setup time	T6	—	50	—	—	ns
S8	SIN hold time	T7	—	50	—	—	ns
S9	SOUT delay time	T8	—	—	—	60	ns
S10	SOUT hold time	T9	—	60	—	—	ns
S11	SOUT enable-Hiz time	T10	—	—	—	60	ns
S12	SOUT Hiz-enable time	T11	—	—	—	60	ns
S13	SOUT Cload	Tsc	—	—	—	40	pF

■ Register List

Register list

Address	Register name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	Luminance Target	—	—	—	—	—	—	Y_TGT[9:0]									
01h	Target Update Timing	Y_PWM_POL	Y_PWM_ON	CDS_AMP_OFF	Reserved	—	—	—	—	TGT_UPDATE[7:0]							
02h	PID Filter(1)	—	—	—	TGT_FLT_OFF	TGT_LPF_FC[3:0]				—	—	DEC_AVE	AVE_SPEED[4:0]				
03h	PID(1)	PID_INV	—	—	LMT_ENB	ARW[3:0]				—	DGAIN[6:0]						
04h	PID(2)	PID_POLE[3:0]				PID_ZERO[3:0]				IRIS_ROUND[3:0]				IRIS_CALC_NR[3:0]			
05h	PID Filter(2)	—	—	—	—	PWM_FIL_OFF	PWM_LPF_FC[2:0]			AS_FLT_OFF	ASOUND_LPF_FC[2:0]			OVER_LPF_FC_2ND[1:0]		OVER_LPF_FC_1ST[1:0]	
06h	Offset DAC	—	—	—	—	—	—	—	—	DAMP_OFFSET_DAC[7:0]							
07h	Analog Adder	—	—	—	—	Y_MIX[3:0]				—	—	—	—	DAMP_MIX[3:0]			
08h	Analog LPF/Gain	Y_GAIN[3:0]				DAMP_GAIN[3:0]				—	—	Y_FLT[1:0]		—	—	DAMP_FLT[1:0]	
09h	PWM/Enable	TEST EN1	—	DT_ADJ_IRIS[1:0]		—	PWM_IRIS[2:0]			PID_CLIP[3:0]				ASWMODE[1:0]		VD_POL	ENABLE
0Ah	ADC Read	—	—	—	—	—	—	IRSAD[9:0] read only									
0Bh	Reserved	Panasonic Reserved															
0Ch	Pulse Generator	—	—	—	—	—	—	START1[9:0]									
0Dh	Pulse Generator	P1EN	—	—	—	WIDTH1[11:0]											
0Eh	Pulse Generator	—	—	—	—	—	—	START2[9:0]									
0Fh	Pulse Generator	P2EN	—	—	—	—	—	—	—	—	—	WIDTH2[5:0]					
20h	Test mode selection	TEST EN2	—	—	—	—	—	Panasonic Reserved		—	—	—	—	PLS_SEL[3:0]*			
21h	Test mode selection	—	—	—	—	—	DUTY_TEST	TGT_IN_TEST[9:0]									
22h	Reserved	Panasonic Reserved															
3Fh	Reserved	Panasonic Reserved															

— : Use prohibited

■ Register function list

Address	Register name / Bit wide	Function	Page
00h	Y_TGT[9:0]	Luminance target	15
01h	TGT_UPDATE[7:0]	Y_TGT update delay time	15
	CDS_AMP_OFF	Luminance signal amplifier enable / disable	37
	Y_PWM_ON	PWM (luminance signal modulation) buffer enable / disable	37
	Y_PWM_POL	PWM_IN polarity selection	37
02h	AVE_SPEED[3:0]	DEC_AVE time controller	16
	DEC_AVE	Moving average of Luminance target	16
	TGT_LPF_FC[3:0]	Luminance target value LPF cut-off frequency	17
	TGT_FLT_OFF	Iris target value LPF function enable / disable	17
03h	DGAIN[6:0]	PID controller digital gain	18
	ARW[3:0]	Number of bits in PID controller integrator	19
	LMT_ENB	PID controller integral stop	19
	PID_INV	PID controller polarity	19
04h	IRIS_CALC_NR[3:0]	PID controller integral error cumulative prevention level	20
	IRIS_ROUND[3:0]	PID controller differential error cumulative prevention level	20
	PID_ZERO[3:0]	PID controller zero point	21
	PID_POLE[3:0]	PID controller pole	21
05h	OVER_LPF_FC_1ST[1:0]	ADC feedback filter (1) cut-off frequency	23
	OVER_LPF_FC_2ND[1:0]	ADC feedback filter (2) cut-off frequency	23
	ASOUND_LPF_FC[2:0]	Filter cut-off frequency before PID controller	24
	AS_FLT_OFF	Filter before PID controller enable / disable	24
	PWM_LPF_FC[2:0]	LPF cut-off frequency after PID controller	25
	PWM_FLT_OFF	LPF after PID controller enable / disable	25
06h	DAMP_OFFSET_DAC[7:0]	Offset adjustment for damping coil output amplifier	34
07h	DAMP_MIX[3:0]	Damping coil signal mixed gain	34
	Y_MIX[3:0]	Luminance signal mixed gain	34
08h	DAMP_FLT[1:0]	Damping coil signal LPF cut-off frequency	35
	Y_FLT[1:0]	Luminance signal LPF cut-off frequency	35
	DAMP_GAIN[3:0]	Damping coil signal amplifier gain	35
	Y_GAIN[3:0]	Luminance signal amplifier gain	36

■ Register function list (continued)

Address	Register name / Bit wide	Function	Page
09h	ENABLE	Enable / Disable CTL	26
	VD_POL	VD_IN polarity selection	10
	ASWMODE[1:0]	ADCIN pin connection selection	39
	PID_CLIP[3:0]	PWM max-duty control	26
	PWM_IRIS[2:0]	PWM frequency of Iris block output	27
	DT_ADJ_IRIS[1:0]	Dead time correction of Iris block output	27
	TESTEN1	Test mode enable 1	—
0Ah	IRSAD[9:0]	ADC output for Iris (read only)	28
0Ch	START1[9:0]	Pulse 1 start time	29
0Dh	WIDTH1[11:0]	Pulse 1 width	29
	P1EN	Pulse 1 output enable	29
0Eh	START2[9:0]	Pulse 2 start time	30
0Fh	WIDTH2[5:0]	Pulse 2 width	30
	P2EN	Pulse 2 output enable	30
20h	PLS_SEL[3:0]*	Monitor output selection	—
	TESTEN2	Test mode enable 2	—
21h	DUTY_TEST	Iris test mode 1	40
	TGT_IN_TEST[9:0]	Iris test mode 2	40

■ Serial Interface Specifications

Data transfer starts at the rising edge of CS, and stops at the falling edge of CS.
One unit of data is 24 bits. (24 bits of the following format are called a data set in this book.)
Address and data are serially input from SIN pin in synchronization with the data clock SCK at CS = 1.
Data is retrieved at the rising edge of SCK.
Moreover, data is output from SOUT pin at data readout. (Data is output at the rising edge of SCK.)
SOUT outputs Hi-Z at CS = 0, and outputs "0" except data readout at CS = 1.
The control circuit of serial interface is reset at CS = 0.

■ Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

C0 : Register write / read selection 0 : write mode, 1 : read mode
C1 : Unused
A5 to A0 : Address of register
D15 to D0 : Data written in register

When C0 bit is "0", the write mode is selected. The address and data are retrieved from SIN in synchronization with the rising edge of data clock SCLK, and the data is stored in internal register in synchronization with the rising edge of CS.
SOUT outputs "0" in the write mode.

When the data which is 23 or less bits per 1 processing is received in the write mode, the received data becomes invalid.
The data of 25 or more bits is regarded as the continuous write mode, and the write operation is performed whenever the data of 24 bits is received. When the last data set is less than 24 bits in the continuous write mode, it becomes invalid. (The previous data set is valid.)
Even if noise occurs on SCK signal in the continuous write mode and the shifted data is received, pay attention to continue receiving or updating the shifted data.

When C0 bit is "1", the read mode is selected. The address is retrieved from SIN in synchronization with the rising edge of SCK, and then the register value of the address specified is output as LSB first from SOUT, in synchronization with the rising edge of SCK.
When C0 bit is "1", the values of D15 to D0 of SIN do not be cared.

■ Formatting

All the SIF functions containing a data register are formatted at RST = 0.

■ Register Setup Timing (continued)

Address	Register Name	Setup Timing
00h	Y_TGT[9:0]	variable
01h	TGT_UPDATE[7:0]	CS
	CDS_AMP_OFF	CS
	Y_PWM_ON	CS
	Y_PWM_POL	CS
02h	AVE_SPEED[3:0]	VD_IN
	DEC_AVE	VD_IN
	TGT_LPF_FC[3:0]	VD_IN
	TGT_FLT_OFF	VD_IN
03h	DGAIN[6:0]	VD_IN
	ARW[3:0]	VD_IN
	LMT_ENB	VD_IN
	PID_INV	VD_IN
04h	IRIS_CALC_NR[3:0]	VD_IN
	IRIS_ROUND[3:0]	VD_IN
	PID_ZERO[3:0]	VD_IN
	PID_POLE[3:0]	VD_IN
05h	OVER_LPF_FC_1ST[1:0]	VD_IN
	OVER_LPF_FC_2ND[1:0]	VD_IN
	ASOUND_LPF_FC[2:0]	VD_IN
	AS_FLT_OFF	VD_IN
	PWM_LPF_FC[2:0]	VD_IN
	PWM_FLT_OFF	VD_IN
06h	DAMP_OFFSET_DAC[7:0]	VD_IN
07h	DAMP_MIX[3:0]	CS
	Y_MIX[3:0]	CS
08h	DAMP_FLT[1:0]	CS
	Y_FLT[1:0]	CS
	DAMP_GAIN[3:0]	CS
	Y_GAIN[3:0]	CS

Address	Register Name	Setup Timing
09h	ENABLE	CS
	VD_POL	CS
	ASWMODE[1:0]	CS
	PID_CLIP[3:0]	VD_IN
	PWM_IRIS[2:0]	VD_IN
	DT_ADJ_IRIS[1:0]	VD_IN
	TESTEN1	CS
0Ah	IRSAD[9:0]	Read only
0Ch	START1[9:0]	VD_IN
0Dh	WIDTH1[11:0]	VD_IN
	P1EN	VD_IN
0Eh	START2[9:0]	VD_IN
0Fhh	WIDTH2[5:0]	VD_IN
	P2EN	VD_IN
20h	PLS_SEL[3:0]*	CS
	TESTEN2	CS
21h	DUTY_TEST	CS
	TGT_IN_TEST[9:0]	CS

VD signal internal processing

■ Specifications

In this LSI, reflection timing are based on the rising edge of VD_IN respectively. The polarities of VD_IN which are used for the internal processing can be set by the following setup.

■ Register detail description

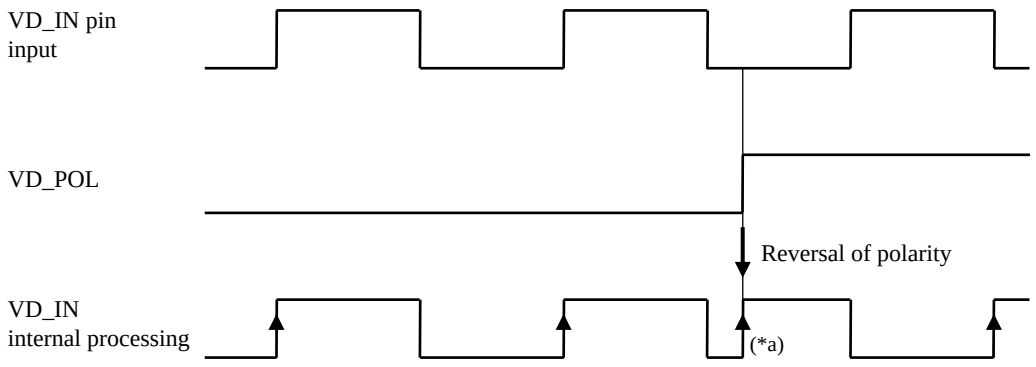
• VD_POL (VD_IN polarity selection)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														VD_POL	

VD_POL respectively set the polarities of VD_IN signals which is input to this IC.
When setting to "0", the polarity is based on the rising edge of VD_IN inputted.
When setting to "1", the polarity is based on the falling edge of VD_IN inputted.

VD_POL selects the polarity of VD_IN inputted. Therefore, depending on the selection timing of VD_POL, the timing which is not related to the edge (*a) of VD_IN which is input as the following figure may be regarded as an edge.

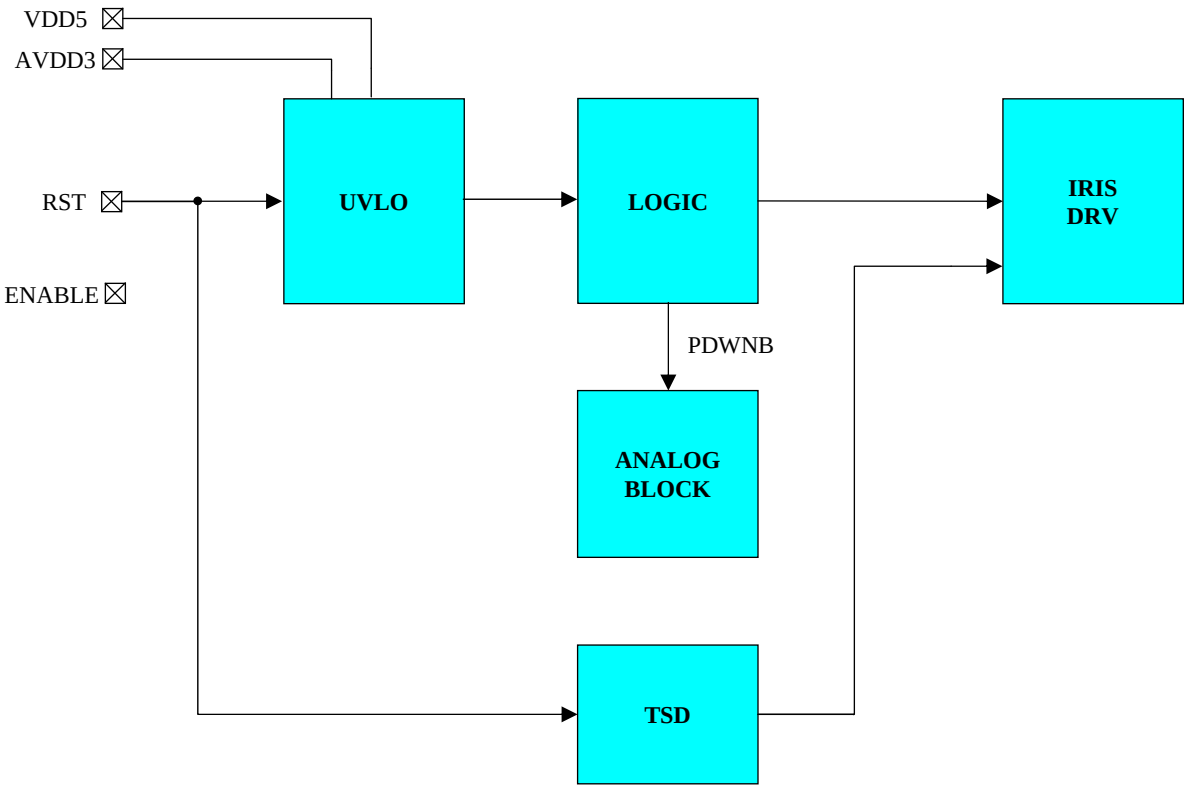
Setup value	VD polarity
0	Non-inverting
1	Inverting



Based on the rising edge of VD_IN internal processing

Reset / Protection circuit

■ Block Diagram / Specifications



Stop direction (Enable → Disable) is shown as above. The specifications are shown as follows.

	COMMON	ANALOG_BLOCK	Iris output
RST pin	Disable	Logic reset→ Disable	Logic → Output OFF
Thermal shutdown (TSD)	×	×	Output OFF
Under-voltage lock-out (UVLO)	×	Logic reset→ Disable	Logic → Output OFF

※Note 1 ×: Don't care

※Note 2 The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to V_{CC} short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

■Electrical Characteristics (Reference values for design) at VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

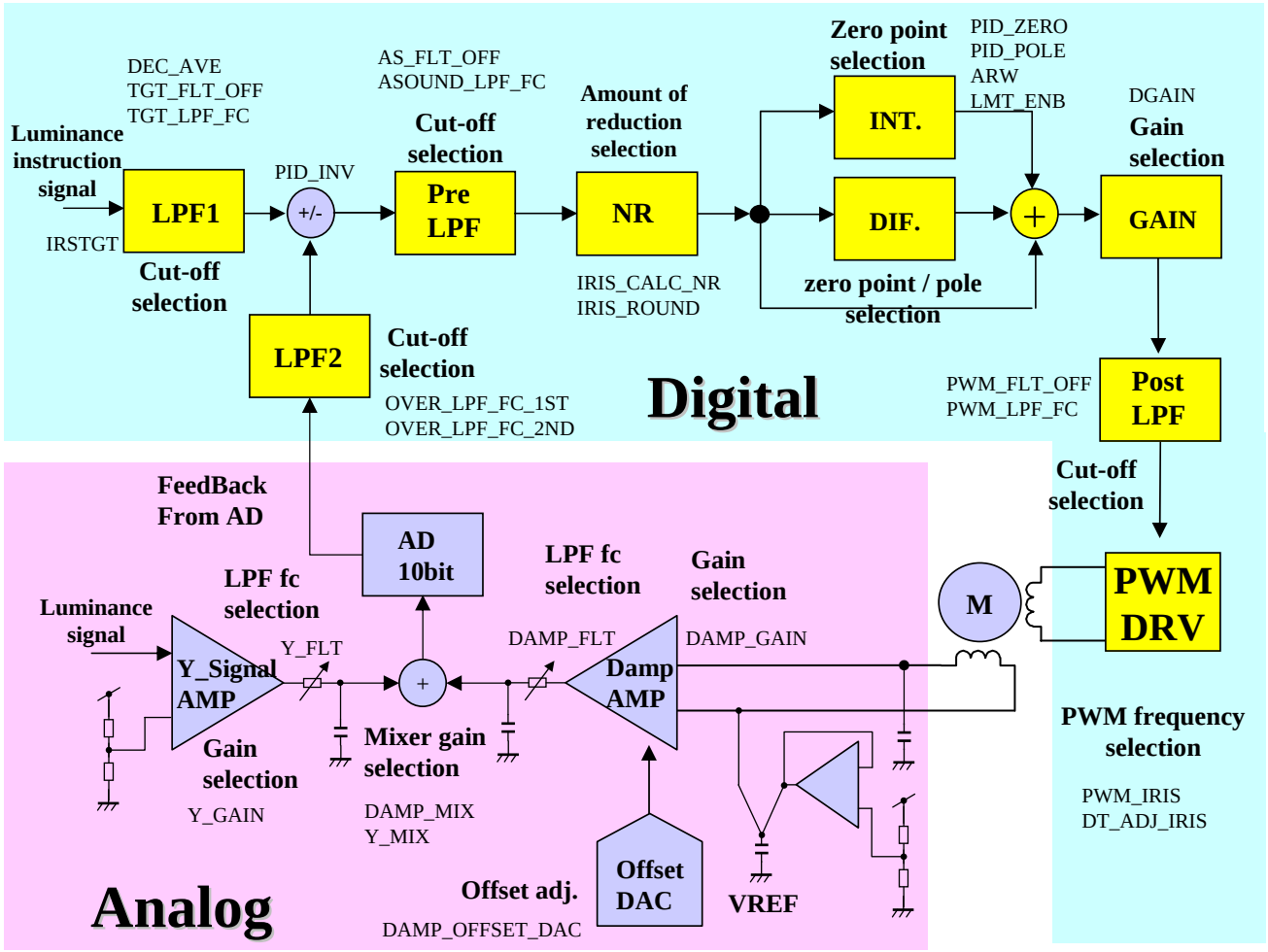
No.	Parameter	Symbol	Conditions	Reference values			Unit
				Min	Typ	Max	
Thermal shutdown							
1	Thermal shutdown circuit Operating temperature	Ttsd	—	—	150	—	°C
2	Thermal shutdown circuit Hysteresis width	DTtsd	—	—	40	—	°C
Power supply voltage monitor circuit							
3	3.3 V Reset operation	Vrston	—	—	2.27	—	V
4	3.3 V Reset hysteresis width	Vrsthys	—	—	0.2	—	V
5	VDD5 Reset operation	$V_{rstISon}$	—	—	2.2	—	V
6	VDD5 Reset hysteresis width	$V_{rstIShys}$	—	—	0.2	—	V
Digital input							
7	High-level input threshold voltage	$V_{in(H)}$	—	—	1.36	—	V
8	Low-level input threshold voltage	$V_{in(L)}$	—	—	1.02	—	V
9	Input hysteresis width	Vhysin	—	—	0.34	—	V
10	Input pull-down resistance	$R_{pullret}$	—	—	100	—	kΩ

Iris control

■ Features

- PWM drive → Low power consumption
- Each filter can be set by serial input. → Low noise drive
- Build-in damp coil signal amplifier
- Built-in 8-bit DAC for adjusting damp-coil signal offset
- Built-in luminance signal amplifier

■ Block Diagram



■Electrical Characteristics at VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.

No.	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Motor driver (Iris)							
1	H bridge ON resistance	R_{onIR}	IM = 50 mA	—	—	5	Ω
2	H bridge leak current	I_{leakIR}	—	—	—	0.8	uA
OPAMP3 (Hall Sensor Amp. for output amplification)							
3	Input voltage range	V_{IN}	AMPINN = 1.55V	1.05	—	2.05	V
4	Input offset voltage	V_{OF}	—	–15	—	15	mV
5	Output voltage (Low)	V_{OL}	ILOAD = –100 uA	—	0.2	0.4	V
6	Output voltage (High)	V_{OH}	ILOAD = 100 uA	AVDD3 – 0.4	AVDD3 – 0.2	—	V
7	Gain	V_{OG}	Gain setting value : 0h	19.7	21.9	24.1	V/V
OPAMP4 (Hall Sensor Amp. for eliminating common-mode voltage)							
8	Input offset voltage	V_{OF2}	—	–20	—	20	mV
9	Output voltage (Low)	V_{OL2}	ILOAD = –100 uA	—	0.2	0.4	V
10	Output voltage (High)	V_{OH2}	ILOAD = 100 uA	AVDD3 – 0.4	AVDD3 – 0.2	—	V
11	Gain	V_{OG2}	Gain setting value : 9h	1.75	2	2.25	V/V
Reference voltage output block							
12	Output voltage 1	VREF	ILOAD = 0 A, CVREF = 100 pF	½ AVDD3 – 0.1	½ AVDD3	½ AVDD3 + 0.1	V

■ Detail descriptions of register

- Y_TGT[9:0] (Iris desired value)

Address			00h			Initial Value			2C0h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						Y_TGT[9:0]									

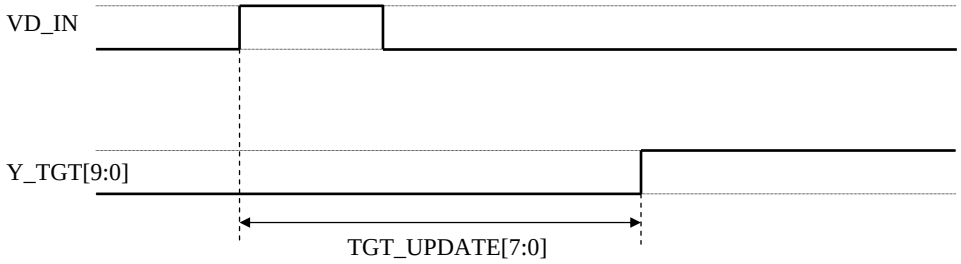
Y_TGT[9:0] sets the desired value of ADC input for using in Iris control block.

Setup value	AD input desired value
0	AVDD3 × 0/1023
1	AVDD3 × 1/1023
1023	AVDD3 × 1023/1023
n	AVDD3 × n/1023

- TGT_UPDATE[7:0]

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TGT_UPDATE[7:0]							

TGT_UPDATE[7:0] adjusts the update timing of Y_TGT[9:0].
Y_TGT[9:0] is updated after the delay time in the below table from rising edge of VD_IN.



Setting Value	Update delay
0	0
1	80 µs
n	n × (270/3.375) µs
255	20.4 ms

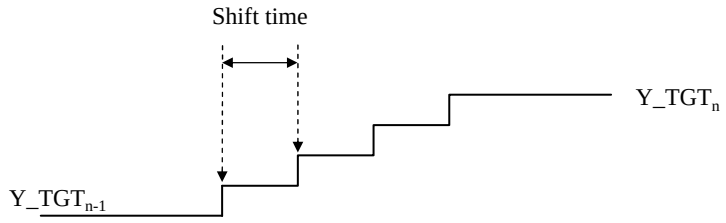
■ Detail descriptions of register (continued)

• AVE_SPEED[4:0]

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											AVE_SPEED[4:0]				

AVE_SPEED[4:0] sets the moving average shift time for iris target.

Setup value	Moving ave. shift time
0	2 µs
1	152 µs
n	(n × 512+1)/3.375 µs
31	4.703 ms



• DEC_AVE(Moving average of iris target)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										DEC_AVE					

Moving average of target value for Iris is set.

Setup value	Moving average
0	8
1	4

■ Detail descriptions of register (continued)

• TGT_LPF_FC[3:0]

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				TGT_LPF_FC[3:0]											

Cut-off frequency of input filter of instruction value for Iris is set.

Setup value	Cut-off frequency
0	325 Hz
1	650 Hz
2	1 300 Hz
3	2 600 Hz
4	40 Hz
5	50 Hz
6	63 Hz

Setup value	Cut-off frequency
7	80 Hz
8	100 Hz
9	125 Hz
10	160 Hz
11	200 Hz
12	250 Hz
—	—

• TGT_FLT_OFF

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			TGT_FLT_OFF												

Whether filtering-function of instruction value for Iris is enabled or disabled is set.
When the function is enabled, LPF is inserted to between instruction value input and deviation calculator.

Setup value	Iris target filter
0	Enable
1	Disable

■ Detail descriptions of register (continued)

• DGAIN[6:0] (PID controller digital gain)

Address			03h			Initial Value			10h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									DGAIN[6:0]						

Digital gain of PID controller is set. The setup gain is defined as the gain between AD input at 35 Hz and motor input under the conditions of PID zero point = 35 Hz, pole = 900 Hz, PWM frequency = 31.25 kHz.
Refer to the details of setup value.

Setup value	Gain
00h	0
01h ~ 7Fh	{ 0.125 × { 2^(MSB 3 bit – 3'd3)} × [16 + LSB 4 bit] } + 3 dB

Register bit epexegesis (Gain table)

DGAIN[3:0]+16	DGAIN[6:4]															
	000		001		010		011		100		101		110		111	
	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB
16	0	-	0.5	– 3.0	1	3.0	2	9.0	4	15.0	8	21.1	16	27.1	32	33.1
17	0.265625	– 8.5	0.53125	– 2.5	1.0625	3.5	2.125	9.5	4.25	15.6	8.5	21.6	17	27.6	34	33.6
18	0.28125	– 8.0	0.5625	– 2.0	1.125	4.0	2.25	10.0	4.5	16.1	9	22.1	18	28.1	36	34.1
19	0.296875	– 7.5	0.59375	– 1.5	1.1875	4.5	2.375	10.5	4.75	16.5	9.5	22.6	19	28.6	38	34.6
20	0.3125	– 7.1	0.625	– 1.1	1.25	4.9	2.5	11.0	5	17.0	10	23.0	20	29.0	40	35.0
21	0.328125	– 6.7	0.65625	– 0.7	1.3125	5.4	2.625	11.4	5.25	17.4	10.5	23.4	21	29.4	42	35.5
22	0.34375	– 6.3	0.6875	– 0.3	1.375	5.8	2.75	11.8	5.5	17.8	11	23.8	22	29.8	44	35.9
23	0.359375	– 5.9	0.71875	0.1	1.4375	6.2	2.875	12.2	5.75	18.2	11.5	24.2	23	30.2	46	36.3
24	0.375	– 5.5	0.75	0.5	1.5	6.5	3	12.5	6	18.6	12	24.6	24	30.6	48	36.6
25	0.390625	– 5.2	0.78125	0.9	1.5625	6.9	3.125	12.9	6.25	18.9	12.5	24.9	25	31.0	50	37.0
26	0.40625	– 4.8	0.8125	1.2	1.625	7.2	3.25	13.2	6.5	19.3	13	25.3	26	31.3	52	37.3
27	0.421875	– 4.5	0.84375	1.5	1.6875	7.5	3.375	13.6	6.75	19.6	13.5	25.6	27	31.6	54	37.6
28	0.4375	– 4.2	0.875	1.8	1.75	7.9	3.5	13.9	7	19.9	14	25.9	28	31.9	56	38.0
29	0.453125	– 3.9	0.90625	2.1	1.8125	8.2	3.625	14.2	7.25	20.2	14.5	26.2	29	32.2	58	38.3
30	0.46875	– 3.6	0.9375	2.4	1.875	8.5	3.75	14.5	7.5	20.5	15	26.5	30	32.5	60	38.6
31	0.484375	– 3.3	0.96875	2.7	1.9375	8.7	3.875	14.8	7.75	20.8	15.5	26.8	31	32.8	62	38.8

■ Detail descriptions of register (continued)

• ARW[3:0]

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				ARW[3:0]											

Number of bits in PID integrator is set. It affects the recovery time from saturation in the PID integrator.

Setup value	Number of bits in integrator
0 to 3	12-bit
4 to 14	(15 – setup value)-bit
15	1-bit

• LMT_ENB

Address			03h			Initial Value			1						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			LMT_ENB												

Integral stop function in PID output is enabled / disabled. It affects the recovery time from saturation in the PID output.

Setup value	Integral stop function
0	Disable
1	Enable

• PID_INV

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PID_INV															

PID control polarity is inverted.

Setup value	PID control polarity
0	Non-inverting
1	Inverting

■ Detail descriptions of register (continued)

• IRIS_CALC_NR[3:0] (PID controller integral error cumulative prevention level)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												IRIS_CALC_NR[3:0]			

Error accumulation prevention level of PID controller integrator is set. When the function is enabled, error accumulation generated by integration in the PID controller can be decreased. However, the integral function may fall.

Setup value	Error accumulation prevention level
0	Disable
1 to 14	$\pm 1/2^{(15-n)}$ LSB
15	$\pm$1 LSB

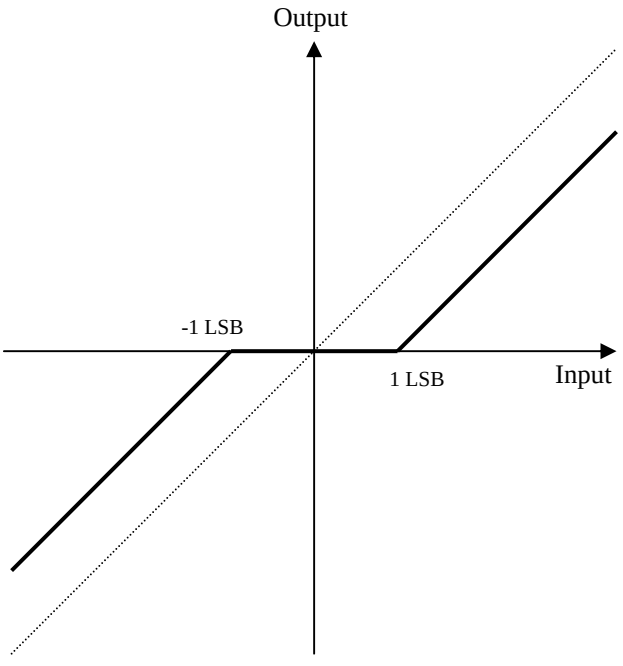
• IRIS_ROUND[3:0] (PID controller differential error cumulative prevention level)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								IRIS_ROUND[3:0]							

Noise respondence prevention level of PID controller differentiator is set. When the function is enabled, the amplitude of noise generated by differentiation in the PID controller can be decreased. However, the differential function may fall.

Setup value	Error accumulation prevention level
0	Disable
1 to 14	$\pm 1/2^{(15-n)}$ LSB
15	$\pm$1 LSB

Figure on right shows the basic concept of above function.
When maximum value is set, input signal smaller than $\pm$1 LSB is ignored.



■ Detail descriptions of register (continued)

• PID_ZERO[3:0] (PID controller zero point)

Address			04h			Initial Value			8h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				PID_ZERO[3:0]											

Zero point of PID controller is set.

• PID_POLE[3:0] (PID controller pole)

Address			04h			Initial Value			Fh						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PID_POLE[3:0]															

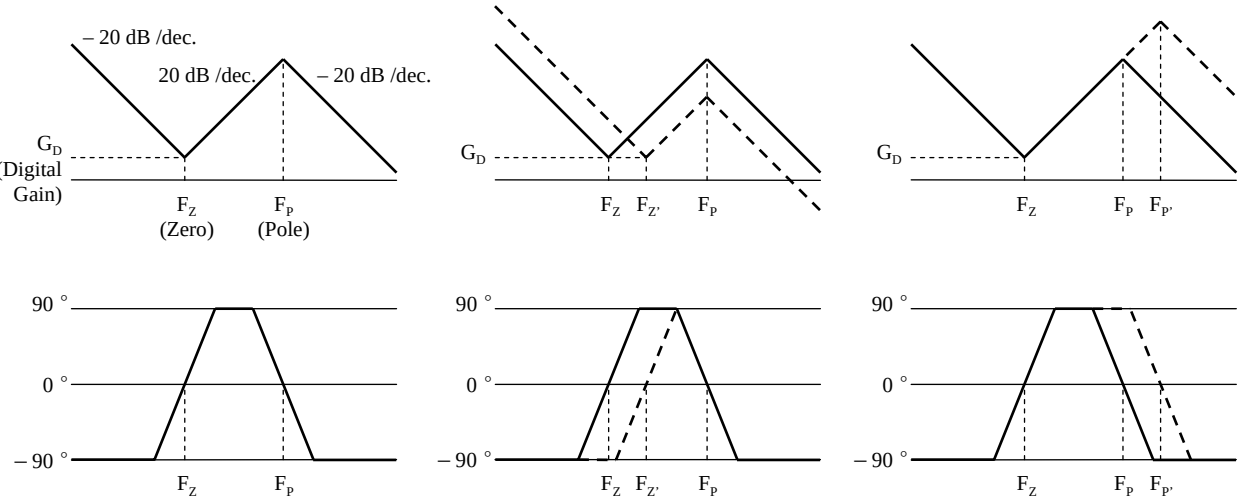
Pole of PID controller is set.

Setup value	Zero point
0	10 Hz / 10 Hz
1	15 Hz / 15 Hz
2	20 Hz / 20 Hz
3	25 Hz / 25 Hz
4	30 Hz / 30 Hz
5	35 Hz / 30 Hz
6	35 Hz / 35 Hz
7	40 Hz / 35 Hz
8	40 Hz / 40 Hz
9	45 Hz / 45 Hz
10	50 Hz / 50 Hz
11	55 Hz / 55 Hz
12	60 Hz / 60 Hz
13	65 Hz / 65 Hz
14	70 Hz / 70 Hz
15	75 Hz / 75 Hz

Setup value	Pole
0	710 Hz
1	790 Hz
2	870 Hz
3	950 Hz
4	1 040 Hz
5	1 120 Hz
6	1 200 Hz
7	1 280 Hz
8	1 370 Hz
9	1 450 Hz
10	1 530 Hz
11	1 620 Hz
12	1 700 Hz
13	1 790 Hz
14	1 870 Hz
15	1 960 Hz

■ Detail descriptions of register (continued)

The characteristic of PID controller, and the effect of changing PID_ZERO[3:0] and PID_POLE[3:0] is shown below (Bode diagram).



Bode diagram of PID controller

Changing zero from F_Z to $F_{Z'}$

Changing pole from F_P to $F_{P'}$

G_D: DGAIN[6:0]
F_Z: PID_ZERO[3:0]
F_P: PID_POLE[3:0]

■ Detail descriptions of register (continued)

• OVER_LPF_FC_1ST[1:0] (ADC feedback filter (1) cut-off frequency)

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														OVER_LPF_FC_1ST[1:0]	

LPF(1) cut-off frequency in AD feedback block is set.

Setup value	Cut-off frequency
0	2 600 Hz
1	3 600 Hz
2	5 200 Hz
3	8 000 Hz

• OVER_LPF_FC_2ND[1:0] (ADC feedback filter (2) cut-off frequency)

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											OVER_LPF_FC_2ND[1:0]				

LPF(2) cut-off frequency in AD feedback block is set.

Setup value	Cut-off frequency
0	2 600 Hz
1	3 600 Hz
2	5 200 Hz
3	8 000 Hz

■ Detail descriptions of register (continued)

• ASOUND_LPF_FC[2:0] (Filter cut-off frequency before PID controller)

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									ASOUND_LPF_FC[2:0]						

Filter cut-off frequency before PID controller is set.

Setup value	Cut-off frequency
0	900 Hz
1	1 300 Hz
2	1 600 Hz
3	2 000 Hz
4	2 600 Hz
5	3 200 Hz
6	4 000 Hz
7	Prohibition

• AS_FLT_OFF (Filter before PID controller enable / disable)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								AS_FLT_OFF							

Whether filtering-function before PID controller is enabled or disabled is set.
When the function is enabled, LPF is inserted to the controller.

Setup value	Filter before PID
0	Enable
1	Disable

■ Detail descriptions of register (continued)

• PWM_LPF_FC[2:0]

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					PWM_LPF_FC[2:0]										

Cut-off frequency after PID controller is set.

Setup value	Cut-off frequency (Hz)
0	900
1	1 300
2	1 600
3	2 000
4	2 600
5	3 200
6	4 000
7	Prohibition

• PWM_FLT_OFF

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			PWM_FLT_OFF												

Whether filtering function after PID controller is enabled or disabled is set. When the function is enabled, LPF is inserted to the controller.

Setup value	Filter after PID
0	Enable
1	Disable

■ Detail descriptions of register (continued)

•ENABLE

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															ENABLE

ENABLE sets disable / enable of iris control circuit.

Setup Vale	Iris control
0	Disable
1	Enable

• PID_CLIP[3:0]

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PID_CLIP[3:0]							

PID_CLIP[3:0] sets maximum duty of iris PWM driver.

Setup value	Maximum duty
0	100%
1	93.75%
n	(100－n×6.25)%
15	6.25%

■ Detail descriptions of register (continued)

• PWM_IRIS[2:0]

Address			09h			Initial Value			4						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					PWM_IRIS[2:0]										

PWM frequency of Iris block is set.

Setup value	PWM frequency (kHz)
0	26
1	31.25
2	62.5
3	93.75
4	125
5	150
6	187.5
7	210

• DT_ADJ_IRIS[1:0]

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		DT_ADJ_IRIS[1:0]													

Dead time correction amount of Iris block is set.

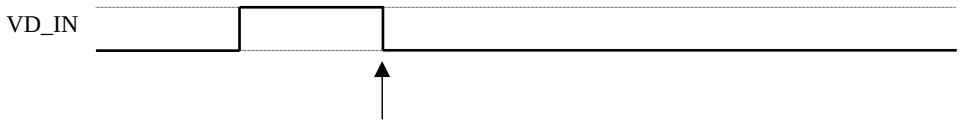
Setup value	Dead time correction amount
0	Standard correction
1	Standard correction – 1
2	Standard correction – 2
3	No correction

■ Detail descriptions of register (continued)

• IRSAD[9:0] read only

Address			0Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						IRSAD[9:0]									

IRSAD[9:0] is a read-only register to retrieve iris ADC output.
Access this register only when VD_IN is low.



Iris ADC output: data is fixed at the falling edge of VD_IN.

■ Detail descriptions of register (continued)

• START1[9:0] (Pulse 1 start position)

Address			0Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						START1[9:0]									

• WIDTH1[11:0] (Pulse 1 width)

Address			0Dh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				WIDTH1[11:0]											

• P1EN (Pulse 1 output)

Address			0Dh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
P1EN															

Refer to the next page for the details of function.

■ Detail descriptions of register (continued)

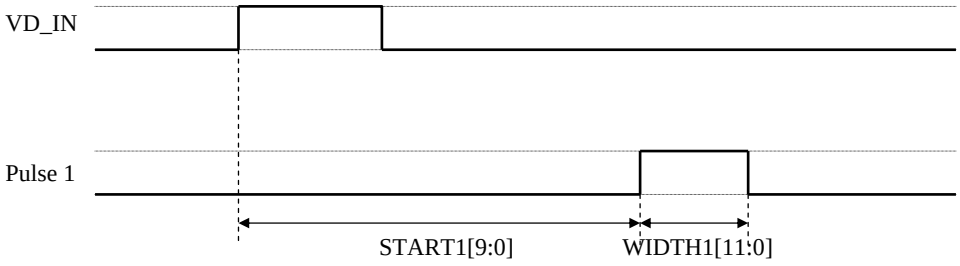
START1[9:0] , WIDTH1[11:0], and P1EN set the pulse output (pulse 1) for strobe.

START1[9:0] sets the start time of pulse 1. The count of start time starts from the rising edge of video sync signal (VD_IN), and continues until the setup time.

WIDTH1[11:0] sets the width of pulse 1. The count of pulse width starts in synchronization with the end of count of start time, and continues until the setup time.

P1EN controls the output of pulse 1.

When any of START1[9:0], WIDTH1[11:0], and P1EN is "0", pulse 1 is not output.



START1	Start time
0	0
1	20.1 µs
n	n × (68/3.375) µs
1023	20.56 ms

WIDTH1	Pulse width
0	0
1	1.19 µs
n	n × (4/3.375) µs
4095	4.87 ms

■ Detail descriptions of register (continued)

• START2[9:0] (Pulse 2 start position)

Address			0Eh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						START2[9:0]									

• WIDTH2[5:0] (Pulse 2 width)

Address			0Fh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										WIDTH2[5:0]					

• P2EN (Pulse 2 output)

Address			0Fh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
P2EN															

Refer to the next page for the details of functions.

■ Detail descriptions of register (continued)

START2[9:0], WIDTH2[5:0], and P2EN set the pulse output (pulse 2) for Iris full-close.

START2[9:0] sets the start time of pulse 2. The count of start time starts from the rising edge of video sync signal (VD_IN), and continues until the setup time.

WIDTH2[5:0] sets the width of pulse 2. The setup is performed at the number of times of rising after the end of count of start time. After the specified number of times of rising edge of VD_IN is counted, the output of pulse 2 ends at the falling edge of VD_IN.

P2EN controls the output of pulse 2.

When any of START2[9:0], WIDTH2[5:0], and P2EN is "0", pulse 2 is output.
Moreover, the setup value is not updated under the count of START2 or WIDTH2.

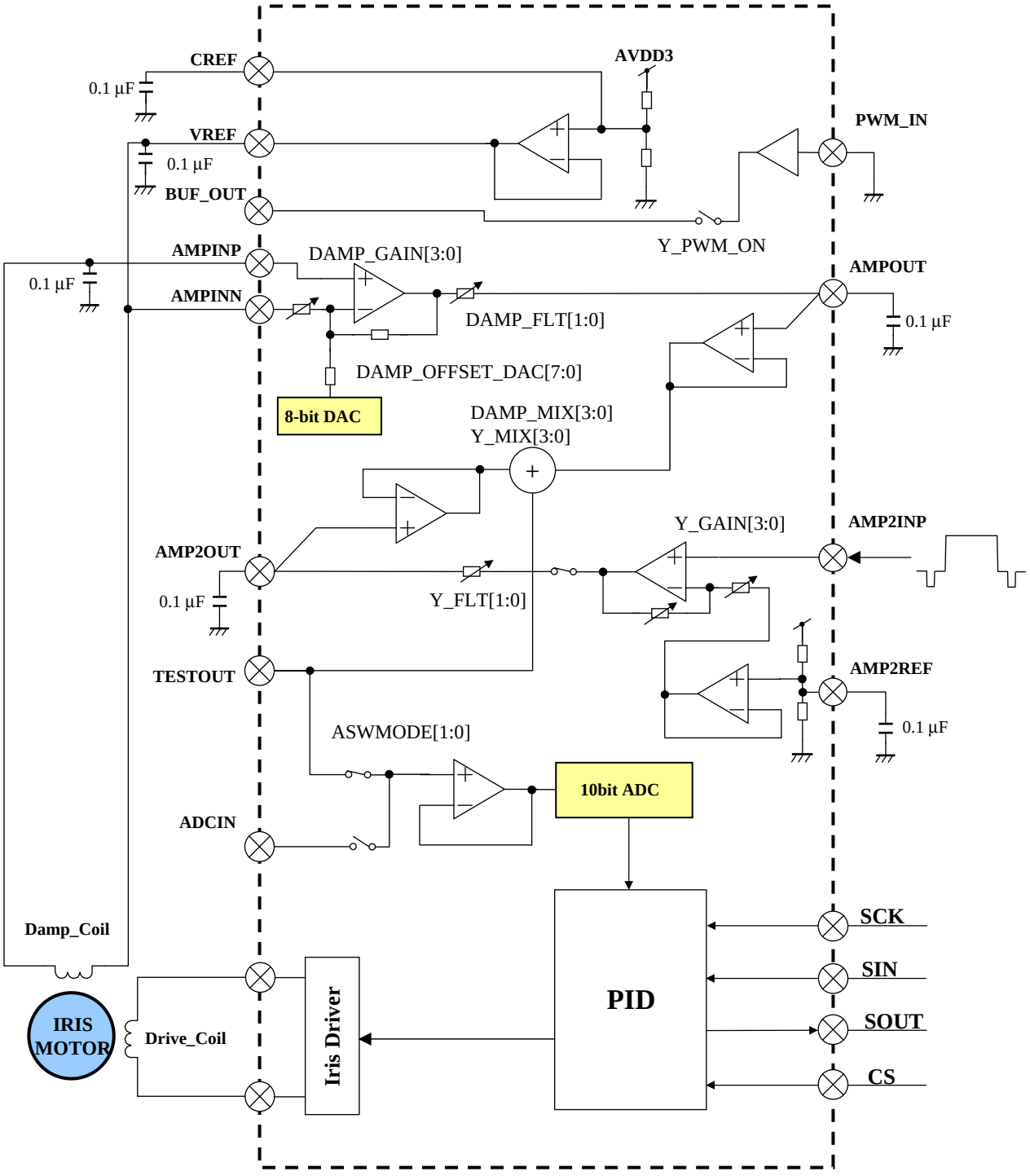
※The above pulse width is under the condition of WIDTH2[5:0]＝4

START2	Start time
0	0
1	20.1 µs
n	n × (68/3.375) µs
1023	20.56 ms

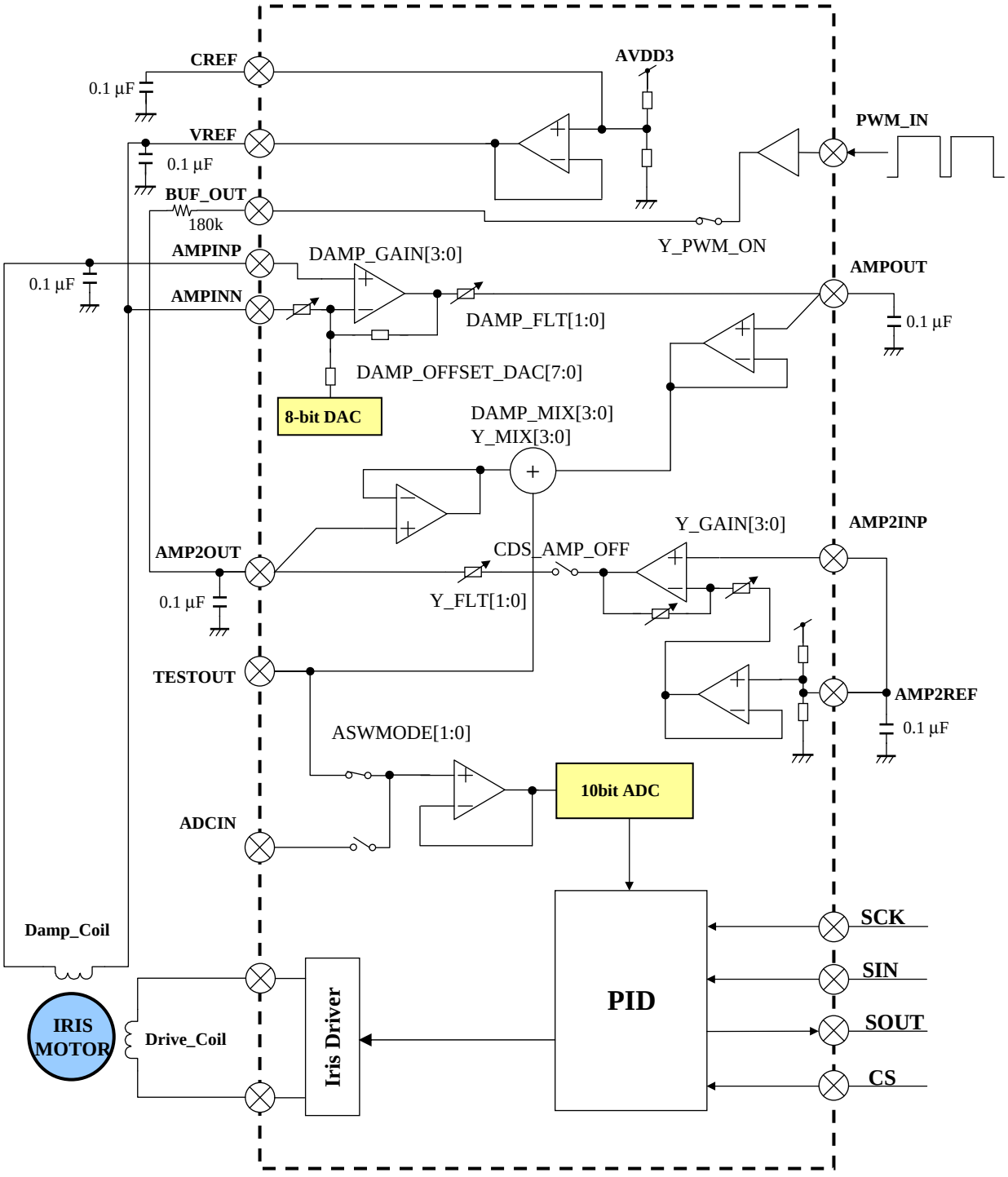
WIDTH2	Pulse width
0	0
1	VD_IN 1 count
63	VD_IN 63 count
n	VD_IN n count

Iris Control Analog Part

■ Block Diagram (Analog Luminance Signal Application)



■ Block Diagram (PWM Luminance Signal Application)



■ Detail descriptions of register

• DAMP_OFFSET_DAC[7:0]

Address			06h			Initial Value		80h							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DAMP_OFFSET_DAC[7:0]							

Offset value for Damp-Coil Amp. is set.

Setup value	Amount of offset
0 to 255	AVDD3 / 256 × (Setup value – 128)

•DAMP_MIX[3:0]
•Y_MIX[3:0]

Address			07h			Initial Value			7h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												DAMP_MIX[3:0]			

Address			07h			Initial Value			3h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				Y_MIX[3:0]											

Gain of damp-coil signal mixing ratio and luminance signal mixing ratio. is set.

Setup value	GAIN (dB)	Setup value	GAIN (dB)
0	-12.0	8	7.0
1	-6.0	9	8.0
2	-2.5	10	8.8
3	0.0	11	9.5
4	1.9	12	10.2
5	3.5	13	10.9
6	4.9	14	11.5
7	6.0	15	12.0

■ Detail descriptions of register

- DAMP_FLT[1:0]
- Y_FLT[1:0]

Address			08h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										Y_FIL[1:0]				DAMP_FIL [1:0]	

LPF register value is set.

Setup value	R_LPF(ohms)
0	200k
1	100k
2	66.6k
3	50k

- DAMP_GAIN[3:0]

Address			08h			Initial Value			9h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				DAMP_GAIN[3:0]											

Gain of damp-coil output Amp. is set.

Setup value	Gain(V/V)	Setup value	Gain(V/V)
0	21.9	8	58.0
1	26.4	9	62.6
2	31.0	10	67.1
3	35.5	11	71.7
4	40.1	12	76.3
5	44.6	13	80.8
6	49.2	14	85.4
7	53.7	15	89.9

■ Detail descriptions of register

•Y_GAIN[3:0]

Address			08h			Initial Value			9h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Y_GAIN[3:0]															

Gain of luminance output Amp. is set.

Setup value	Gain (V/V)	Setup value	Gain (V/V)	Setup value	Gain (V/V)
0	1.025	4	1.125	8	1.5
1	1.05	5	1.25	9	2
2	1.075	6	1.375	10	2.5
3	1.1	7	1.5	11	3

■ Detail descriptions of register

•CDS_AMP_OFF

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	CDS_AMP_OFF														

CDS_AMP_OFF sets disable / enable of luminance amplifier.

Setup Vale	Mode
0	Enable
1	Disable

•Y_PWM_ON

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Y_PWM_ON															

Y_PWM_ON sets disable / enable of luminance PWM signal buffer.

Setup Vale	Mode
0	Disable
1	Enable

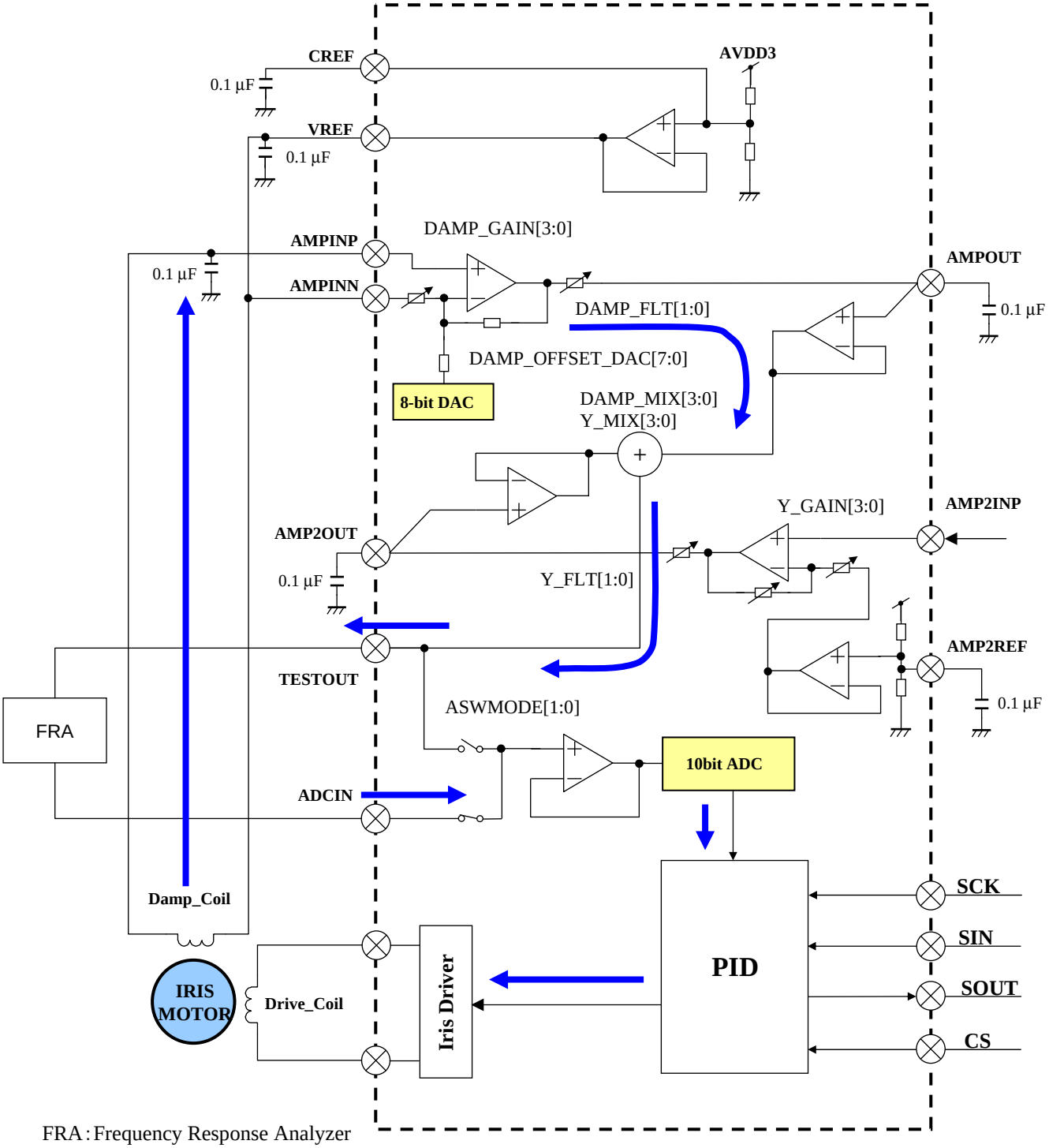
•Y_PWM_POL

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Y_PWM_POL															

Luminance PWM signal polarity is inverted.

Setup value	Polarity
0	Non-inverting
1	Inverting

■ Method for measuring open loop frequency response



FRA : Frequency Response Analyzer

1) Set ASWMODE[1:0]=2.
2) Connect FRA (frequency response analyzer) between TESTOUT and ADCIN.
3) Set parameters for PID controller.
4) Open loop frequency from ADCIN to TESTOUT can be measured.

■ Detail descriptions of register (continued)

• ASWMODE[1:0]

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												ASWMODE[1:0]			

ASWMODE[1:0] sets test mode for iris ADC.

Setup value	Iris ADC mode
0	Normal mode
1	Normal mode
2	Iris test mode
3	—

By setting ASWMODE[1:0]=2, open loop frequency response of iris can be measured.
Refer to page xx for detail.

■ Detail descriptions of register (continued)

• TGT_IN_TEST[9:0]

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						TGT_IN_TEST[9:0]									

Drive duty of Iris output block can be directly controlled. DUTY_TEST should be set to "1" in order to enable this function.
TGT_IN_TEST[9] sets the rotation direction of Iris output block. TGT_IN_TEST[8:0] sets the drive duty of Iris output block.

• Method for calculating drive duty

Drive duty depends on the setup value of PWM_IRIS[2:0].
a is calculated by a = { TGT_IN_TEST[8:1], 2'b00, TGT_IN_TEST[0] } (binary 10-bit).
b corresponding to PWM_IRIS[2:0] is selected from the following table.
The drive duty is given by calculating a/b. When a/b > 1, the drive duty is 100%.
Example) When TGT_IN_TEST[8:0] = 80h, PWM_IRIS[2:0] = 2,
a = { 40h, 2'b00, 1'b0 } = 200h
a/b = 200h / 862 = 0.59

TGT_IN_TEST[9]	Drive direction
0	Current direction DRV_OUT2 → DRV_OUT1
1	Current direction DRV_OUT1 → DRV_OUT2

TGT_IN_TEST[8:0]	Drive duty
000h	0%
1FFh	100%
n	a/b

PWM_IRIS[2:0]	b
0	2 046
1	1 726
2	862
3	574
4	430
5	350
6	286
7	254

• DUTY_TEST

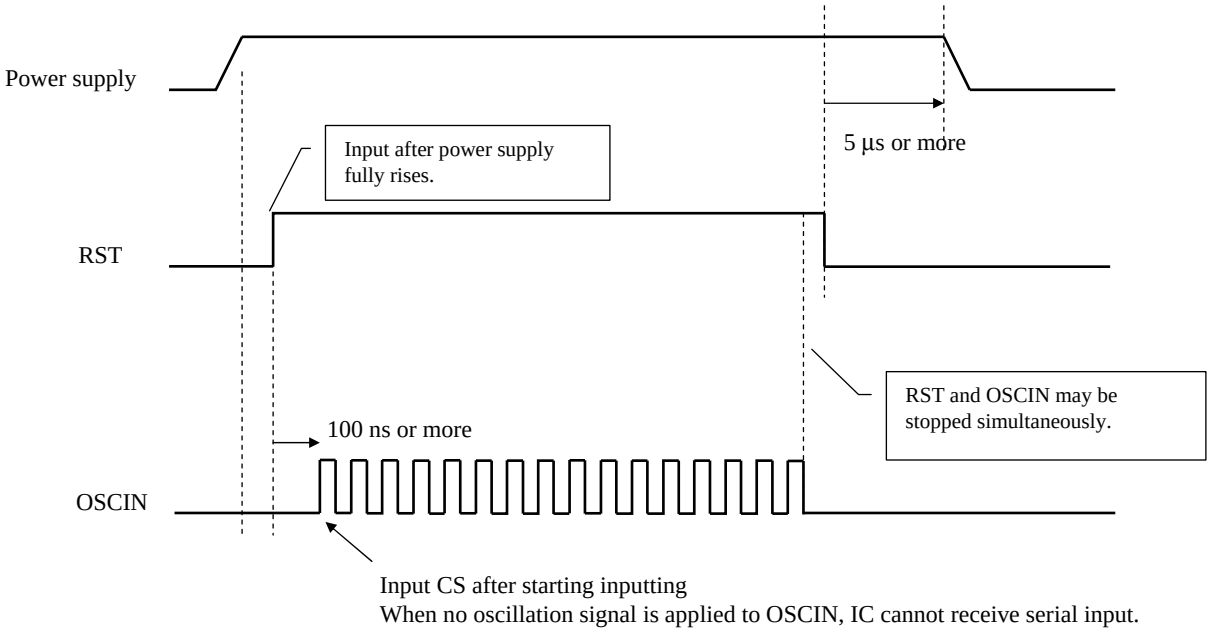
Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				DUTY_TEST											

Whether duty direct control function in Iris output block is enabled or disabled is set.

Setup value	Function
0	Disable (Normal operation)
1	Enable

1. Start / Stop sequence

The Start / Stop sequence of power supply, RST, ENABLE, and OSCIN is shown as follows.



2. Input capacitance of input pin

Input capacitance of input pin is 10 pF or less.

3. Timing of OSCIN and VD signal

Since the processing which VD signal (VD_IN input) is synchronized with OSCIN is performed in this IC, OSCIN and VD signal do not have restrictions of input timing.

4. Connections to VREF and CREF

To VREF (Pin 2), do not connect other than recommended capacitor and damp coil.
To CREF (Pin 3), do not connect other than recommended capacitor.

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