

## **Notification about the transfer of the semiconductor business**

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

※ Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

**Nuvoton Technology Corporation Japan**

# □ MN103SE5 Series

Type	MN103SFE5P
Internal ROM type	FLASH
ROM (byte)	624K
RAM (byte)	32K
Package (Lead-free)	LQFP048-P2-0707A
Minimum Instruction Execution Time	20.9 ns (at 3.0 V to 3.6 V, 48 MHz)

## ■ Interrupts

RESET. IRQ × 3. Timer × 12. I<sup>2</sup>C × 7. SIF × 8. DMA × 12. Stream DMA × 1. WDT. System error. USB × 2. I2S × 1

## ■ Timer Counter

8-bit timer × 6

Reload-down count. Cascade connection possible (usable as a 16-bit to 32-bit timer)

16-bit timer × 2

Up-down count. Input capture. PWM output. Compare/capture register 2 channels

Watchdog timer × 1

## ■ Serial interface

Multi-master I<sup>2</sup>C × 2

UART/Synchronous interface selective × 4

## ■ Audio Output Interface

I2S interface × 1

## ■ DMA controller

Number of channels: 4 channels

Unit of transfer: 8/16/32 bits

Maximum transfer cycles: 65535

Starting factor: External interrupt. Timer. Serial transmission/reception. I<sup>2</sup>C transmission/reception. Software. USB transmission/reception end. I2S empty

Transfer method: 2-bus cycle transfer

Addressing modes: Fixed. Increment. Decrement

Transfer mode: Word transfer. Burst transfer. Intermittent transfer

## ■ Stream DMA controller

Number of channels: 1 channels

Unit of transfer: 8/32 bits

Maximum transfer cycles: 65535

Transfer source: Interface RAM

Transfer destination: Serial I/F. Audio output interface

## ■ USB HOST Controller

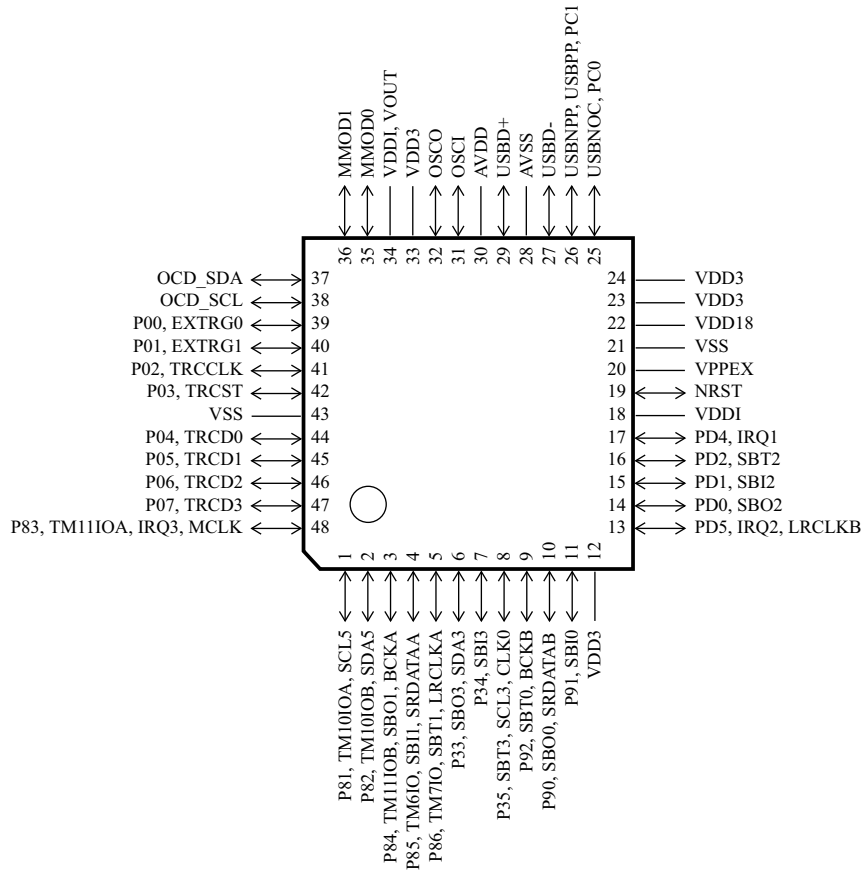
Conforms to USB 2.0: Full-speed (12 Mbps) supported

OHCI R1.0a standard conforming. External power supply control function. USB transceiver built-in

## ■ I/O Pins

I/O 27 : (3 V I/O) Common use

■ Pin Assignment  
LQFP048-P2-0707A



## Request for your special attention and precautions in using the technical information and semiconductors described in this book

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