

## **Notification about the transfer of the semiconductor business**

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

※ Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

**Nuvoton Technology Corporation Japan**



# FC4B22070L

## Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

### ■ Features

- Low source-source ON resistance:  $R_{ss(on)}$  typ. = 17.5 m $\Omega$  (VGS = 4.5 V)
- CSP package: smallest & thinnest size
- RoHS compliant (EU RoHS / MSL: Level 1 compliant)

### ■ Marking Symbol: 14

### ■ Packaging

Embossed type (Thermo-compression sealing) : 8 000 pcs / reel (standard)

### ■ Absolute Maximum Ratings Ta = 25 °C

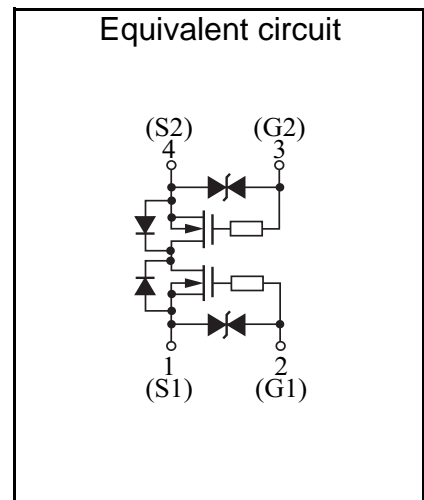
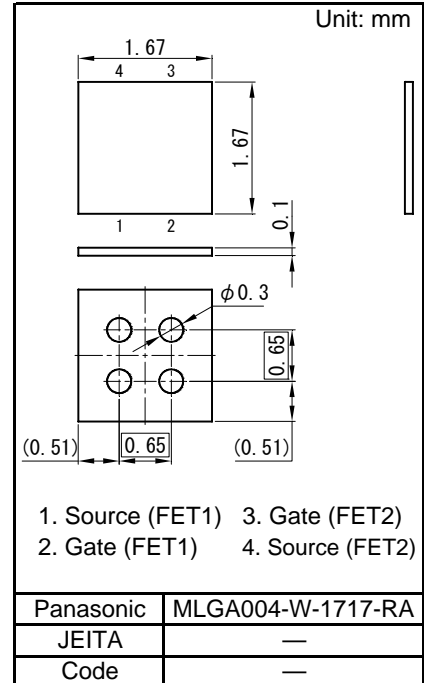
Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	24	V
Gate-source Voltage	VGS	$\pm 12$	V
Source Current	DC <sup>*1</sup>	IS1	3.5
	DC <sup>*2</sup>	IS2	6
	Pulse <sup>*2,*3</sup>	Isp	60
Total Power Dissipation	DC <sup>*1</sup>	PD1	0.4
	DC <sup>*2</sup>	PD2	1.5
Channel Temperature	Tch	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Thermal Resistance	Channel to Case <sup>*1</sup>	Rth(ch-a)1	312
	Channel to Case <sup>*2</sup>	Rth(ch-a)2	83

Note \*1 Mounted on FR4 board ( 25.4 mm × 25.4 mm × t1.0 mm )

using the minimum recommended pad size (36 $\mu$ m Copper ).

\*2 Mounted on Ceramic substrate (70 mm × 70 mm × t1.0 mm).

\*3 t = 10  $\mu$ s, Duty Cycle  $\leq$  1 %



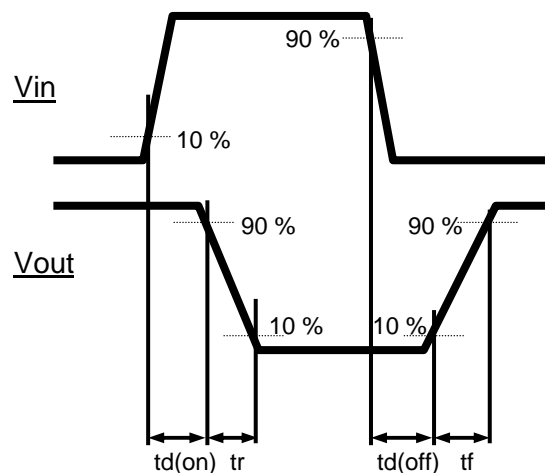
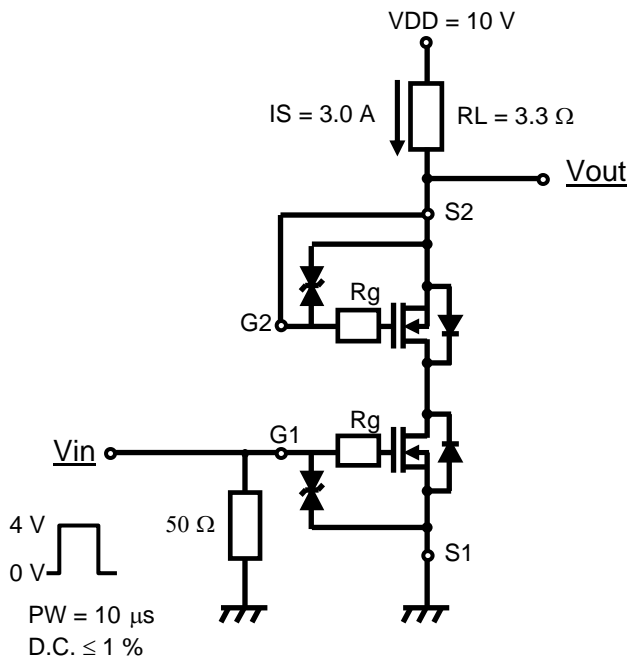
■ Electrical Characteristics Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	24			V
Zero Gate Voltage Source Current	ISSS	VSS = 24 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	IS = 1.0 mA, VSS = 10 V	0.4	0.9	1.4	V
Source-source On-state Resistance	RSS(on)1	IS = 3.0 A, VGS = 4.5 V	12	17.5	22	mΩ
	RSS(on)2	IS = 3.0 A, VGS = 3.1 V	13	20	28	
	RSS(on)3	IS = 3.0 A, VGS = 2.5 V	15	23	37	
Body Diode Forward Voltage	VF(S-S)	IF = 6.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance <sup>*1</sup>	Ciss			1780		pF
Output Capacitance <sup>*1</sup>	Coss	VSS = 10 V, VGS = 0 V, f = 1 MHz		410		
Reverse Transfer Capacitance <sup>*1</sup>	Crss			407		
Turn-on delay Time <sup>*1,*2</sup>	td(on)	VDD = 10 V, VGS = 0 to 4.0 V		0.8		μs
Rise Time <sup>*1,*2</sup>	tr	IS = 3.0 A		1.5		
Turn-off delay Time <sup>*1,*2</sup>	td(off)	VDD = 10 V, VGS = 4.0 to 0 V		6.0		μs
Fall Time <sup>*1,*2</sup>	tf	IS = 3.0 A		3.0		
Total Gate Charge <sup>*1</sup>	Qg			15.0		nC
Gate-source Charge <sup>*1</sup>	Qgs	VDD = 10 V, VGS = 0 to 4.0 V, IS = 6.0 A		4.1		
Gate-drain Charge <sup>*1</sup>	Qgd			3.8		

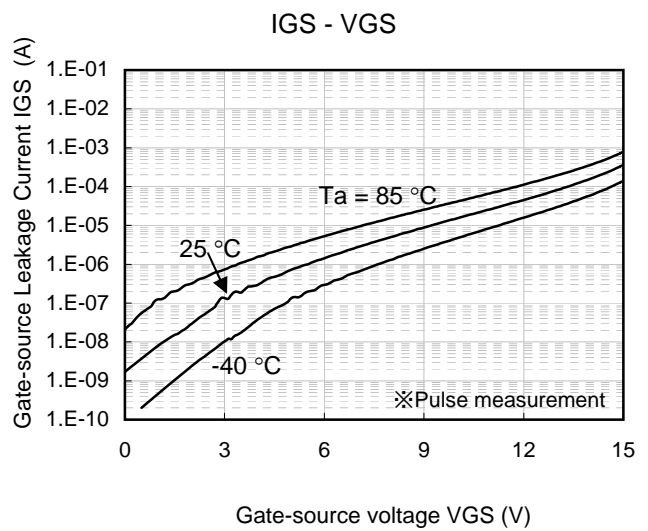
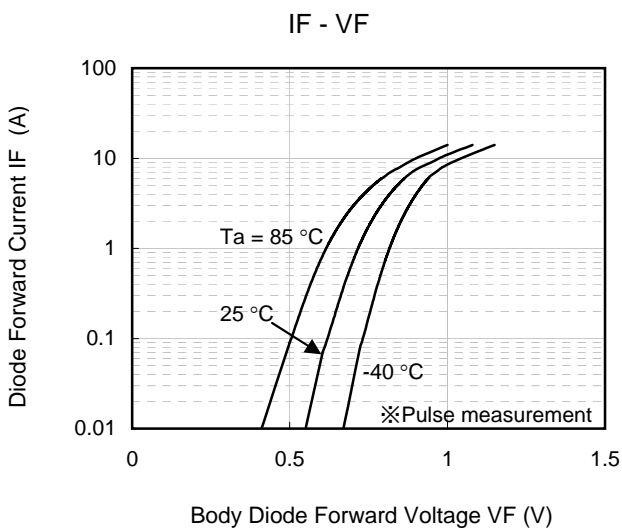
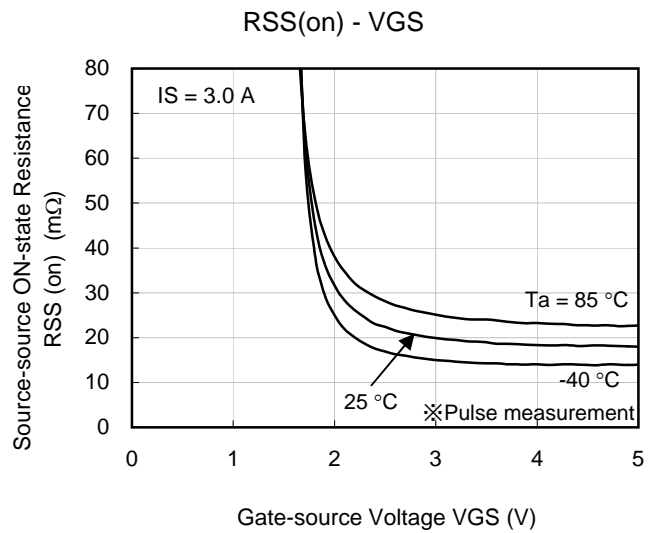
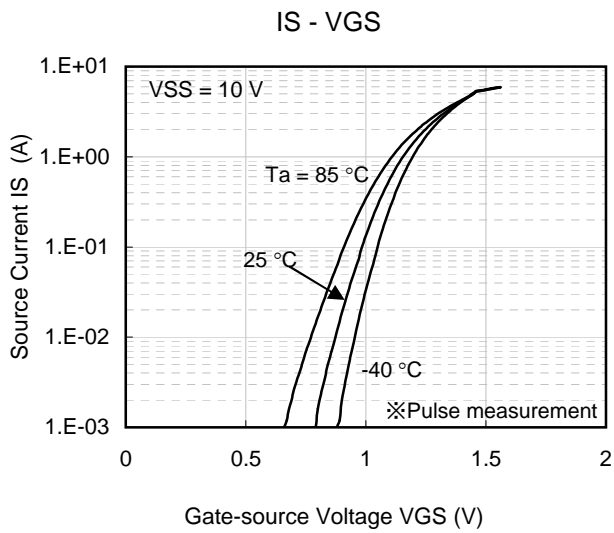
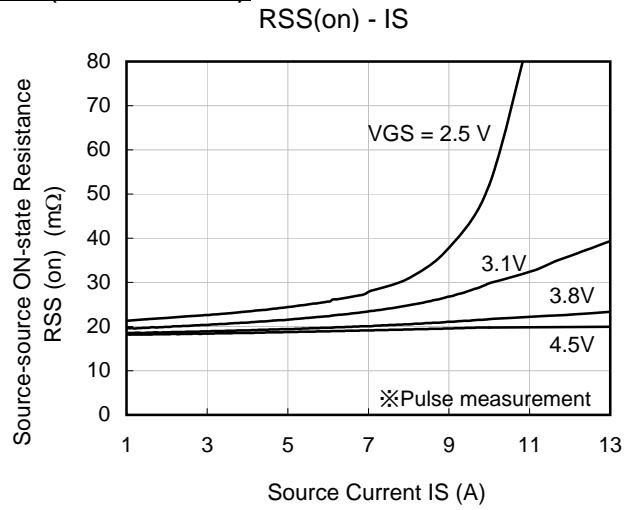
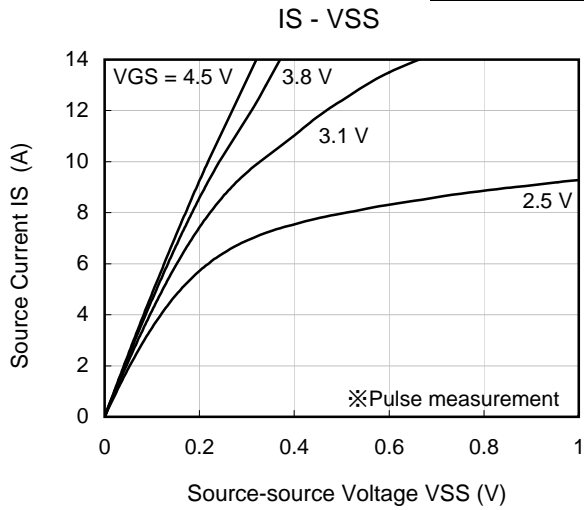
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\*1 Assured by design

\*2 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

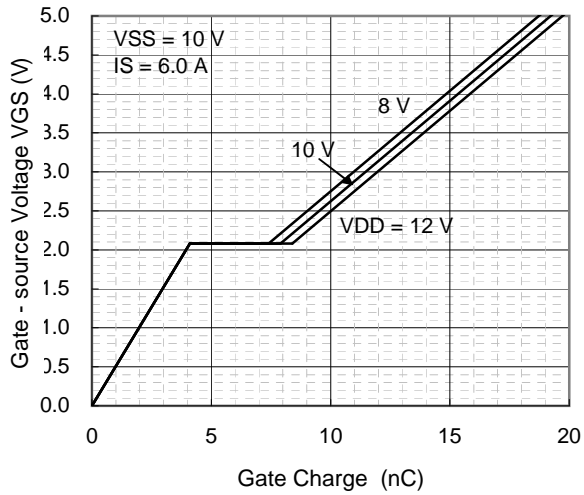


Technical Data ( reference )

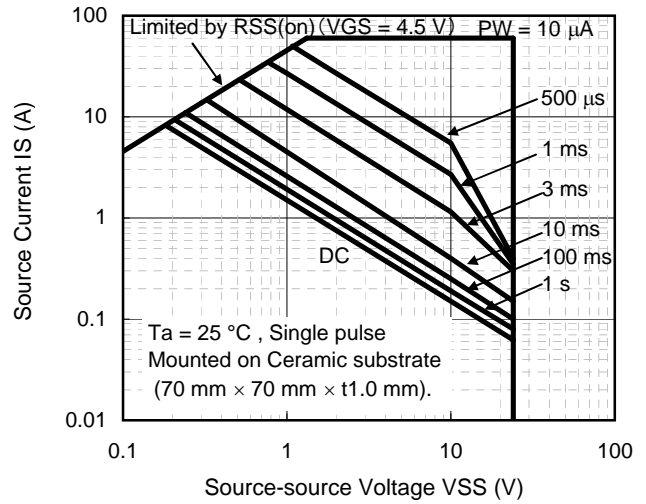


Technical Data ( reference )

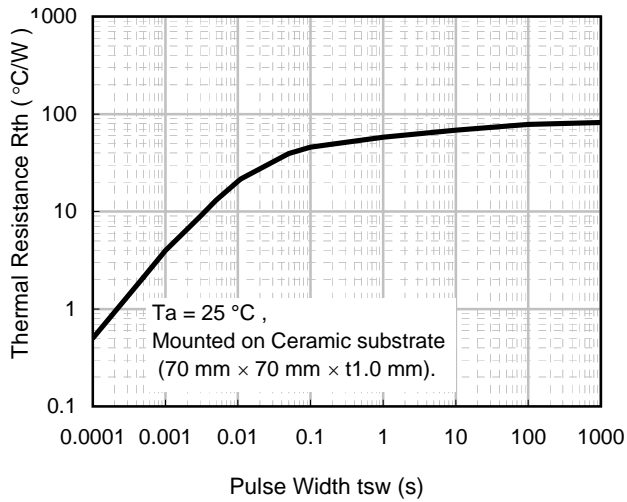
Dynamic Input/Output Characteristics



Safe Operating Area

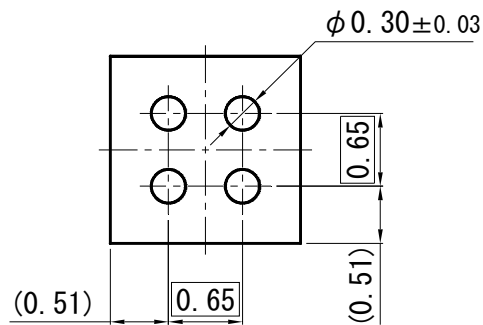
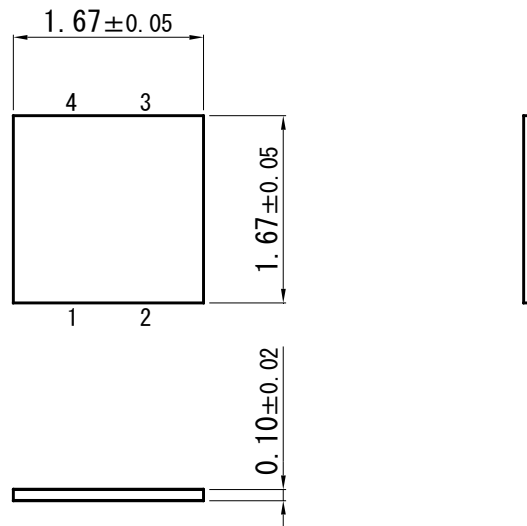


$R_{th} - t_{sw}$

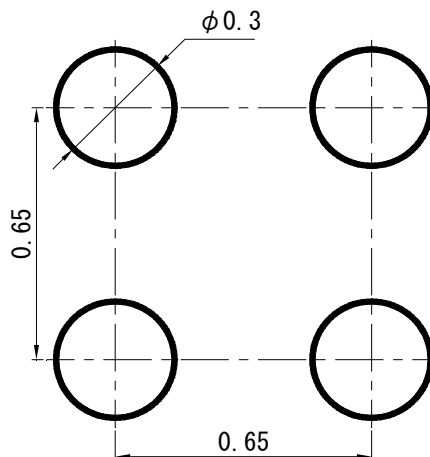


MLGA004-W-1717-RA

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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