Panasonic GaN Power
Breaking Mechanism

APEC2019 Exhibiter Seminar
Mar 19/2019
Panasonic X-GaN™ Power Transistor

First of Normally OFF GaN power Transistor qualifying Mass Production. Fully qualify JEDEC standards and beyond, current collapse free and so on.

**Features**

- GaN Epitaxial Growth Technique on **Si Substrate**
- **Normally-Off** operation with single GaN Device
- **Current-Collapse-Free** 600V and more
- **Zero Recovery** Characteristics

**Panasonic X-GaN™ Family**

<table>
<thead>
<tr>
<th>Product</th>
<th>PGA26E34HA</th>
<th>PGA26E19BA</th>
<th>PGA26E07BA</th>
<th>PGA26H04KA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>DFN 6x4</td>
<td>DFN 8x8</td>
<td>DFN 8x8</td>
<td>PSOP 20</td>
</tr>
<tr>
<td>Small footprint</td>
<td>High Speed</td>
<td>High Speed</td>
<td>High Power</td>
<td></td>
</tr>
<tr>
<td>Blocking Voltage</td>
<td>600V</td>
<td>600V</td>
<td>600V</td>
<td>600V</td>
</tr>
<tr>
<td>Drain Current</td>
<td>8.5A</td>
<td>13A</td>
<td>26A</td>
<td>52A</td>
</tr>
<tr>
<td>Rdson(typ)</td>
<td>270mΩ</td>
<td>140mΩ</td>
<td>56mΩ</td>
<td>32mΩ</td>
</tr>
<tr>
<td>Qg</td>
<td>1nC</td>
<td>2nC</td>
<td>5nC</td>
<td>8nC</td>
</tr>
<tr>
<td>Qr</td>
<td>0nC</td>
<td>0nC</td>
<td>0nC</td>
<td>0nC</td>
</tr>
<tr>
<td>Status</td>
<td>Sampling</td>
<td>Mass Production</td>
<td>Mass Production</td>
<td>Sampling</td>
</tr>
</tbody>
</table>

Samples available from Panasonic X-GaN™ Power Transistor
X-GaN composition

- 6 inch Si-substrate
- GaN/AlN Super-lattice Buffer layer
- P-typ GaN Gate
- Lateral structure

- Cu lead frame 0.5mm thickness
- High temp soldering die attachment
- Resin as conventional
- Au wire 50um diameter

Similar to conventional Si
Major reason of device failure

Not only GaN but all power semiconductors are broken by stress of voltage, current, thermal and/or mechanical stress. The relationship between the Time and Failure Rate of semiconductor is represented by a bathtub curve.

**Early Failures**
Insufficient design margin; thermal deleting design, inrush current, ringing and so on. Escape inspection; incomplete inspection of the Set as well as GaN itself.

**Random Failures**
External stress; electric surge, lightning, misconnection, mechanical damage and so on.

**Wear Out Failures**
Accumulate stress, as voltage, current, thermal and mechanical, and reach to life end. GaN comes to life end due to operating mission profile.
<table>
<thead>
<tr>
<th>Stress</th>
<th>Failure mechanism</th>
<th>Failure mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal &amp; Voltage</td>
<td>Time Dependent Dielectric Breakdown</td>
<td>Leakage current is induced via trap due to thermal &amp; voltage stress and proceed with time. Finally reaches Dielectric Breakdown.</td>
</tr>
<tr>
<td>Voltage</td>
<td>Exceed Electric Field breakdown</td>
<td>Uncontrollable current occurs due to exceeding the withstand electric field, leading breakdown. Eg. VDS&gt;900V.</td>
</tr>
<tr>
<td>Thermal</td>
<td>Thermal breakdown</td>
<td>Collision ions are generated at high temperature, increases current. Leading to short breakdown.</td>
</tr>
<tr>
<td>Current density</td>
<td>Electro migration</td>
<td>Metal ions move by electrons moving at high current density, resulting open circuit or short circuit.</td>
</tr>
<tr>
<td>Thermal</td>
<td>Al Dissolution</td>
<td>Al layer of the gate electrode expands and dissolves at extreme high temperature. At the resulting, G-S short circuit and/or G-D short.</td>
</tr>
<tr>
<td>High Current</td>
<td>Wire fusing</td>
<td>Wire temperature rises due to wire impedance and high current, and it fuse by reaching the melting point.</td>
</tr>
<tr>
<td>Current &amp; Voltage</td>
<td>Current Collapse</td>
<td>It is an issue unique to GaN and its mechanism has not been defined. It is reported shorter lifetime due to current concentration caused by Trapped-Electron interfering electrons moving.</td>
</tr>
<tr>
<td>ESD</td>
<td>ESD: Electrostatic Discharge</td>
<td>Discharge current flows in the device, which is destroyed by local heat generation and electric field concentration.</td>
</tr>
<tr>
<td>Thermal</td>
<td>Resin water vapor explosion</td>
<td>Water vapor explosion occurs due to the rapidly exothermic Die/Wire and the moisture contained in the resin. Open circuit occurs when the resin crushes with wire.</td>
</tr>
<tr>
<td>Humidity &amp; Presser</td>
<td>Corrosion</td>
<td>Routing metal on the die corrodes due to moisture intruding into the package, resulting in short circuit or open circuit.</td>
</tr>
<tr>
<td>Vibration</td>
<td>Metal fatigue</td>
<td>Repeatedly applied physical stress on Metal such as wire, die mounting and so on. Resulting weakening, higher impedance, open circuit.</td>
</tr>
<tr>
<td>Physical stress</td>
<td>Package crack</td>
<td>Physical stress on package by different thermal coefficient between package and PCB, PCB curvature due to mechanical defect.</td>
</tr>
</tbody>
</table>
Uncontrollable current occurs due to exceeding the withstand electric field, leading breakdown. Eg. VDS>900V

The breakdown voltage between Drain and Source is dominated by the breakdown voltage between Drain and Substrate in the vertical direction.

600V X-GaN product series design 900V and more breakdown voltage between Drain and Substrate.
Leakage current is induced via trap due to thermal & voltage stress and proceed with time. Finally reaches Dielectric Breakdown, short circuit.

The insulating layer is immediately broken, when applying voltage is higher than the electric field strength. In the case where the applied voltage is lower than this, degradation progresses with the time, high temperature further degradation accelerates.

Below Weibull plot is X-GaN HTRB test results for the reference, they show TDDB dependency by voltage and temperature.

Weibull plot for various temperatures

Weibull plot for various drain voltage

Leakage defect ➔ D-S short defect
Drain Source Voltage

VDS Electric Field breakdown occurs instantaneously is 900V or more. Design drain-source breakdown voltage 900V or more and 100% tested.

Reliability assurance is carried out at 480V of 80% derating of AMR. TDDB: Time Dependent Dielectric Breakdown occurs when applying Vds<900V, lifetime is determined by the amount of applied stress.
Collision ions are generated at high temperature, increases current. Leading to short circuit.

Generally, Collision ions are generated for the Si device when the junction temperature exceeds 170 degree C, and increases current. Uncontrollable current breaks device. In contrast to Si, one of the GaN advantage is high operating temperature due to large bandgap and high potential barrier. **GaN device itself can operate at 400 degree C or more.** However, **X-GaN composes conventional Si materials as packaging resin, routing metal & passivation on die and so on, withstanding 150 degree C.** GaN does not yet reach thermal breakdown at the temperature that had occurred in conventional Si. Because the GaN can operate to a higher temperature, they can see different breakdown mechanism that could not be seen with Si.
Electro migration occurs at high temperature and high current density. As the electron momentum moves to the metal atom, the metal ions in the conductor gradually move. It can cause the eventual loss of connection or short to Adjacent routing.

Electron push Al ion

Metal ions gradually move

Resulted short circuit or open.

Metal ions movement occurs Al empty.

Loss of connection

Over flow Metal ions from contact window.

Short to Adjacent routing.

Gate Open defect

Gate source Short defect
Al Dissolution

Al layer of the gate electrode expands and dissolves at extreme high temperature. At the resulting, G-S short circuit and/or G-D short.

Drain region heat up extremely by short circuit or other similar occasion.

When the temperature approaching the melting point, 660 deg C.

The Al of Gate melts and travels through the gap and short circuit with Source terminal.

Accelerate Gate Source short by the combination of Al dissolution and Electro Migration.
Wire fusing

Wire temperature rises due to wire impedance and high current, and it fuse by reaching the melting point.

Source & Drain: Number of wires is designed to allow the current that is greater than the device current capability. The wire may fuse by secondary failure of device short breaking.

Gate & Kelvin Source: current capability is 3A and more. Wire fusing by miss-connection or/and abnormal rush current.

Gate Open defect

SK Open defect

Fusing by IG>3A

Fusing by ISK>3A
Current Collapse mechanism

Electrons TRAP, which might cause crystal dislocation, and blocks Drain current flow, results in higher Dynamic Rdson called Current Collapse.

**Mechanism**

- Occurs Minor Crystal dislocation by Compressive Strain though implemented Super-lattice buffer.

- Trapped Electron occur on the surface and bulk, which might be caused Crystal Dislocation.

  - The number of Trapped Electrons has Vds correlations.
  - High electronic fields capture Trapped Electron easily.

**Static Condition**
(No switching)

Reproduce same Rdson value as datasheet

**Dynamic Condition**
(Switching Operation)

RDSon rises

Drain voltage waveform

Trapped Electrons block normal electron mobility

Source

Gate

Drain

p-GaN

AlGaN

GaN

Buffer layer

Si-substrate

- Source

- Gate

- Drain

Trapped Electron

Blocked

Blocked

Blocked
Current Collapse countermeasure

General method i.e. process countermeasure, reaches about 500V, but not enough. HD-GIT structure injects Hole and eliminate Trapped Electron immediately.

Approach 1  
General method

Reduce Compressive Strain to minimize Crystal Distortion

Fine tuning Super-lattice Buffer. Fine tuning GaN epitaxial growing.

Approach 2  
Panasonic Original method

Panasonic unique structure HD-GIT: **Hybrid-Drain-embedded GIT (HD-GIT)**

2\textsuperscript{nd} Drain as similar to gate structure is automatically turn on during the switching period.

**Release Trapped Electrons**
By Hole(+) injected from 2\textsuperscript{nd} Drain

**Former Panasonic GaN structure**

**Panasonic X-GaN structure**

**HD-GIT**  
**No Degradation**

**Conventional**

**HD-GIT**  
**No collapse**

**RON Ratio**

**HD-GIT**  
**No Degradation**
Concentration of current and electric field occur due to Current Collapse, and Time Dependent Dielectric Breakdown is accelerate by Drain-Source voltage and Drain current.

Concentration of Current and electric field due to Current Collapse progresses degradation with time, accelerate degradation by higher voltage and higher current. Below Weibull plot is X-GaN D-HTOL test results, they show TDDB dependency by voltage and current. Dynamic High Temperature Operating Life D-HTOL test is unique for GaN to define the relationship between Current Collapse and lifetime.

** PGA26E07BA **

D-HTOL test results (PGA26E07BA)

X-GaN demonstrate long lifetime of 3600h and more under the D-HTOL test.

Leakage/High Rdson defect ➔ D-S short defect
X-GaN Gate configuration.

To achieve Normally OFF, X-GaN adopts pGaN gate which is a commonly used structure. pGaN layer lifts up potential at the channel and blocked electron movement.

To improve Gate robustness, X-GaN adopts resistive connection which is unique structure. Wider driving margin by Current Control Gate, and it is possible to release the voltage limit of Gate.

GaN pn junction characteristic

X-GaN: Current control Gate

Normal Operation Absolute Maximum Peak
>5mA 50mA 1.5A

Wider Margin

Conventional: Voltage control Gate

Normal Operation Absolute Maximum Peak
6V 7V 10V

No Margin
Regarding to Gate voltage rating, X-GaN has only negative VGS rating.
Positive VGS rating is determined by Gate Current.

### Absolute Maximum Ratings

** PGA26E07BA **

<table>
<thead>
<tr>
<th>No.</th>
<th>Item</th>
<th>Symbol</th>
<th>Values</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Gate-source voltage (DC) *1</td>
<td>VGSS</td>
<td>-10</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td>*VGSS+ is given by IG ratings</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>*See application note</td>
</tr>
<tr>
<td>4</td>
<td>Gate current (DC) *1</td>
<td>IG</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>mA</td>
<td>*See application note</td>
</tr>
<tr>
<td>5</td>
<td>Gate current (pulse) *3.4</td>
<td>IGP</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>A</td>
<td>*See application note</td>
</tr>
<tr>
<td>6</td>
<td>Electric gate charge</td>
<td>QGP</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>32</td>
<td>nC</td>
<td>*f=200kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>*See application note</td>
</tr>
</tbody>
</table>

- **Negative Gate voltage rating**
- **No Positive Gate voltage rating**
- **Consists by current items**

**G-S short defect**

- **Surge Protection**
- **Gate threshold**
- **Plateau Voltage**

**No degradation, no breaking**

No positive limitation for Gate voltage.

All breakdown events for positive by consisting gate current rating.
Gate Current

X-GaN has no positive VGS rating, AMR determined by Gate Current.
Unlimited VGS rating; Gate does not break by voltage rise due to gate current surge.

<table>
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<tr>
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<th>Values</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Gate current (DC) *1</td>
<td>IG</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>5</td>
<td>Gate current (pulse) *3,4</td>
<td>IGP</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>6</td>
<td>Electric gate charge</td>
<td>QGP</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
</tbody>
</table>

A. ABSOLUTE MAXIMUM RATINGS (T) = 25°C, unless otherwise specified.

**Degradation ➔ Leakage defect ➔ D-S short defect**

**D-S open defect**

**IG DC**

IG = 50 mA

**IG Pulse**

IGP = 1.5 A

Wire fusing
Open circuit

50 mA

1.5 A

3.0 A

Gate current

TDDB: Time Dependent Dielectric Breakdown

Long

Short
Drain Current

ID and IDR are calculated with the ideal usage condition.
ID itself is not the direct reason of breakdown. Device breaks when junction temperature reaches appropriate temperature.

ID pulse described in Datasheet means the value caused by the maximum gate DC current IG.
ID itself is not the direct reason of breakdown. Device breaks when junction temperature reaches appropriate temperature.

A. ABSOLUTE MAXIMUM RATINGS (T) = 25 °C , unless otherwise specified) 

<table>
<thead>
<tr>
<th>No.</th>
<th>Item</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Drain current (DC) (Tc = 25°C) *1</td>
<td>ID</td>
<td>Min. -</td>
<td>Typ. -</td>
<td>Max. 26</td>
</tr>
<tr>
<td>8</td>
<td>Drain reverse current (DC) (Tc = 25°C) *1</td>
<td>IDR</td>
<td>Min. -</td>
<td>Typ. -</td>
<td>Max. 26</td>
</tr>
<tr>
<td>9</td>
<td>Drain current (pulse) *5 (Tc = 25°C) *1</td>
<td>ID pulse</td>
<td>Min. -</td>
<td>Typ. -</td>
<td>Max. 61</td>
</tr>
<tr>
<td>10</td>
<td>Drain reverse current (pulse) *5 (Tc = 25°C) *1</td>
<td>IDR pulse</td>
<td>Min. -</td>
<td>Typ. -</td>
<td>Max. 61</td>
</tr>
</tbody>
</table>

Degradation ➔ D-S short defect

Thermal breakdown due to thermal design
Limited by SOA

DC ID=26A

pulse ID pulse=61A

Wire fuse
Open circuit

D-S open defect

26A 61A 90A Drain Current

ID pulse described in Datasheet means the value caused by the maximum gate DC current IG.
ID itself is not the direct reason of breakdown. Device breaks when junction temperature reaches appropriate temperature.
Safe Operating Area

Once exceed SOA, Safe Operating Area, device immediately breaks.

![Graph showing Safe Operating Area](image)

- **Current limited area**: even if it exceeds this area, breakdown does not instantaneously occur but depends on junction temperature.
- **Voltage limited area**: it is specified for 600V in Datasheet for convenience, but in fact it is designed with over 900V and guaranteeing 750V for transient.

Figure 4: Safe operating area $T_c = 25 \, ^\circ\text{C}$
Resin explosion

The resin contains moisture as usual. Die surface temperature is rapidly rising by high voltage and high current due to short circuit. Then Water vapor explosion occurs.

1. Short Circuit
2. Id=70A and Vds=400V generate heat on Die surface.
3. The moisture of the resin adjacent to the Die surface locally evaporates rapidly.
5. Resulted open circuit, if the resin blows away with wire.

Other occasion: resin blows away by wire heat.

Note: make sure the soldering condition and the storage environment in side delivery specifications.
ESD: Electrostatic Discharge

**X-GaN achieves 2000V HBM Gate ESD capability by adopting unique ESD countermeasures.**
Gate of GaN has a structural weakness on ESD. That measure is an important issue for GaN device development.

### Actual Measurement Value
PGA26E07BA, n=3 from each 3 lot

<table>
<thead>
<tr>
<th></th>
<th>HBM</th>
<th>MM</th>
<th>CDM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Positive</td>
<td>Negative</td>
<td>Positive</td>
</tr>
<tr>
<td>Gate-Source</td>
<td>&gt;5000V</td>
<td>&gt;5000V</td>
<td>500V</td>
</tr>
<tr>
<td>Gate-Drain</td>
<td>&gt;5000V</td>
<td>2300V</td>
<td>1200V</td>
</tr>
<tr>
<td>Drain-Source</td>
<td>&gt;5000V</td>
<td>&gt;5000V</td>
<td>&gt;1500V</td>
</tr>
</tbody>
</table>

X-GaN has ESD protection diode between Gate and Source. Its breakdown voltage is approximate VGS=-10V. Instantaneous Breakdown was occurred when VGS<-10V.

Positive Gate voltage rating is determined by Gate Current. Refer to next page.
Panasonic Total Product Management Capability

- **Design**
- **Wafer Process Control**
- **Probe Test**
- **Package Assembly**
- **Final Test**
- **Delivery**

**Robustness design**
- Normal Operation: >5mA
- Absolute Maximum: 50mA
- Peak: 1.5A
- Wider Margin

**High Reliability design**
- Source
- Gate
- Drain
- AlGaN
- GaN
- Buffer layer
- Si - substrate

⇒ Accumulate Lifetime data
⇒ Suggest Actual Lifetime from operation mission profile

- **Reduce Random Failures**
- **Reduce Wear Out Failures**
- **Reduce Early Failures**
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