Panasonic web simulation for Totem Pole PFC (TTP) featuring:

1. PGA26E07BA 600V 70mΩ / PGA26E19BA 600V 190mΩ X-GaN Power Transistor
2. AN34092B Single channel X-GaN Gate Driver IC
3. Web-based simulator PowerEsim

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X-GaN TTP Simulation Manual Ver. 1.1
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Key device part number

- X-GaN power transistor (PGA26E07BA / PGA26E19BA)
  - Blocking voltage: 600V
  - Pulse peak I_{DS}: 61A / 23A
  - I_{DS} (continuous): 31A / 15A
  - RDS(on) max: 70mΩ / 190mΩ
  - Normally-off device

- X-GaN driver (AN34092B)
  - Supports high switching frequency (~4MHz)
  - Achieved safe operation by
    - negative voltage source, active miller clamp
  - Facilitate gate drive design
    - high precision gate current source
Overview

Totem pole PFC (TTP) is one of the valuable topologies for GaN implementation. TTP is able to achieve over 99% efficiency ideally. However, conventional Si device can't achieve 99% due to its high recovery loss. X-GaN has '0' Qrr characteristic i.e. negligible recovery loss makes it very suitable for TTP topology. However, TTP PFC & GaN is new to all power electronics engineers.

To enable power supply engineers to understand the operation of TTP PFC and the GaN performance, Panasonic has created an on-line simulator using PowerEsim. This on-line simulator is useful for feasibility study to implement GaN on a TTP PFC without having the need to create an actual evaluation board first. It also helps to understand the gate drive design necessary for X-GaN.

Features

- Simulator: PowerEsim by PowerELab Ltd.
- Topology: Totem pole PFC (fixed schematic)
- Various Input & Output conditions.
- Optimization of device & passive values.
- Key Waveforms
- Each component losses.
- Loop stability, EMI and Harmonics.
- Easy comparison with other devices.
- Save/load features for all your designs

http://www.poweresim.com/

PowerEsim - Free on-line switch mode power supply SMPS circuit, magnetic, transformer, thermal, stability, Monte Carlo, DVT, MTBF, life, current harmonics, simulation & design software tools.
Getting started with PowerEsim simulation

PowerEsim is a powerful on-line simulator which can be accessed in few simple steps.


2. Use Panasonic sponsor account login page to get the full feature

Click “Free Account”

Click on Panasonic sponsor account for full version usage
3. You are now ready to use the full design features!

You can start designing using full design features brought to you by Panasonic.
Design options

There are several options to start with your designs.

1. Start designing based on specification

   ![Set the specification]

   ![Add more outputs?]

2. Start designing based on topology

   ![Choose application]

   **Totem pole PFC** will be the design example presented in this manual

3. Start from reference designs

   ![Select Panasonic reference designs]
Schematic outline

Totem pole PFC (TTP) schematic shown below uses Panasonic X-GaN 70mΩ power transistor (PGA26E07BA) and X-GaN driver IC (AN34092B). This topology can achieve above 99% efficiency ideally using our X-GaN. Main losses components in this topology are as followings:

1. PFC choke coil (L1)
2. High frequency leg (M1, M2)
3. Rectification leg (M3, M4)

Figure 1: Totem pole PFC (TTP) schematic on PowerEsim
Design considerations

- PFC choke coil design

PFC choke coil is the highest losses component in totem pole PFC design. Micrometals choke coil 1.18mH is selected to keep ripple current below 1A. At initial stage, total choke coil loss is targeted to be around 54%, i.e. 6.5W at 100kHz frequency. From default copper wire AWG16 x 1, it is desired to change to AWG16 x 2 to reduce DC copper (conduction) losses significantly.

![Figure 2: Choke coil parameters](image1)

![Figure 3: Choke coil current](image2)
Qrr parameter (M1, M2) is very crucial for fast switching leg in totem pole design. Existing state-of-the-art MOSFET is still in microcoulombs (μC) range. Panasonic X-GaN 600V 70mΩ (PGA26E07BA) is selected from the component list because of its high Figure Of Merit (F.O.M) in $\text{Ron} \cdot \text{Qrr}$. Table 1 shows a comparison of our X-GaN compared to MOSFET.

R1 and R4 are default resistors provided in the TTP schematic. They are not in use, hence both are set to 0Ω on the schematic. M1 and M2 gate terminals labeled as “M1 gate” and “M2 gate” on Figure 4 are connected to Panasonic X-GaN driver IC (AN34092B), which will be discussed on next page.

Table 1: X-GaN vs. equivalent SJ-MOS IPL60R199CP

<table>
<thead>
<tr>
<th></th>
<th>PGA26E07BA</th>
<th>IPL60R199CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDSS</td>
<td>600 V</td>
<td>600 V</td>
</tr>
<tr>
<td>IDSS</td>
<td>31 A</td>
<td>16.4 A</td>
</tr>
<tr>
<td>Ron (typ)</td>
<td>56 mΩ</td>
<td>180 mΩ</td>
</tr>
<tr>
<td>Qg</td>
<td>5.0 nC</td>
<td>32 nC</td>
</tr>
<tr>
<td>Qrr</td>
<td>~0 nC</td>
<td>5.5 uC</td>
</tr>
<tr>
<td>$\text{Ron} \cdot \text{Qrr}$</td>
<td>~0 nC.Ω</td>
<td>990 nC.Ω</td>
</tr>
</tbody>
</table>

[1] RC snubber is not needed for this design. Hence R7 / R8 are both set to 0Ω, and both C4 / C5 are set to very small values.

Figure 4: X-GaN on M1 / M2
- PWM driver design (U1, U2)

As indicated from previous page, M1 gate connection to R10 / R12 / C6, and M2 gate connection to R11 / R13 / C7 are shown on Figure 5 below. Panasonic X-GaN driver IC (AN34092B) is specially designed to drive high speed X-GaN power transistor (M1, M2).

![Figure 5: PWM gate driver design using AN34092B](image)

- Rectification leg design (M3, M4)

M3 and M4 are used to replace slow diode for 50Hz / 60Hz rectification. Hence Ron parameter of M3 / M4 is very crucial to achieve lowest conduction losses possible. A single MOSFET device with 15mΩ Ron is used for M3 and M4 each.

![Figure 6: Rectification leg with M3 / M4](image)
- Feedback loop design

For loop stability, 45 degree phase margin or more is desired. Default design gives 7.4 degree phase margin. After feedback circuit optimizations, 45.28 degree phase margin is obtained as shown on Figure 9.

Figure 7: TTP voltage feedback block

Figure 8: Transient output waveform

Figure 9: Loop analysis results

R3: 1kΩ → 564Ω
R29: 750kΩ
R30: 390kΩ
R31: 390kΩ
R32: 10kΩ
C2: 680nF → 22μF
C3: 680nF → 1pF

R3: 1kΩ
C3: 680nF
C2: 680nF

Unity-gain frequency: 34.2 Hz
Phase margin: 7.4 degree
Phase margin is too low!

After optimizations

Phase margin: 45.28 degree
Phase margin is OK!
DVT report
- Before optimizations

Simulation was carried out at input 240Vac and output 400V / 3A (1.2kW). Initial DVT results failed for C24 and C25 due to voltage rating issue. After replacing the 250VAC rated capacitor to 300VAC, voltage rating test passed as shown on Table 2.

![C24, C25 rating: 250VAC → 300VAC](image)

Figure 10: DVT report failure correction on C24, C25

Table 2: Detailed DVT report with focus on FAIL items

<table>
<thead>
<tr>
<th>Ref</th>
<th>Description</th>
<th>Simulated Value</th>
<th>Rated Value</th>
<th>Rated Factor</th>
<th>Result</th>
<th>Message</th>
</tr>
</thead>
<tbody>
<tr>
<td>C24</td>
<td>2.2 nF 250 Vac 0.2 Ω 110°C 19x13x5 mm PECY2 20%</td>
<td>Vpk: 336.7 V</td>
<td>353.6 V</td>
<td>0.95</td>
<td>Reject</td>
<td>You may need to select a capacitor having higher sustain voltage rating.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Loss: 0.065 W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Irms: 164.6 uA</td>
<td>0.4185 A</td>
<td>1</td>
<td>Pass</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tj: 60 °C</td>
<td>110 °C</td>
<td>1</td>
<td>Pass</td>
<td></td>
</tr>
<tr>
<td>C25</td>
<td>2.2 nF 250 Vac 0.2 Ω 110°C 19x13x5 mm PECY2 20%</td>
<td>Vpk: 336.7 V</td>
<td>303.6 V</td>
<td>0.95</td>
<td>Reject</td>
<td>You may need to select a capacitor having higher sustain voltage rating.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Loss: 0.065 W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Irms: 164.6 uA</td>
<td>0.4185 A</td>
<td>1</td>
<td>Pass</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tj: 60 °C</td>
<td>110 °C</td>
<td>1</td>
<td>Pass</td>
<td></td>
</tr>
</tbody>
</table>

C24/C25 Voltage rating: **FAIL**

After optimizations

| C24 | 2.2 nF 300 Vac 110°C 13x9x4 mm R-41 ARCOTRONICS 10% | Vpk: 336.9 V | 424.3 V | 0.95 | Pass |         |
|     | Loss: 0.008 W | Irms: 164.7 uA | 0.4185 A | 1 | Pass |         |
|     |             | Tj: 50 °C | 110 °C | 1 | Pass |         |
| C25 | 2.2 nF 300 Vac 110°C 13x9x4 mm R-41 ARCOTRONICS 10% | Vpk: 336.9 V | 424.3 V | 0.95 | Pass |         |
|     | Loss: 0.008 W | Irms: 164.7 uA | 0.4185 A | 1 | Pass |         |
|     |             | Tj: 50 °C | 110 °C | 1 | Pass |         |
After optimizations

Overall circuit design verification passed after component optimizations. Results shown below on Table 3. Items passed include “Insufficient gate drive”, “Excess gate drive” and “OCP” checks.

Table 3: Circuit design verification

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insufficient Gate Drive</td>
<td>Pass</td>
</tr>
<tr>
<td>Excess Gate Drive</td>
<td>Pass</td>
</tr>
<tr>
<td>OCP</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Overall component verification passed after component optimizations. Selectively displayed below on Table 4 are simulation results for Panasonic X-GaN devices (M1 and M2) only.

Table 4: Component verification

<table>
<thead>
<tr>
<th>Ref</th>
<th>Description</th>
<th>Simulated Value</th>
<th>Rated Value</th>
<th>Rated Factor</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>54 mΩ 600 V 15 A PGA26E08BA Panasonic</td>
<td>Vpk: 574.5 V</td>
<td>600 V</td>
<td>1</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I rms: 3.718 A</td>
<td>15 A</td>
<td>0.8</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ipk: 7.256 A</td>
<td>24 A</td>
<td>0.8</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pd: 1.585 W</td>
<td>104 W</td>
<td>0.7</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tj: 60 °C</td>
<td>150 °C</td>
<td>0.8</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Var: 574.5 V</td>
<td>600 V</td>
<td>1</td>
<td>Pass</td>
</tr>
<tr>
<td>M2</td>
<td>54 mΩ 600 V 15 A PGA26E08BA Panasonic</td>
<td>Vpk: 574.5 V</td>
<td>600 V</td>
<td>1</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I rms: 3.718 A</td>
<td>15 A</td>
<td>0.8</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ipk: 7.256 A</td>
<td>24 A</td>
<td>0.8</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pd: 1.585 W</td>
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<td></td>
<td>Tj: 60 °C</td>
<td>150 °C</td>
<td>0.8</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Var: 574.5 V</td>
<td>600 V</td>
<td>1</td>
<td>Pass</td>
</tr>
</tbody>
</table>
Waveform simulation results

**<Input voltage & input current>**

- CH1: Input AC voltage
- CH2: Input AC current

**<Input voltage & bulk capacitor voltage>**

- CH1: Input AC voltage
- CH2: Rectified bulk capacitor voltage

**<M1 switching>**

- CH1: M1 switching voltage
- CH2: M1 switching current

**<M2 switching>**

- CH1: M2 switching voltage
- CH2: M2 switching current

Figure 11: Typical TTP simulation waveforms
Efficiency results

After optimizations on PFC choke coil (L1) and EMI input stage components, following final efficiency results are as shown below.

Pout = 500W (115Vac input)

![Efficiency graph for 500W](image)

Pout = 1.2kW (240Vac input)

![Efficiency graph for 1.2kW](image)

Pout = 2kW (240Vac input)

![Efficiency graph for 2kW](image)

Figure 12: Efficiency results for 500W, 1.2kW and 2kW designs
Loop stability results

With design tweaking on feedback circuits, more than 45 degree phase margin are ensured for all output power conditions. This is important to keep stability at all output power conditions.

Pout = 500W (115Vac input)

Unity-gain frequency: 3.76Hz

Phase margin: 47.68 degree

Pout = 1.2kW (240Vac input)

Unity-gain frequency: 9.68Hz

Phase margin: 49.45 degree

Pout = 2kW (240Vac input)

Unity-gain frequency: 9.19Hz

Phase margin: 50.6 degree

Figure 13: Loop stability results for 500W, 1.2kW and 2kW designs
THD results

High power factor and low THD results are obtained from every output power condition.

**Pout = 500W (115Vac input)**

![Graph showing THD results for 500W design]

- $V_{i\text{rms}} = 115V$, $I_{i\text{rms}} = 4.432A$, $I_{\text{peak}} = 6.317A$
- Crest factor = 1.43, $I_{\text{fund}} = 4.431A$, Input power = 507.7W
- Power factor ~ 1
- THD = 2.937%

**Pout = 1.2kW (240Vac input)**

![Graph showing THD results for 1.2kW design]

- $V_{i\text{rms}} = 240V$, $I_{i\text{rms}} = 5.079A$, $I_{\text{peak}} = 7.344A$
- Crest factor = 1.45, $I_{\text{fund}} = 5.075A$, Input power = 1.21kW
- Power factor = 0.99
- THD = 4.941%

**Pout = 2kW (240Vac input)**

![Graph showing THD results for 2kW design]

- $V_{i\text{rms}} = 240V$, $I_{i\text{rms}} = 8.49A$, $I_{\text{peak}} = 12.24A$
- Crest factor = 1.44, $I_{\text{fund}} = 8.485A$, Input power = 2.023kW
- Power factor = 0.99
- THD = 4.572%

Figure 14: THD results for 500W, 1.2kW and 2kW designs
Input harmonic results

Simulated harmonic results passed every output power condition. Shown are the results tested with Class A limit, EN61000-3-2 standard.

Pout = 500W (115Vac input)

Simulated result: PASS

Pout = 1.2kW (240Vac input)

Simulated result: PASS

Pout = 2kW (240Vac input)

Simulated result: PASS

Figure 15: Input harmonic results for 500W, 1.2kW and 2kW designs
Differential mode EMI results

Simulated differential mode EMI results passed every output power condition. Shown are the results tested with Class B limit, EN55022 standard.

Pout = 500W (115Vac input)

Simulated result: PASS

Pout = 1.2kW (240Vac input)

Simulated result: PASS

Pout = 2kW (240Vac input)

Simulated result: PASS

Figure 16: Differential mode EMI results for 500W, 1.2kW and 2kW designs
Noise current waveforms

Pout = 500W (115Vac input)

![Noise current waveform for 500W design](image)

Pout = 1.2kW (240Vac input)

![Noise current waveform for 1.2kW design](image)

Pout = 2kW (240Vac input)

![Noise current waveform for 2kW design](image)

Figure 17: Noise current waveforms for 500W, 1.2kW and 2kW designs
Important Notice

Please read and understand the following items, "Restriction" and "Limitation of Use" before using the web simulator. Panasonic reserves the right to change these terms at any time without notice.

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- The simulator is intended for use as conceptual and engineering study. It should not be used as actual verification purpose.
- This simulator is not intended for a finished end-product fit for general consumer use.
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- Fine tuning on actual board is necessary in order to achieve desired performance and results.
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(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. We do not guarantee quality for disassembled products or the product re-mounted after removing from the mounting board. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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