GaN-Tr Application Note
（PGA26E06BA）

Panasonic Semiconductor Solutions Co., Ltd.
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1. Introduction

- This product features『High-speed Switching』, 『Low On-resistance』 will contribute to miniaturization of equipment, and higher efficiency
- By using GaN material, it provides the value that exceeds the performance of Si device
- This document shows how to use Part Number: PGA26E06BA (DFN Package 56mohm typical) and important points are described.

Panasonic GaN Power Transistor features are 『High-speed Switching』、『Low On-resistance』, 『Miniaturization of equipment』, and it greatly contributes to 『High Efficiency』.

Nowadays, typical power transistors used in the power equipment such as power supplies and inverters are the Power MOSFET and IGBT made by Si (Silicon) material. But, significant performance improvement are not expected in the future, because the trade-off between on-resistance and breakdown electric field are closing to the theoretical performance limit determined by the physical properties of the Si. In this way, GaN(Gallium nitride) whose theoretical performance limit is significantly higher compared to Si, has attracted much attentions as next generation semiconductor material.

Because of the excellent basic performance of the GaN material, GaN Power Transistor achieves high breakdown voltage and low on-resistance more than the limit of Si. Furthermore in term of high-speed switching characteristics, it will be able to provide a new value to the product. This application note, which is written for those who have basic knowledge on circuit design and Si power devices, to understand how to use our GaN power transistor. We hope that we can serve you in your product design and contribute to the product development of your company.

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2. Features and Benefits of GaN Power Transistor

Features of GaN Power Transistor

- Low on-resistance / 600V Breakdown
  Low on-resistance and small PKG size
  (Size: 8 × 8mm, on-resistance: 56mohm)

- High Speed Switching
  Small gate capacitance device
  Small parasitic inductance package

- Conduction in both directions
  Possible conduction from the source to drain
  Good recovery characteristics

Merits to onboard equipment

- Low Loss
  Low Heat
  High Efficiency

- High frequency operation
  Peripheral components miniaturization

- External diode is not necessary
  For application with recirculation process, external diode is unnecessary

Switching Waveform

- **Turn-on**
  - Vds = 400V
  - dV/dt = 200 V/ns
  - Ids = 5 A
  - 0 V
  - 5ns/div

- **Turn-off**
  - Vds = 400V
  - dV/dt = 140 V/ns
  - Ids = 15 A
  - 0 V
  - 5ns/div

Note: dV/dt rising and falling are taken from 280V to 120V
This result depends on the operation condition such as a drive circuit and PCB layout.

DFN Package

- Parasitic inductance of package is small
- Drive circuit design easy with driving source terminal (S1)
2.1 GaN Power Transistor Gate Characteristics

We'll explain the behaviour of the gate voltage and the drain voltage during turn-on.

<Gate voltage in the case where a constant current is injected to the gate, the change of the drain voltage>

Gate voltage Vgs in the case where the gate of GaN Power Transistor is injected with constant current, change of the drain voltage Vds is described as below. (Please refer to the test circuit shown in Figure 2.1-2)

Figure 2.1-2 test circuit shows when the constant current is applied to the gate, accumulation of charge Q will increase in proportion to the application time of constant current. This is shown in Figure 2.1-1. From T0 to Ta, Tb, Tc at Figure 2.1-1, the gate-to-source voltage change is shown in black solid line as the time passes, and that slope changes in three stages. So far, Si power MOSFET, IGBT and GaN power transistor have the same behaviour.

After Tc, gate voltage of Si power transistor and IGBT is increased with injection of current. However, this gate voltage of GaN power transistor increase is clamped by the voltage between gate and source (Vgs) determined by gate current (lg). Since parasitic diode is formed between gate and source, gate voltage is clamped by forward current flow into this diode.

Next page shows the detailed explanation about the changes in gate and drain voltages during each period. It should be noted that when drain voltage Vds is reduced during Tb~Td, it indicates that the transistor is turned on.

![Figure 2.1-1 Changes of Vgs, Vds when transistor ON (When gate is injected with constant current)](image)

![Figure 2.1-2 Gate voltage measuring circuit](image)
# 2.1 GaN Power Transistor Gate Characteristics

<table>
<thead>
<tr>
<th>Section</th>
<th>Gate Electric Charge Mechanism</th>
<th>Gate Charge</th>
</tr>
</thead>
<tbody>
<tr>
<td>0⇒Ta</td>
<td>Begins to charge the gate-source capacitance (Cgs).</td>
<td>Gate-Source Charge Qgs</td>
</tr>
<tr>
<td>Ta⇒Tb</td>
<td>Gate voltage reaches the threshold voltage, until the plateau voltage in the (Ta⇒Tb) period, and drain current begins to flow. Take note that since Ciss=dQ/dVgs, the slope of Vgs waveform is given by 1/Ciss.</td>
<td>Gate-Drain Charge Qgd</td>
</tr>
<tr>
<td>Tb⇒Tc</td>
<td>Drain current flows and Vds drops. Ciss appears larger due to the Miller effect of the negative feedback of the feedback capacitance Crss between drain-gate. Hence, the Vgs slope, which is the reciprocal of Ciss, is gradual. At the same time, current begins to flow into the parasitic diode which is formed between the gate and source.</td>
<td>Charge amount Q’ for the flow of current of the diode between gate-source</td>
</tr>
<tr>
<td>Tc⇒Td</td>
<td>Turn on is completed. Miller effect disappears with the saturation of Vds. Slope of Vgs becomes steep.</td>
<td></td>
</tr>
<tr>
<td>Td &lt; T</td>
<td>By flowing constant current into the parasitic diode between the gate and source, on-state is maintained.</td>
<td></td>
</tr>
</tbody>
</table>

**<Gate Current Path>**

<table>
<thead>
<tr>
<th>0⇒Ta</th>
<th>Ta⇒Tb</th>
<th>Tb⇒Tc</th>
<th>Tc⇒Td</th>
<th>Td &lt; T</th>
</tr>
</thead>
</table>

The amount of charge to the gate voltage Vg until full conduction is total gate charge Qg (Qg=Qgs + Qgd + Q’).
2.2 On Operation (Forward direction and Backward direction)

ON operation (forward and backward direction) is described using the following circuit

<table>
<thead>
<tr>
<th>(1) ON Operation (Forward Direction)</th>
<th>(2) OFF Operation (Like diode)</th>
<th>(3) ON Operation (Backward Direction)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direction of current (Q1): Drain ⇒ Source</td>
<td>Direction of current (Q2): Source ⇒ Drain</td>
<td>Direction of current (Q2): Source ⇒ Drain</td>
</tr>
<tr>
<td>Gate-Source Voltage: Above Vth</td>
<td>Gate-Drain Voltage: Above Vth</td>
<td>Gate-Source Voltage: Above Vth</td>
</tr>
</tbody>
</table>

Q1, Q2: GaN Power Transistor

(1) **ON Operation (Forward Direction)**
High side of the GaN power transistor is turned ON, current flows in the forward direction (from the drain to the source)

(2) **OFF Operation (Like Diode)**
Even if Gate-Source is the same potential or applying a negative bias to the gate, when the Gate-Drain voltage (Vgd) is greater than the threshold voltage (Vth) by the Drain potential is lowered, current flows from the source to the drain (It is defined as the reverse conduction mode)

(*) At this time, Negative potential partial offset voltage becomes larger and conduction loss occurs (Please refer to the next page for details)

(3) **ON Operation (Reverse Direction)**
At reflux, by turning ON the transistor by applying a threshold voltage higher than the gate, it is possible to reduce heat loss. This is an effective means for reducing the conduction loss of the above (2)
2.2 On Operation (Vgs>VTH), Conduction loss

Figure 2.2-1 describes the on operation when a positive bias is applied to the gate (Figure 2.2-2).

![Graph showing voltage-current characteristics of the on operation](image)

**Figure 2.2-1  Voltage-current characteristics of the on operation (PGA26E06BA)**

Figure 2.2-1 shows the voltage-current characteristics of the on operation. Blue line shows the on-resistance Ron (=56mohm at Tc=25deg). When the enough positive bias is applied to the gate, the characteristics between the drain and the source shows as resistor for bidirectional current.

\[ \text{Ron} = \frac{dVDS}{dIDS} \]

At on operation, conduction loss is represented by the following formula.

\[ \text{conduction loss} = \text{Ron} \times \text{IDS}^2 \]
Figure 2.2-3 describes the off operation when a negative bias is applied to the gate (Figure 2.2-4).

Figure 2.2-3 Voltage-current characteristics of the off operation like diode (PGA26E06BA)

Figure 2.2-3 shows the voltage-current characteristics of the off operation. Orange line shows the characteristic at \( V_{a} = 0 \text{V} \) (Gate-Source: short circuit condition). Other colours represent the characteristics of the time that apply \(-V_{a}\). \((V_{ds} : \text{Drain-to-Source Voltage}, \; I_{ds} : \text{Drain-to-source current})\)

If negative bias \(-V_{a}\) is applied, \( V_{SD} > V_{th} + V_{a} \). \( V_{SD} (\text{@} V_{gs} = -V_{a}) = V_{SD} (\text{@} V_{gs} = 0) + V_{a} \)

At off operation, conduction loss is represented by the following formula.

\[
\text{conduction loss} = V_{SD} \times I_{sd} = (V_{SD} (\text{@} V_{gs} = 0) + V_{a}) \times I_{sd}
\]

Negative bias is an effective means for false turn-on preventive measures but the trade-off is conduction loss. Please consider negative bias value and the dead time.
## 2.2 Switching operation example of bridge circuit

- **In order to reduce the conduction loss during reflux operation, please apply voltage higher than threshold to the gate and minimize a deadtime.**

In bridge circuit with inductive load (Figure 2.2-3), when high side GaN transistor is turned off, circulated current flows via low side transistor from Source to Drain. In order to reduce the conduction loss, it is better to make low side transistor ON. Then, the below explains how to control the low side transistor.

<Notes>

1. During reflux operation, low side transistor is turned ON by applying a voltage higher than threshold to the gate.
   - It is possible to reduce conduction loss by making low side transistor ON.
   - In the case of $V_{gs} > V_{th}$ conduction loss $= (V_{sd} \times R_{on}) \times I_{sd}$
   - However, if applied gate voltage is lower than threshold, conduction loss becomes larger because of larger offset voltage($V_{SD}$). (Please refer to page of 7,9)
   - In the case of $V_{gs} = -V_a$ conduction loss $= V_{SD} \times I_{sd}$

2. Set a deadtime of which a period that high and low side transistor are turned OFF at the same time
   - To prevent high and low side transistors being turned ON at the same time, after high side transistor is turned OFF, set a deadtime. (High and low side transistor are turned OFF at the same time.) After the deadtime, control the gate voltage to be ON state.

### Switching operation example of bridge circuit

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="ON" alt="Diag1" /></td>
<td>![Diag2](OFF</td>
<td>![Diag3](OFF</td>
<td>![Diag4](ON</td>
<td>![Diag5](ON</td>
</tr>
<tr>
<td><img src="OFF" alt="Diag1" /></td>
<td><img src="ON" alt="Diag2" /></td>
<td><img src="ON" alt="Diag3" /></td>
<td><img src="OFF" alt="Diag4" /></td>
<td>![Diag5](OFF</td>
</tr>
<tr>
<td>$V_{gs} = 0V$</td>
<td>$V_{gs} = 0V$</td>
<td>$V_{gs} &gt; V_{th}$</td>
<td>$V_{gs} = 0V$</td>
<td>$V_{gs} = 0V$</td>
</tr>
</tbody>
</table>

The deadtime is needed to prevent a flow-through current. For a period, conduction loss occurs because of the Source-Drain voltage($V_{SD}$). It is recommended to check the safety operation and set a deadtime to reduce conduction loss as short as possible.
2.2 Operation Notes of the GaN Power Transistor

Usage Notes

1) During conduction period injection of dc current to gate is necessary ⇒ Note the loss due to this current
2) Low gate threshold voltage ⇒ Note that the drive circuit is designed to maintain the off-state

1) During conduction period injection of dc current to gate is necessary

Panasonic GaN Power Transistor has a PN junction diode formed between gate-source. In order to maintain the on-state, current must continuously be supplied to the diode. This gate-source diode current increases the drain current by injecting holes into the channel. Figure 2-3 shows that the gate current increases exponentially with gate voltage.

During the conduction period, gate current continues to flow, therefore loss due to this current is generated. For this reason, the gate current is desired to be set as small as possible in the above required value.

Considering both the trade-off for the gate current / on resistance characteristic in Figure 2-4, gate current about 10mA is recommended (PGA26E06BA).

Diode characteristic of VGSF = about 3.5V

![Diode characteristic graph](image)

<table>
<thead>
<tr>
<th>Gate-source voltage VGS [V]</th>
<th>Gate-source current IGS [A]</th>
<th>Drain-source on-state resistance RDSon [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0001</td>
<td>0.1</td>
<td>0.00</td>
</tr>
<tr>
<td>0.001</td>
<td>0.08</td>
<td>0.10</td>
</tr>
<tr>
<td>0.1</td>
<td>0.04</td>
<td>0.20</td>
</tr>
</tbody>
</table>

Figure 2-3 Gate voltage/current characteristics

Figure 2-4 Gate current/On resistance characteristic

2) Low Gate Threshold Voltage

Panasonic GaN Power Transistor has lower gate threshold voltage compared to Si Power MOSFET and IGBT. Hence, it does not need a high gate voltage like the case for IGBT to conduct current with low on resistance. However, noise immunity of gate voltage in off-state is small (in other words it is easy to turn on due to fluctuation in gate voltage). Therefore, care must be taken in the design of the drive circuit.

Actual use of driving gate current

- During On period when gate current flows, driving loss occurs.
- Large gate current is necessary for high speed switching at turn-on and for on-resistance reduction. For driving loss reduction, small gate current flow is necessary at On time. Hence, driving current must behave such as the above mentioned red line. (Refer to chapter 3 for more information)

![Actual use of driving gate current diagram](image)
3. Gate Drive Circuit Design

In this chapter, method of driving the GaN power transistor is described. To drive a GaN power transistor, Table 3.1 shows the parts that are required. In the following pages along with the notes in the design, 4 states of ① turn-on, ② on period, ③ turn-off, ④ off period will be described.

![GaN Power Transistor Drive Circuit Diagram]

**Table 3.1 GaN-Tr Drive circuit parts and recommended constant**

<table>
<thead>
<tr>
<th>Key components</th>
<th>Reference part (Initial value)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver IC</td>
<td>Texas Instruments UCC27511 is recommended</td>
</tr>
<tr>
<td></td>
<td>Power supply voltage of driver IC: 12V</td>
</tr>
<tr>
<td>Rgon</td>
<td>Resistance to adjust gate current (peak)</td>
</tr>
<tr>
<td></td>
<td>6.2Ω</td>
</tr>
<tr>
<td>Rig</td>
<td>Resistance that determines the steady gate current flow</td>
</tr>
<tr>
<td></td>
<td>680Ω</td>
</tr>
<tr>
<td>Cs</td>
<td>Capacitance to provide a high current at turn-on/off</td>
</tr>
<tr>
<td></td>
<td>1500pF</td>
</tr>
<tr>
<td>Rgoff</td>
<td>Resistance to adjust the turn-off speed</td>
</tr>
<tr>
<td></td>
<td>4.7Ω</td>
</tr>
<tr>
<td>Rpd</td>
<td>Pull-down resistor</td>
</tr>
<tr>
<td></td>
<td>10kΩ</td>
</tr>
</tbody>
</table>

※ Please confirm the actual waveform, please adjust the constant appropriately

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3.1 Gate Driving Method (Turn-On)

(1) We'll explain for gate voltage and gate current at turn-on

A  Gate-source voltage (Vgs) is increased through the speed-up capacitor Cs, the charge between gate and source (Cgs) is charged.

B  When Vgs rises to Vplateau, charge between gate-drain is charged and Vgs continuously rises. At this time, current between the drain-source begins to flow and the peak value Igp of the gate current Igs can be adjusted by the following formula.

\[
I_{gp} = \frac{V_{CC}}{R_{gp}} \quad [R_{gp} = 1/(1/R_{ig} + 1/R_{gon})]
\]

※Formula above is the ideal expression
※Actual Igp will be a lower value than the above-mentioned formula because it depends largely on the ability of the driver.
※To determine the final value, please check the Igp by measuring the voltage across the Rgon and please ensure that the flow of the actual gate current does not exceed the rating.

C  After Cgd is charged completely, gate voltage will be charged further until it reach VGSF.
3.1 Gate Driving Method (ON period)

(2) Gate voltage and gate current during ON period will be explained

<table>
<thead>
<tr>
<th>Section</th>
<th>Gate Voltage (Vgs), Gate Current (Igs) during turn on</th>
</tr>
</thead>
</table>
| D       | When parasitic diode (Dp) between the gate-source voltage (Vgs) reaches the VF value VGSF, steady electric current flows through Dp.  
At this time, Vgs is clamped at VGSF but actually it will behave like Vgs overshoot to the VGSF.  
During this period, since the charging on Cs is also completed, final gate current Irg is equal to the current Irg flowing into Dp through Rig.  
\[ Irg = \frac{(VCC - VGSF)}{Rig} \]  
※Please design so as not to exceed the rating of the gate current (IG) |
(3) Behaviour at turn-off can be understood as shown below.

$$V_{neg1} = -(VCC \times Cs \div (Cs+Cg) - VGSF)$$

Rgoff is the resistance to adjust the turn-off speed.
Although dV / dt at the turn-off is highly dependent on the coil current, please set a few Ω for false turn-on prevention.
3.1 Gate Drive Method (Off period)

(4) Behaviour of the off period can be understood as follows.

![Gate Voltage (Vgs), Gate Current (Igs) during turn-off](image)

<table>
<thead>
<tr>
<th>Section</th>
<th>Gate Voltage (Vgs), Gate Current (Igs) during turn-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Charge of Cs and Cg are discharged through Rgon and Rig, Vgs is close to zero volts. In this case, representation of Vgs during Toff from turn-off is given by following formula</td>
</tr>
</tbody>
</table>

\[
V_{gs}(\text{Toff}) = V_{neg1} \times \exp(-\text{Toff} / \tau) \quad \tau = (R_{gon}+R_{ig}) \times (C_s + C_g)
\]

【Important Point】
- 「When the oscillation frequency is high」、「When the on-duty is large」, charge on Cs is not discharged, next turn-on will occur.
  At that time, Vg right before turn on is represented by the following formula

\[
V_{neg2} = V_{neg1} \times \exp(-\text{Toff} / \tau) \quad \tau = (R_{gon}+R_{ig}) \times (C_s + C_g)
\]

※Toff: Off time

- If Vgs is turned on at non-zero voltage, as compared to the case of Vgs=0V, dV/dt will be reduced and loss will be increased.
- If a time constant of about five times of the Rig × Cs, next turn-on dV/dt is not affected.
### 3.2 Gate drive constant (initial value)

It is recommended that the following constant to be considered as the initial value.

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Function</th>
<th>Constant determination method</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VCC</strong></td>
<td>The power supply voltage of the driver IC It will be advantageous to the high and fast switching.</td>
<td></td>
</tr>
<tr>
<td>(Voltage Value)</td>
<td></td>
<td>【Initial setting value】 12V When using UCC27511 (made by TI) for driver IC, this setting is within the UCC27511 VCC voltage rating.</td>
</tr>
<tr>
<td>Cs</td>
<td>Speed-up capacitor that accelerates the turn-on. Charge Q must be greater than charge to the gate Qgd + Qgs. In addition, sufficient capacitance value is necessary to make gate voltage negative during turn-off.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>【Initial setting value】 1500pF ① Cs is set to meet Q(Cs)= Cs × (VCC- VGSF)&gt; Qgd+Qgs ② Cs is set to provide enough negative gate voltage value Vneg1 immediately after turn-off that does not generate false turn-on. [Recommended characteristics] 1H(50V),B(X7R),Tolerance5%</td>
</tr>
<tr>
<td>Rgon</td>
<td>Resistor that prevents excessive gate voltage during turn-on. Smaller resistance value makes switching speed higher, and it is also possible to lower the Igp by larger resistance value.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>【Initial setting value】 6.2Ω ① Igp= VCC × (1/ Rig + 1/ Rgon) Igp is set to be within the rating ※Actual Igp is lower than the value of an expression, because Igp is highly dependent on the slew rate of driver IC. ② Turn on time tr (= Qg/ Igp) , dV/ dt (= VIN(DC)/ tr) While checking the parameters, determine the Rgon. [Power rating] [Cg × VGSF^2+Cs × (VCC- VGSF)^2] × fsw/2 above [Recommended characteristics] Tolerance5% （Chip resistor is recommended）</td>
</tr>
<tr>
<td>Rig</td>
<td>During GaN-Tr ON period, the resistance which determines the injection current Igf of the gate upon steady state. Using larger resistance value, Igf can be reduced. Igf &lt; 50mA is necessary.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>【Initial setting value】 680Ω Irg = (VCC-VGSF)/Rig &gt; 10mA ※See previous page To reduce the loss, about Irg = 10mA setting is recommended [Power rating] Irg^2 × Rig × On-duty above [Recommended characteristics] Tolerance5% （Chip resistor is recommended）</td>
</tr>
<tr>
<td>Rgoff</td>
<td>Resistor that prevents excessive gate voltage during turn-off.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>【Initial setting value】 4.7Ω [Power rating] Equivalent to Rgon [Recommended characteristics] Tolerance5% （Chip resistor is recommended）</td>
</tr>
<tr>
<td>Rpd</td>
<td>Pull-down resistor that prevents the gate voltage from rising when the DC link voltage is applied to the drain during the absence of driver power supply (Few kΩ)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>【Initial setting value】 10kΩ Ileak × Rpd &lt;&lt; Vth （Ileak : leak current between the drain-gate） [Power rating] VGSF^2/R above （Chip resistor is recommended）</td>
</tr>
</tbody>
</table>
3.3 Consideration of Absolute Maximum Rating of Gate

Basic consideration of Absolute Maximum Rating of Gate
1) It should be confirmed that Gate current is within that rating. (Not Gate voltage)
2) It is accepted that Gate current is more than IG (, but less than IGP) from starting Gate current drawing to Gate to Charge of Gate reaching to QGP.

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings(Max)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Current (DC)</td>
<td>IG</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>Gate Current (pulse)</td>
<td>IGP</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>Electric Gate Charge</td>
<td>QGP</td>
<td>32</td>
<td>nC</td>
</tr>
</tbody>
</table>

* Ig of Above calculation is smaller than that real value. Strict consideration is possible by measuring Ig by the evaluation.

Figure 3.3-1. Drive circuit around Gate

**The method to confirm the rating of Gate at Circuit design**

Please design the circuit around Gate according to the following mention.

1) Setting Rig to make Ig(DC Gate current) within IG.
   \[ IG > Ig = (VCC-VGSF)/ Rig \]

2) Setting Rgon to make Igp(Pulse Gate current) within IGP
   \[ IGP > Igp = VCC/ Rgp \]
   \[ Rgp = 1/(1/Rig + 1/Rgon ) \]

3) Setting Cs to make Gate Charge by Cs & Rgon less than QGP
   \[ QGP > Cs \times (VCC-VGSF) \]

[Supplementary Note ]
- Gate voltage isn’t suitable, because Gate voltage is decided by Gate current and the characteristic of the device.
- The accurate measurement of Gate voltage might be difficult because of the noise from Drain terminal.
3.4 Drive circuits for Half bridge

The drive circuit examples for Half bridge are shown.

Please be careful of CMTI of the isolated driver.

### Normal drive circuit

- **Dr2**
  - VCCH
  - Rgoff
  - Rs
  - CG
  - N

- **Dr1**
  - VCCL
  - Rgoff
  - Rs
  - CG
  - N

[Recommendation] Dr1, Dr2: 1EDI20N12

### For 2ch Drive IC (1)

- **VCCH**
- **Rgoff**
- **Rs**
- **CG**
- **N**

[Recommendation] Dr1: Si8273, UCC27712

Doff: PMEG3002EJ

### For 2ch Drive IC (2)

- **VCCH**
- **Rgoff**
- **Rs**
- **CG**
- **N**

[Recommendation] Dr1: Si8273, UCC27712

Doff, Dclp: PMEG3002EJ

### Driving waveforms

- **Gate current (Ig)**
- **On period**
- **Off period**
- **Gate voltage (Vgs)**

**Parts value can be decided according to P17.**

**Negative voltage can support the stable operation.**

- **Small negative voltage reduce the dead time loss**

---

**Semiconductor Business Unit, Panasonic Semiconductor Solutions Co., Ltd**
4. Switching characteristics evaluation and application

In this chapter, using the following evaluation board equipped with a drive circuit described in Chapter 3, switching characteristic when driving constants (Rgon, Rgoff, Rig, Cs) change is described. Depending on the application, please use as a reference to determine the optimum drive constants.

<table>
<thead>
<tr>
<th>Single-Switch boost converter circuit</th>
<th>Bridge circuit (High side regeneration)</th>
<th>Bridge circuit (Low side regeneration)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Single-Switch boost converter circuit" /></td>
<td><img src="image2.png" alt="Bridge circuit (High side regeneration)" /></td>
<td><img src="image3.png" alt="Bridge circuit (Low side regeneration)" /></td>
</tr>
</tbody>
</table>

- High side: SBD
- Low side: GaN Power transistor

- High side: GaN Power transistor
- Low side: GaN Power transistor

See page 18–23.
See page 24–25.
See page 26–27.
4.1 Hard switching evaluation (low-side switch circuit)

In order to understand the switching characteristics of the GaN power transistor in Single-Switch boost converter, an evaluation circuit on Figure 4.1-1 is used, and a double-pulse evaluation is described as an example.

As described in chapter 3, the driving circuit of the GaN Power Transistor has different characteristics from the conventional Si-MOSFET driver circuits. Under the condition of 100kHz, duty50%, drive constant of Table 4.1-1 is recommended, assuming that high-speed switching and stable operation can be achieved.

When the circuit in Figure 4.1-1 is mounted with the constants shown on Table 4.1-1, Figure 4.1-2 shows the turn-on waveform while Figure 4.1-3 shows the turn-off time waveform.

\[ \text{dV/dt of Vds during turn-on is } 145V/\text{ns in Fig 4.1-2, } 32V/\text{ns}(10\%-90\%) \text{ during turn-off, it can be driven at a high speed as compared with the conventional Si-based power semiconductor. Comparing GaN Power transistor with the Si-based transistor, very small Qgs and Qgd switching operation in a short period of time is possible, loss can be greatly reduced with GaN power transistor.}\]

In addition, Turn-on dV / dt can be controlled by changing the Rgon value.

For transistors using a depletion type GaN device which has realized the normally-off by controlling the MOS transistor connected in series, switching speed and EMI measures are difficult to adjust to suit the application. However, for Enhancement type GaN power transistor that achieves normally-off, there is a high flexibility in the switching speed control.

In subsequent article, function of each of the parts will be explained by changing the parameters of the recommended circuit.
4.1 Hard switching evaluation (low-side switch circuit) (Rgon)

- Rgon affects the turn-on dV / dt
- The turn-off dV / dt is not affected

*Actual relationship of dV/dt (10%～90%) and Rgon when Rgon is varied are shown in Figure 4.1-4 and Figure 4.1-5.*

From Figure 4.1-4, change of Rgon affects the turn-on dV / dt, it is not nearly dependent on the coil current. In addition, from Figure 4.1-5, the turn-off dV / dt is not affected.
The following sections describe the relationship of the dV/dt and Rgoff when Rgoff is changed.

Turn-off dV/dt of Vds is highly dependent on the coil current amount. In addition, it also depends on Rgoff. However, it is almost independent of Rgon.

Increase of Rgoff will lead to increased impedance between the gate to a low level potential at the time of turn-off. There is a risk concern of shoot-through current. Therefore, setting in the order of several Ω is recommended.

In addition, Rgoff does not depend to dV/dt of Vds at turn-on.

The relationship between the turn-on and turn-off dV/dt with Rgoff is shown in Figure 4.1-6 and Figure 4.1-7.

※ dV/dt is derived from 10%-90% of the rise and fall
The following describes the relationship between the $dV/dt$ and Cs when changing the Cs.

For Cs, it does not particularly affect the driving characteristics as long as it meets the $Q_g ((V_{drv}-V_{GSF}) \times Cs)$ on the drive circuit. In actual, a false turn-on symptom might occur after turn-off. Changing the Cs to a larger value can increase the negative bias on the gate-source voltage and prevent shoot-through current.

However, if Cs is too big, drive loss increases and Cs discharge time becomes longer during the OFF period. On the other hand, if it is too small, the switching loss will increase because $dV/dt$ of $V_{ds}$ is reduced.

- **Cs does not affect the turn-off $dV/dt$ if it meets the $Q_g ((V_{drv}-V_{GSF}) \times Cs)$**

![Figure 4.1-8](image1)  
**Figure 4.1-8** Relationship between the turn-on of the $dV/dt$ and Cs

![Figure 4.1-9](image2)  
**Figure 4.1-9** Relationship of the turn-off time of $dV/dt$ and Cs

※ $dV/dt$ is derived from 10%-90% of the rise and fall
4.1 Hard switching evaluation (low-side switch circuit) (Rig)

- Since Rig is a resistance that determines the gate current (Ig), it does not directly affect the turn-on and turn-off dV/dt.
- Since the parameters depend on Cs discharge, the turn-on dV/dt will be affected if Cs is not completely discharged during off period.

The following sections describe the relationship of the dV / dt and Rig with changing Rig.

For Rig, gate current (Ig) of more than 10mA is recommended. If Ig is not set to more than 10mA, you will not be able to get a sufficiently low on-resistance at high temperature.

Since Rig is a parameter affecting the discharge time of Cs, the turn-on dV/dt may reduce if Rig is high. Based on Figure 4.1-10, for the condition of Rig=2200Ω, result shows reduced turn-on dV/dt because Cs is not completely discharged at the next turn-on. This is because the discharge path time constant is 3.3us within the 5us off-time.

Figure 4.1-10 Relationship of dV / dt and Rig at turn-on

Figure 4.1-11 Relationship of dV / dt and Rig at turn-off

※ dV/dt is derived from 10%-90% of the rise and fall
4.1 Hard switching evaluation (low-side switch circuit) (off-time of the Notes)

- The shorter the off period, the harder for Cs to be completely discharged and hence more likely to cause turn-on dV/dt reduction.

Then, Figure 4.1-12 shows the effect of changing off time towards dV/dt of Vds at turn-on time with recommended drive circuit.

< When off time is short >

From the result of Figure 4.1-12, when the turn-off time is short, there is a tendency that the dV / dt is reduced.

For high frequency drive, in case dV/dt is a problem in the short off time, it is possible to adjust the switching speed by reducing the value of Cs or Rig.

However, negative bias at turn-off is reduced when Cs is reduced. In addition, drive loss will increase when Rig is reduced. In order to fit the application specifications, please adjust the optimum constant.

![Figure 4.1-12  dV / dt at the time of changing the OFF time](image)

※ dV/dt is derived from 10%-90% of the rise and fall
4.2 Hard switching evaluation Bridge circuit (High side regeneration)

In order to understand the switching characteristics of the GaN power transistor in Bridge circuit (High side regeneration), an evaluation circuit on Figure 4.2-2, 4.2-3 is used, and a double-pulse evaluation is described as an example.

High and low side GaN Power Transistor are arranged in Figure 4.2-2. Drive circuit is shown in Figure 4.2-3. This sections describe the relationship of the low side transistor’s dV/dt and driving constants when driving constants is changed. Dead time is set 450ns, because of stable operation. Recommended drive constant is shown on Table 4.2-1. Waveform image of input signal for high and low side transistor are shown in Figure 4.2-1.

In order to optimize the high-speed switching features and ensure stable operation of the GaN power transistor, an isolator having specification item (Common Mode Transient immunity) about 100kV/μs is used. In this chapter, using the evaluation board equipped with a shortest drive circuit like low side switching circuit.

![Figure 4.2-1 Drive signal for bridge circuit (High side regeneration)](image)

![Figure 4.2-2 The operation of bridge circuit (High side regeneration)](image)

![Table 4.2-1 Reference Value](image)

<table>
<thead>
<tr>
<th>Part name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rig</td>
<td>680Ω</td>
</tr>
<tr>
<td>Cs</td>
<td>1500pF</td>
</tr>
<tr>
<td>Rgon</td>
<td>6.2Ω</td>
</tr>
<tr>
<td>Rgoff</td>
<td>4.7Ω</td>
</tr>
<tr>
<td>Rpd</td>
<td>10kΩ</td>
</tr>
</tbody>
</table>

![Part name Value](image)

<table>
<thead>
<tr>
<th>Part</th>
<th>name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rig</td>
<td>H</td>
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</tr>
<tr>
<td>Cs</td>
<td>H</td>
<td>1500pF</td>
</tr>
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![Part name Value](image)

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<th>Part</th>
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<tr>
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</tr>
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<td>Rpd</td>
<td>L</td>
<td>10kΩ</td>
</tr>
</tbody>
</table>

![Part name Value](image)
4.2 Hard switching evaluation Bridge circuit (High side regeneration)

- Like low side switch circuit, Rgon affects the turn-on dV / dt
- The turn-off dV / dt is not affected

*Actual relationship of dV/dt(10%～90%) and Rgon when Rgon is varied are shown in Figure 4.2-4 and Figure 4.2-5.

![Figure 4.2-4 Relationship of dV / dt and Rgon at turn-on time](image1)

![Figure 4.2-5 Relationship of dV / dt and Rgon at the turn-off time](image2)

From Figure 4.2-4, change of Rgon affects the turn-on dV / dt, it is not nearly dependent on the coil current.
In addition, from Figure 4.2-5, the turn-off dV / dt is not affected like low side switch circuit.

【About other value】: Other value(Rgoff,Rig,Cs) tend to change like low side switch circuit. For details, please see chapter 4.1.

- **Rgoff**: Rgoff affects the turn off dV/dt (Dependency of coil current is large)
- **Rig**: Since Rig is a resistance that determines the gate current, it does not directly affect the turn-on and turn-off dV/dt.
  - If Rig is extremely high, Rig is affected the discharge time of Cs.
- **Cs**: Cs does not affect the turn-off dV / dt if it meets the Qg (<(Vdrv-VGSF) × Cs)
4.3 Hard switching evaluation Bridge circuit (Low side regeneration)

In order to understand the switching characteristics of the GaN power transistor in Bridge circuit (Low side regeneration), an evaluation circuit on Figure 4.3-2, 4.3-3 is used, and a double-pulse evaluation is described as an example.

High and low side GaN Power Transistor are arranged in Figure 4.2-2. Drive circuit is shown in Figure 4.3-3. This sections describe the relationship of the high side transistor’s dV/dt and driving constants when driving constants is changed. Dead time is set 450ns, because of stable operation. Recommended drive constant is shown on Table 4.3-1. Waveform image of input signal for high and low side transistor are shown in Figure 4.3-1.

In order to optimize the high-speed switching features and ensure stable operation of the GaN power transistor, an isolator having specification item (Common Mode Transient immunity) about 100kV/μs is used. In this chapter, using the evaluation board equipped with a shortest drive circuit like low side switching circuit.

Table 4.3-1 Reference Value

<table>
<thead>
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</tr>
<tr>
<td>Rgon</td>
<td>6.2Ω</td>
</tr>
<tr>
<td>Rgoff</td>
<td>4.7Ω</td>
</tr>
<tr>
<td>Rpd</td>
<td>10kΩ</td>
</tr>
</tbody>
</table>

Figure 4.3-2 The operation of bridge circuit (Low side regeneration)
4.3 Hard switching evaluation Bridge circuit (Low side regeneration)

- Like low side switch circuit, $R_{gon}$ affects the turn-on $dV/dt$
- The turn-off $dV/dt$ is not affected

*Actual relationship of $dV/dt(10\%\sim90\%)$ and $R_{gon}$ when $R_{gon}$ is varied are shown in Figure 4.3-4 and Figure 4.3-5.

![Figure 4.3-4](image1.png)  
**Figure 4.3-4** Relationship of $dV/dt$ and $R_{gon}$ at turn-on time

![Figure 4.3-5](image2.png)  
**Figure 4.3-5** Relationship of $dV/dt$ and $R_{gon}$ at the turn-off time

From Figure 4.3-4, change of $R_{gon}$ affects the turn-on $dV/dt$, it is not nearly dependent on the coil current.
In addition, from Figure 4.3-5, the turn-off $dV/dt$ is not affected like low side switch circuit.

**About other value:** Other value($R_{goff}, R_{ig}, C_s$) tend to change like low side switch circuit. For details, please see chapter 4.1.

- $R_{goff}$: $R_{goff}$ affects the turn off $dV/dt$ (Dependency of coil current is large)
- $R_{ig}$: Since $R_{ig}$ is a resistance that determines the gate current, it does not directly affect the turn-on and turn-off $dV/dt$.
  - If $R_{ig}$ is extremely high, $R_{ig}$ is affected the discharge time of $C_s$.
- $C_s$: $C_s$ does not affect the turn-off $dV/dt$ if it meets the $Q_{g}(<(V_{drv}-V_{GSF}) \times C_s)$
5. Printed circuit board design

In this chapter, a design example will be used to illustrate the board pattern design

In order to optimize the high-speed switching features and ensure stable operation of the GaN power transistor, pattern design of the drive circuit and its vicinity is very important.

Notes on pattern design are summarized in the table below. It is advisable to refer to the detailed design example and layout diagram on following pages to achieve high dV/dt and achieve low switching loss, which is a feature of the GaN power transistor, and also to avoid unstable operation.

<table>
<thead>
<tr>
<th></th>
<th>Notes on pattern design</th>
</tr>
</thead>
</table>
| 1 | Please ensure wiring of the power loop※1 as short as possible  
   ※1 For the power loop, refer to page 32 |
| 2 | Please ensure gate loop※2 wiring as short as possible  
   Please keep to minimum loop area  
   ※2 Driver output ⇒ GaN(gate terminal) ⇒ GaN(source1 terminal) ⇒ Driver GND |
| 3 | Please design wiring in (2) above to be as thick as possible |
| 4 | Please keep a distance between gate drive circuit and the pattern whose voltage dynamically changes. |
5.1 Printed Circuit Board Design and Operation Notes

- In order to realize high-speed switching, parasitic inductance of the printed circuit board should be minimized.
- Since layout and wiring are important, please take note of following points in board design.

(1) Shortest power loop and minimum loop area should be designed in order to reduce the parasitic inductance (Lp) of the printed circuit board.

- It can suppress surge voltage at turn-off.
- It can achieve high switching speed, and reduce switching loss.
- Ringing loss during switching will be reduced.

Fig. 5.1-1 Power circuit block diagram

- Please place GaN-Tr, SBD and the capacitor nearest to each other, and design shortest power loop.
5.1 Printed Circuit Board Design and Operation Notes

(2) Minimum loop area of driver output terminal ⇒ gate terminal (GaN) ⇒ source1 terminal (GaN) ⇒ driver GND terminal
Please place the gate circuit parts like that. In addition, they should be connected by thick wiring lines as much as possible.

- With high speed rise of the driver output voltage, high switching dV/dt will be achieved.
- Gate voltage rising and Self turn on by Gate loop oscillation are prevented from.

![Gate drive circuit diagram](image)

Minimize parasitic inductance
Minimize gate loop

Fig. 5.1-2 Gate drive circuit diagram

![Gate drive circuit layout example](image)

GND line is located at opposite side.

Fig. 5.1-3 Gate drive circuit layout example

(4) Please keep a distance between gate drive circuit and the pattern whose voltage dynamically changes.

- Gate voltage rising and Self turn on by Gate loop oscillation are prevented from.

![Gate drive circuit diagram](image)

① Drive circuit of low side isn’t closed to GND line of high side.
② Drive circuit of high side isn’t closed to GND line of low side and Drain live of high side.

* Especially, be careful of ②, please.

In case of 4 layers PCB, we’d like to suggest to put the GND pattern of high side at 2nd layer under drive circuit of high side in order to make the voltage of high side drive circuit stable, when the drive circuit of high side is located at 1st layer and GND line of low side is located at 4th layer at that opposite side.
【Notes】
- Shortest and thick gate loop wiring is designed
- Shortest loop of red line is designed

Bottom side

Top side

Distance is kept between gate drive circuit and GND line of low side/ Drain pattern of high side.

Shortest and thick gate loop wiring should be designed.
5.2 Thermal design (Reference pattern example: Thermal resistance = 3.4[K/W])

- Heat dissipation for surface mount components is mainly through PCB patterns. Therefore, pattern design has great significance towards heat dissipation characteristics.
- For heat dissipation consideration, it is recommended following PCB pattern of GaN-HFET (SMD Package)
  ① Number of layers: 2 layers ② Thermal vias area: 3.2mm × 12mm ③ Cu pattern area: 12mm□

PCB pattern design

Thermal vias:
- 0.3Φ / 0.6mm pitch / Cu thickness 20um

※ Drive circuit pattern is placed around Gate, Source1

SMD GaN footprint

<Bottom View>

【PCB pattern heat dissipation characteristics】
- Thermal resistance reduction is possible with Cu pattern area increase. If needed to place thermal vias, take note about the saturation trend in the long side 12mm□ or more.
- There is no significant difference in heat dissipation characteristics between a 2-layer board with 4-layer board. Difference is only 0.1~0.3K/W.

【Reference pattern example】
Based on the above heat dissipation characteristics, below patterns are selected, in considerations of cost (2 layer < 4 layer) and its impact to the surrounding patterns
  ① Number of layers: 2 layers ② Thermal vias area: 3.2mm × 12mm ③ Cu pattern area: 12mm□

For this example, the thermal resistance from PCB backside up to the junction will be 3.4[K/W].

Described here is one example of pattern, which does not guarantee reliability. Evaluation of actual environment on your side is appreciated.
5.2 Thermal design (Reference pattern example: Thermal resistance = 3.4[K/W])

**Reference: PCB pattern design**

1. **Number of layers:** 2 layers
2. **Thermal vias area:** 3.2mm × 12mm
3. **Cu pattern area:** 12mm

※Drive circuit pattern is placed around Gate, Source1

---

**<Specification of board>**
- **Board material:** FR-4
- **Number of layers:** 2 layers
- **Thickness of the Cu foil:** 70um

**<Details to thermal via>**
- **Arrangement number of thermal via:** 5 × 20 = 100
- **Pitch:** 0.6mm (the distance between centers)
- **Diameter:** 0.3Φ
- **Cu thickness:** 20um

---

Panasonic
5.3 Recommended footprints

- Shown are the IC land, printed circuit board and metal mask opening patterns

<table>
<thead>
<tr>
<th>IC land pattern</th>
<th>Printed circuit board pattern</th>
<th>Metal mask opening pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
<td><img src="image3" alt="Diagram" /></td>
</tr>
</tbody>
</table>

**Reference dimensions of the terminal**

<table>
<thead>
<tr>
<th>Terminal pitch</th>
<th>IC land</th>
<th>Printed circuit board land</th>
<th>Metal mask opening</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width Wp</td>
<td>Length Lp</td>
<td>Width W</td>
<td>Total length L</td>
</tr>
<tr>
<td>2.00</td>
<td>1.00</td>
<td>0.50</td>
<td>1.30</td>
</tr>
</tbody>
</table>

Unit: mm
5.3 Recommended footprints

The resist and metal mask specification is shown in below reference example.

Reference dimensions of the heat sink

For the relationship between the heat radiating portion land size and the metal mask openings, we recommend that you design according to the area ratio shown in the following equation.

\[
\frac{\text{Heat sink area of metal mask opening}}{\text{Heat sink area of printed circuit board}} \approx 40\%
\]

<table>
<thead>
<tr>
<th>IC land/printed circuit board pattern</th>
<th>Metal mask opening pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width (W) × Length (L)</td>
<td>Width (W_m) × Length (L_m)</td>
</tr>
<tr>
<td>Same dimension as the heat sink exposure dimension in package standard diagram</td>
<td>1.0～1.5 mm ((\text{The variable is also a square in a circle}))</td>
</tr>
</tbody>
</table>

Resist specification:
Board footprint size + 0.10mm (Each side + 0.05mm)

Metal mask thickness:
0.13mm
5.3 Recommended footprints

Implementation notes

- The Cu land pattern should be same shape as the die pad design exposed at the center of IC products, and recommended to make a metal mask opening size smaller than the Cu land pattern. If the mask opening is larger than Cu land pattern, the solder on resist will float, and there is a risk of the defect of a capillary ball and a solder bridge.

- Metal mask specifications previously described that the opening dimension is 1.00 ~1.50mm and the slit space is about 0.50~1.00mm. This is for the suppression of void caused by gas generated from the flux or the substrate. Since it is difficult to completely control a void, please also consider to approach from the material surface such as a void reduction solder paste.

- Dimensions shown on the figure above do not guarantee the mounting reliability. Please kindly verify based on actual mounting conditions and the environment.
Safety precautions

Danger
• Please always read the product specifications and application notes in order to use this product safely.
  • When dealing with high voltage, please ensure that the product will not be handled in an environment where you can touch the product.
    There is a risk of electric shock, burnout.

Warning
• Please use the product within its rating (voltage, current, temperature).
  There is a risk of burnout, explosion.
• During device evaluation, please ensure to ground the ground terminal of the system.
  There is a risk of electric shock.
• Please do not modify or further process the device.
  There is a risk of burnout, explosion.

Note
• The product should not be used near water, corrosive gas or combustible material.
  There is a risk of electric shock, fire.
• When dealing with high voltage, please implement safety measures such as protective cover in order to prevent unintentional contacts with the product and other components.
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(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. We do not guarantee quality for disassembled products or the product re-mounted after removing from the mounting board. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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