## Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

# Panasonic
# Driver LSI for Stepping Motor
# **AN44180A Application Note**

## ■ Contents

# 1.Description / Features / Package

## ■Description

AN44180A is a 2-channel H-bridge driver LSI and can control Bipolar stepping motor.
It is possible to drive by 2-phase, half step,1-2 phase, W1-2 phase excitation systems.

## ■Features

- Absolute maximum voltage / current : 37V / 1.5A
- Operating power voltage : 8 to 34V
- Built-in protection functions:
  Under-voltage lockout, over-current protection, thermal protection
- Support parallel drive method:
  2 phase, half step, 1-2 phase, W1-2 phase excitation enabled
- Support current decrement method by Mix Decay
- PWM can be driven by internal oscillator
  (3-value can be selected during PWM OFF period.):
  The selection of PWM OFF interval enables the best PWM drive.
- Built-in EMI reduction circuit
- Lower power consumption by internal standby function

## ■Applications

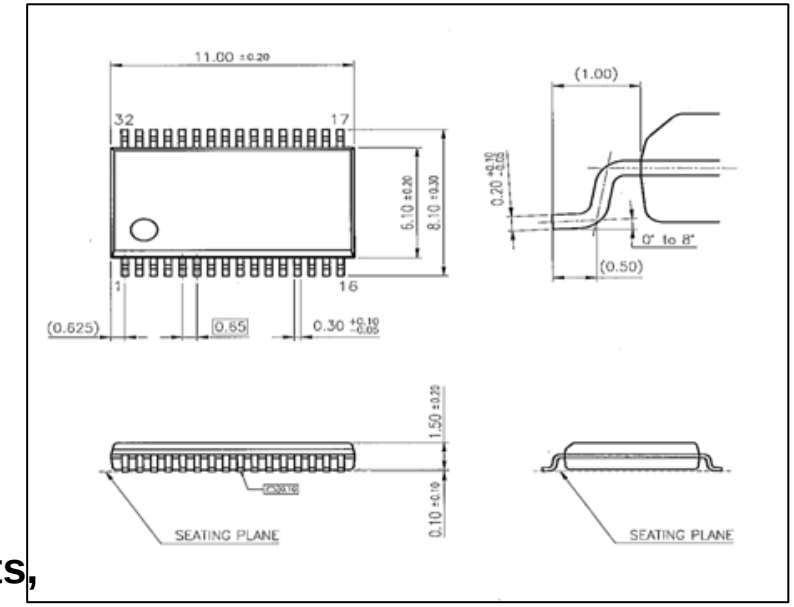
- Printer, Copier, Facsimile, FA, Security camera, Robots, Medical equipment, ATM, Home appliances, etc.

## ■Package

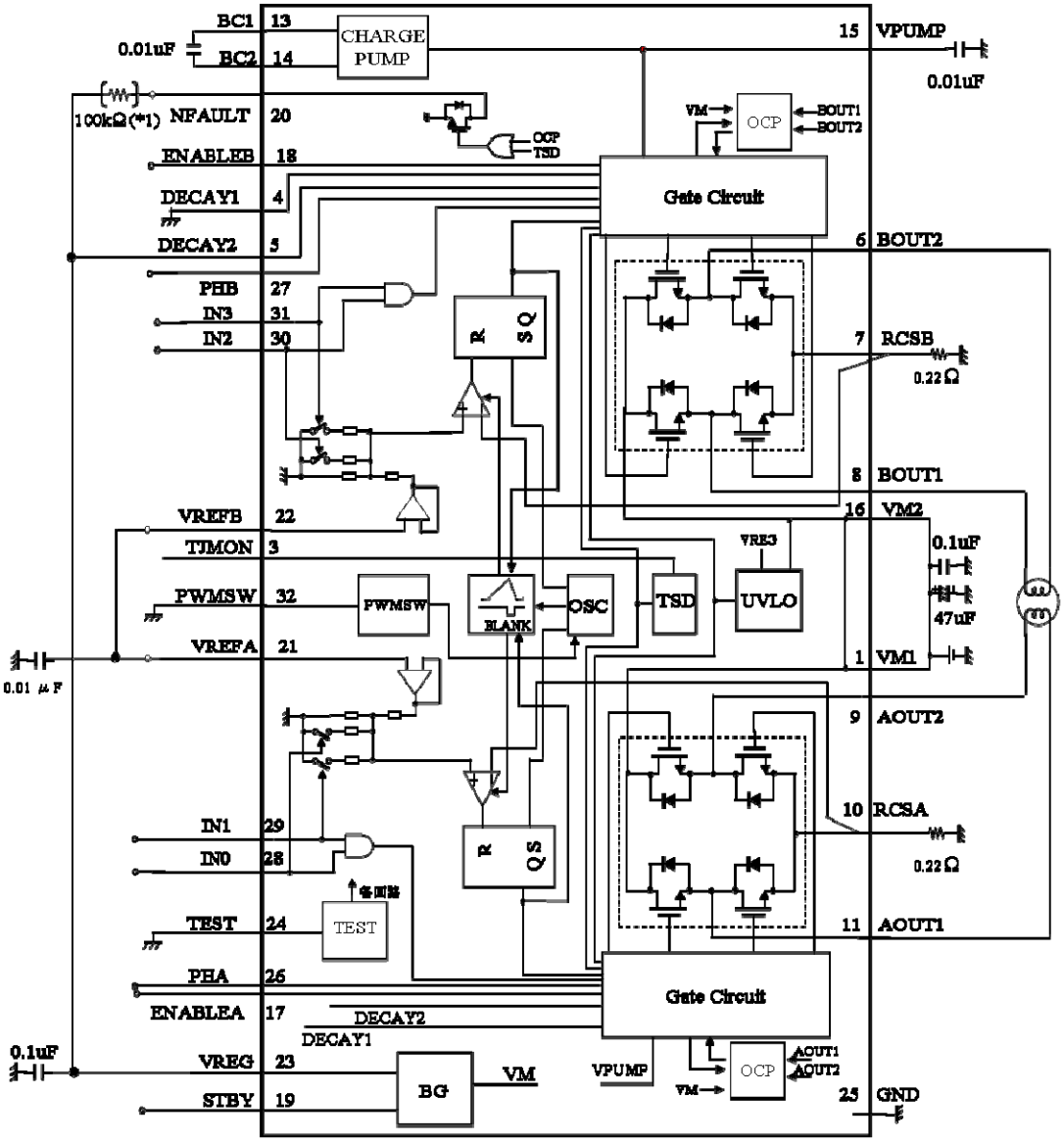
- 32pin Plastic Shrink Small Outline Package (SSOP Type)

**Fig: 32 Pin Small Outline Package**

**SSOP032-P-0300D**



# 2. Functional Block Diagram




Note) This application circuit is an example. The operation of mass production set is not guaranteed. To explain the function, block diagram is simplified and omitted.

• STBY pin cannot be set to “H” when it is connected to VREG with resistor. Therefore, set an external signal, if you want to set STBY pin to “H”.

* Connect GND to TEST terminal.

* When ENABLE, RESET, DIR, ST1-3 and TEST are used with “H” or ” L”, connect to “H” (connected to VREG or external signal) or “L” (connected to GND), respectively.

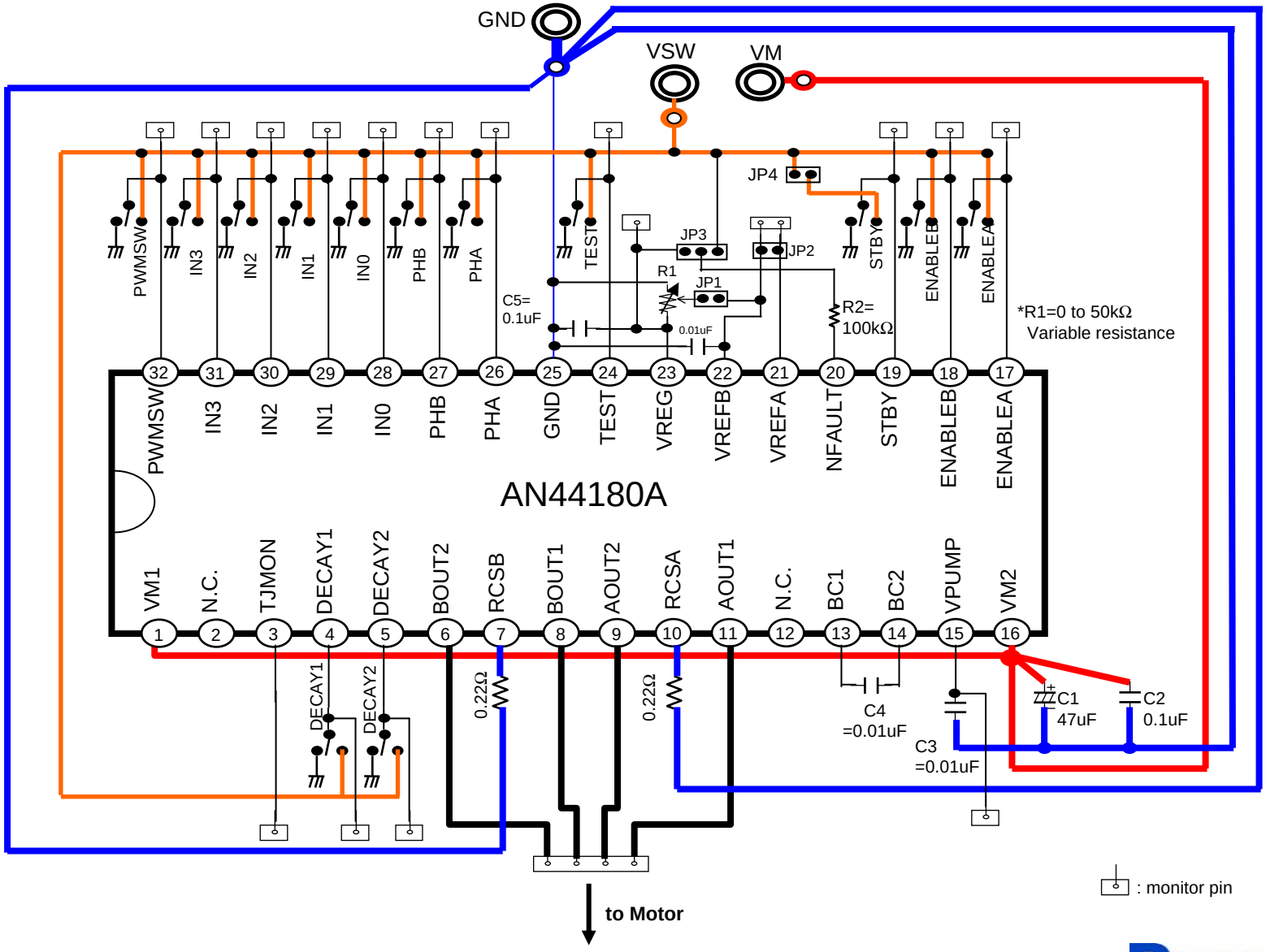
* DECAY1, DECAY2 and PWMSW are not interface input pins. If you want to set to “H” or “L”, connect to VREG or GND respectively.

* PWMSW can be set to “M“ by setting PWMSW to Open. However, it might occur the error of operation due to the noise. In this case, connect the capacitor of 0.01μF or more between PWMSW and GND .

* It is recommended that N.C. terminal be connected to GND.

*1 : Only when FAULT pin is used, connect it to VREG with resistor. Recommended that it should be left open when not used.

# 3. Recommended Application Circuit



# 4-1. Control Mode Chart

## ■STBY( Control / Voltage up circuit )

| STBY | ENABLEA | ENABLEB | Control / Voltage up circuit | Ach-Output transistor | Bch-Output transistor |
|---|---|---|---|---|---|
| "L" | - | - | OFF | OFF | OFF |
| "H" | "L" | "H" | ON | OFF | ON |
| “H" | "H" | "L" | ON | ON | OFF |
| "H" | "H" | "H" | ON | ON | ON |

Note) Input external signals to STBY pin in order to set STBY signal to High-level. Because, STBY pin cannot be set to High-level when it is connected to VREG.
Note) Low : 0V to 0.8V , High : 2.1V to 5.5V

## ■Output Polarity for PHA/PHB

| PHA/PHB | AOUT1/BOUT1 | AOUT2/BOUT2 |
|---|---|---|
| "H" | "H" | "L" |
| "L" | "L" | "H" |

Note) “L” : 0V to 0.8V , “H” : 2.1V to 5.5V

## ■Output Current for IN* Signal

| IN0/IN2 | IN1/IN3 | Output current |
|---|---|---|
| "L" | "L" | (VREF / 10) × (1 / Rs) × 100% = $I_{OUT}$ |
| "H" | "L" | (VREF / 10) × (1 / Rs) × 70.7% = $I_{OUT}$ |
| "L" | "H" | (VREF / 10) × (1 / Rs) × 38.4% = $I_{OUT}$ |
| "H" | "H" | 0 |

Note) Rs : current detection resistance
Note) IN0 = IN1 = “H” / IN2 = IN3 = High, all outputs transistors turn off.
Note) "L" : 0V to 0.8V 、"H“ : 2.1V to 5.5V

## ■PWM OFF Period Selection

| PWMSW | PWM OFF period selection |
|---|---|
| "L" | 28.0 µsec |
| "M“ or OPEN | 8.1 µsec |
| "H" | 15.2 µsec |

Note) “L”: → 0V to 0.6V, “M”: → 1.2V to 1.7V , “H”: → 2.3V to 5.5V
Note) PWMSW can be set to “M“ by setting PWMSW to Open.
However, it might occur the error of operation due to the noise.
In case, connect the capacitor of 0.01µ F or more between PWMSW and GND .

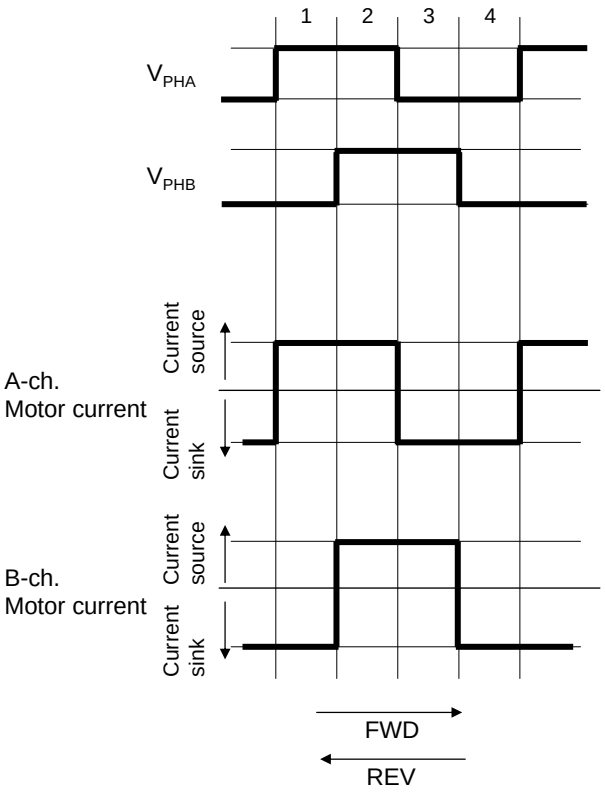
## ■Decay Control

| DECAY1 | DECAY2 | Decay control |
|---|---|---|
| "L" | "L" | Slow Decay |
| "L" | "H" | 25% |
| "H" | "L" | 50% |
| "H" | "H" | 100% |

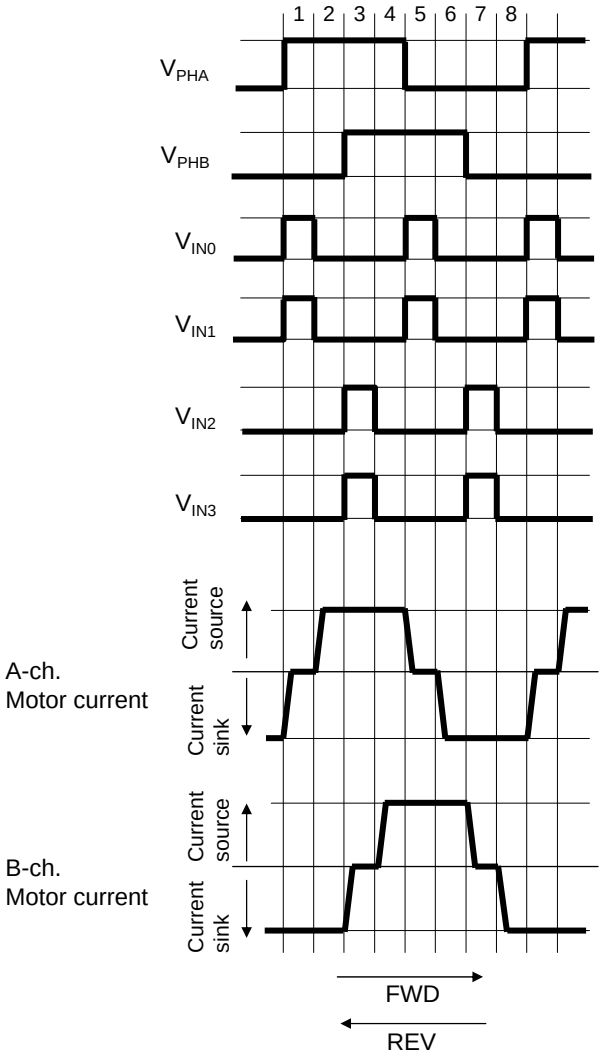
Note) The above rate is applied to Fast Decay every PWM OFF period.
Note) "L": → 0V to 0.8V , "H": → 2.1V to 5.5V
Note) DECAY1 and DECAY2 can be set to “L” by setting DECAY1 and DECAY2 to Open.
However, it might change to High setting due to the noise. In case, DECAY1 pin and DECAY2 pin is shorted to GND.

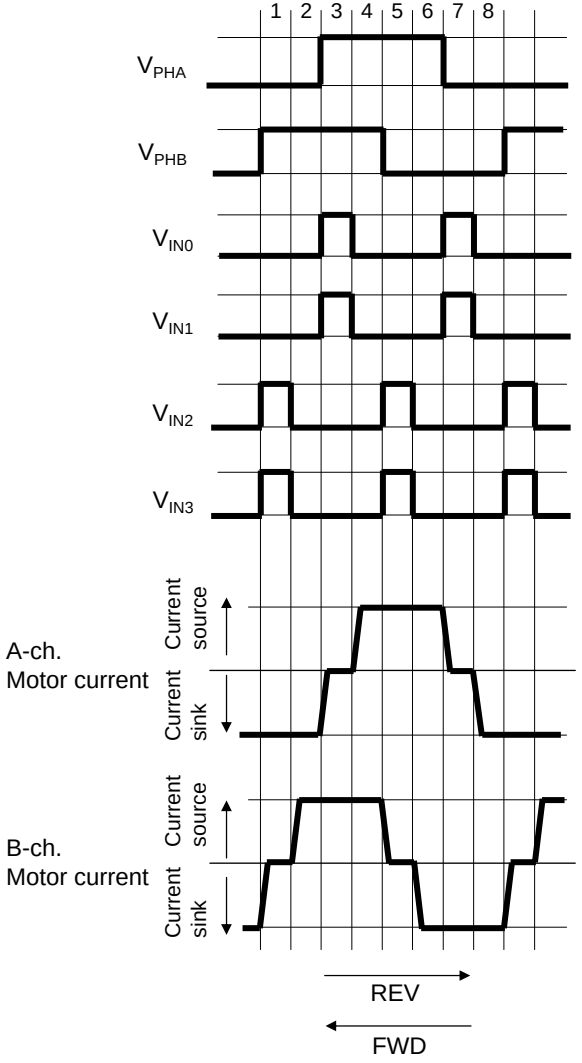
# 4-2. Timing Chart No.1

## 2 phase excitation

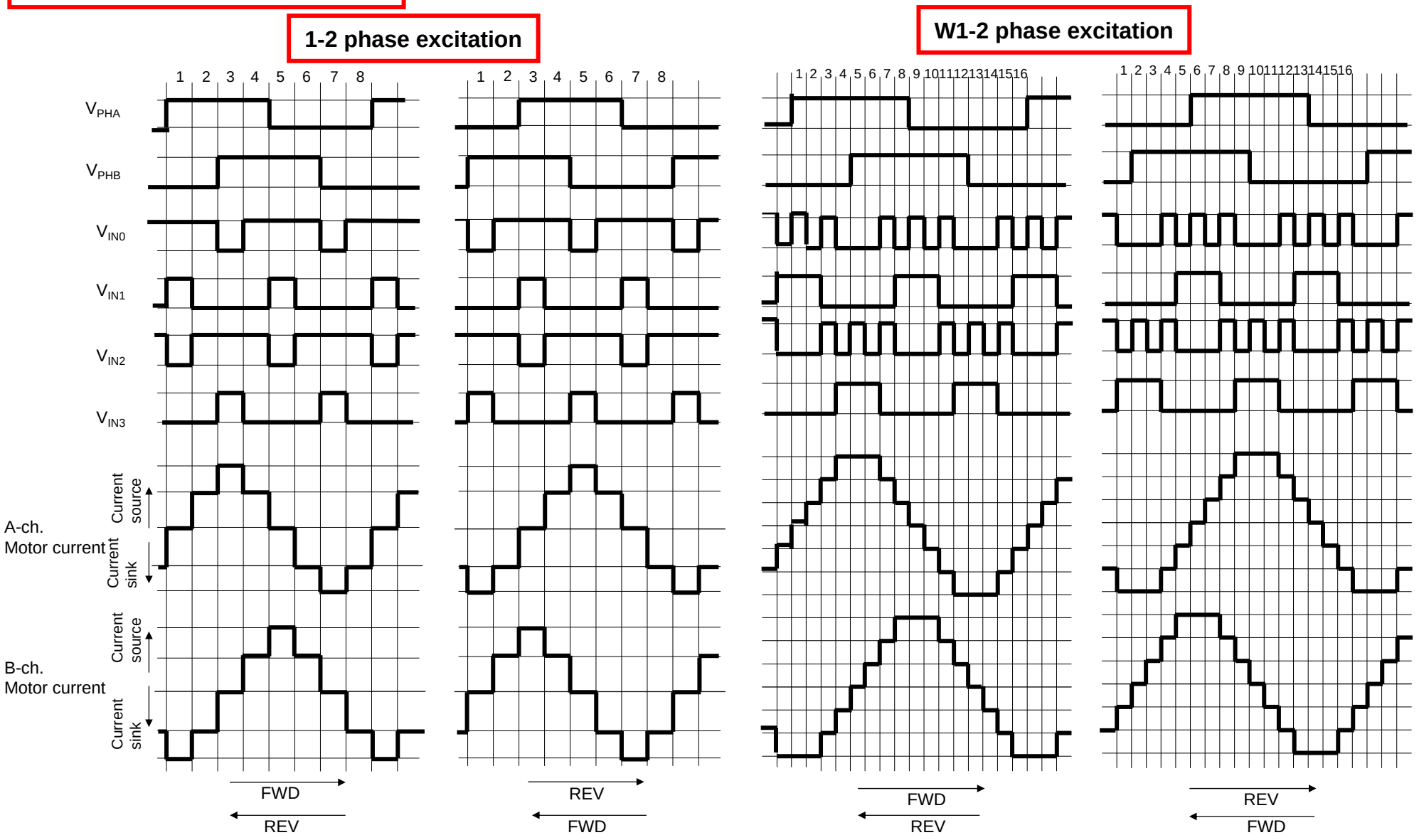



## Half step



# 4-3. Timing Chart No.2



# 4-4. Timing Chart No.3 (VREF Control)

- This LSI can output each excitation pattern by inputting VREFA,VREFB,PHA1,PHB1 and IN0 to IN3. Specifically, it is shown as follows. The motor current changes depending on a change of VREF. The sinusoidal motor current can be output by changing VREF sinusoidally.

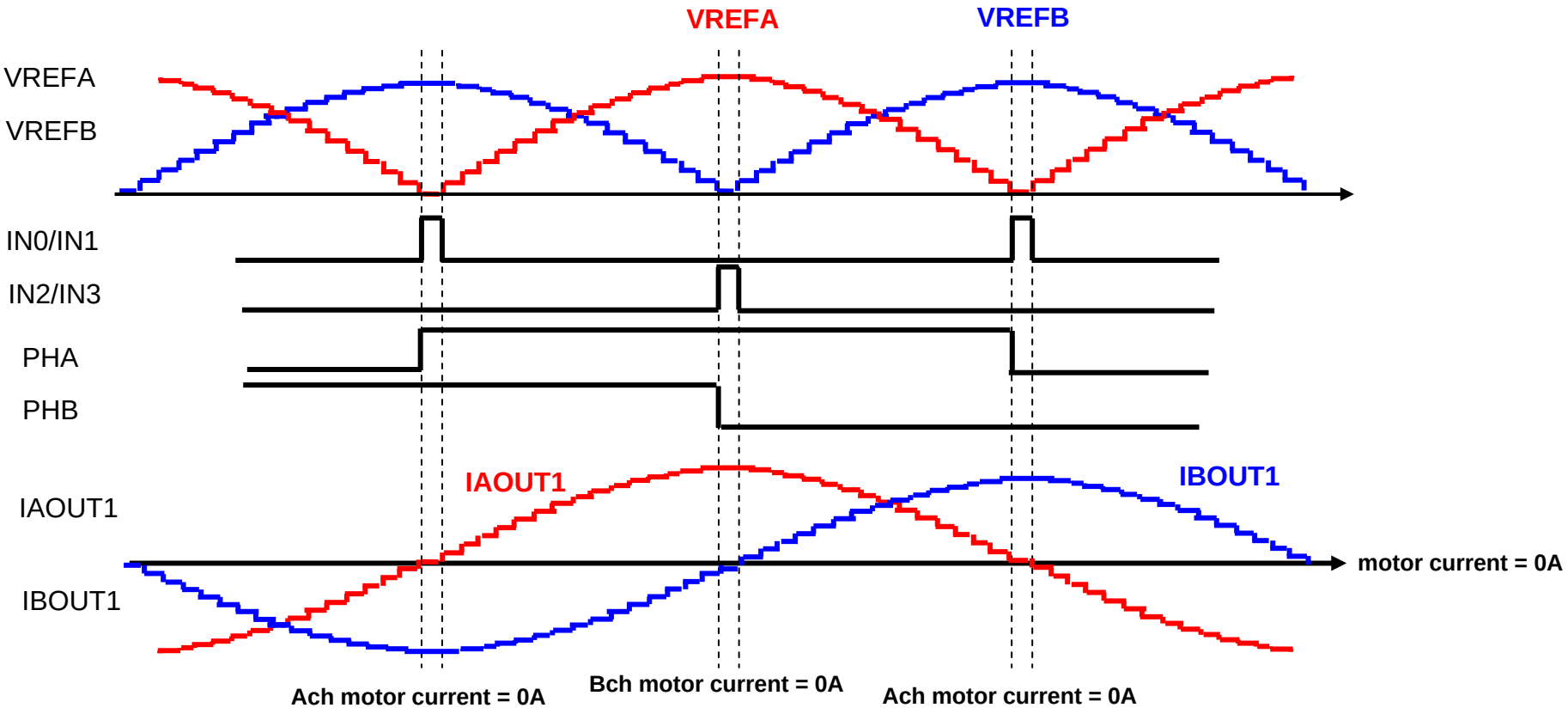



**Fig: Motor Current Timing Chart**

# 4-5. Input/Output Block Circuits

VREG (Pin23)

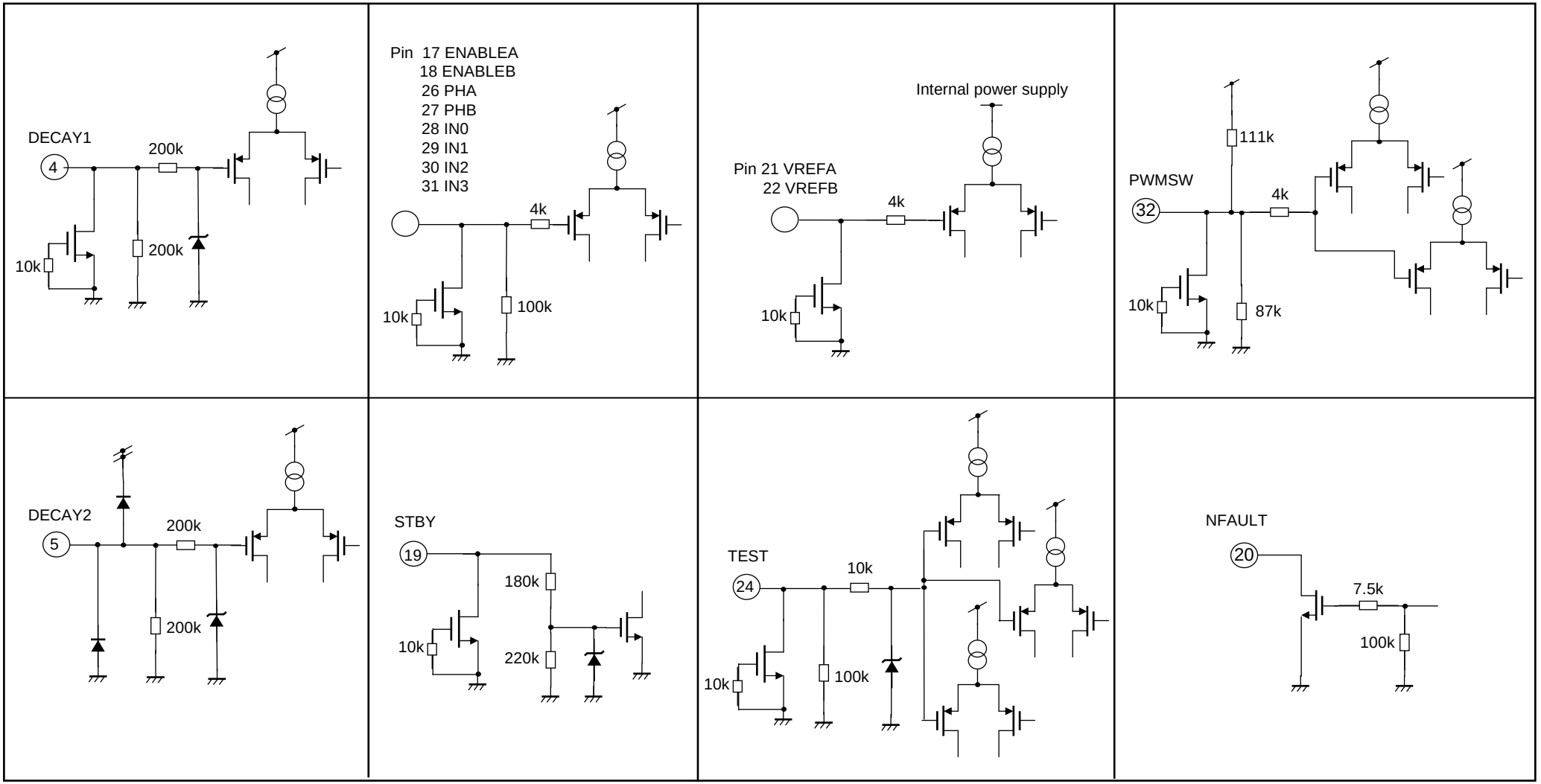
VM1(Pin1), VM2(Pin16)

Diode

Zener diode

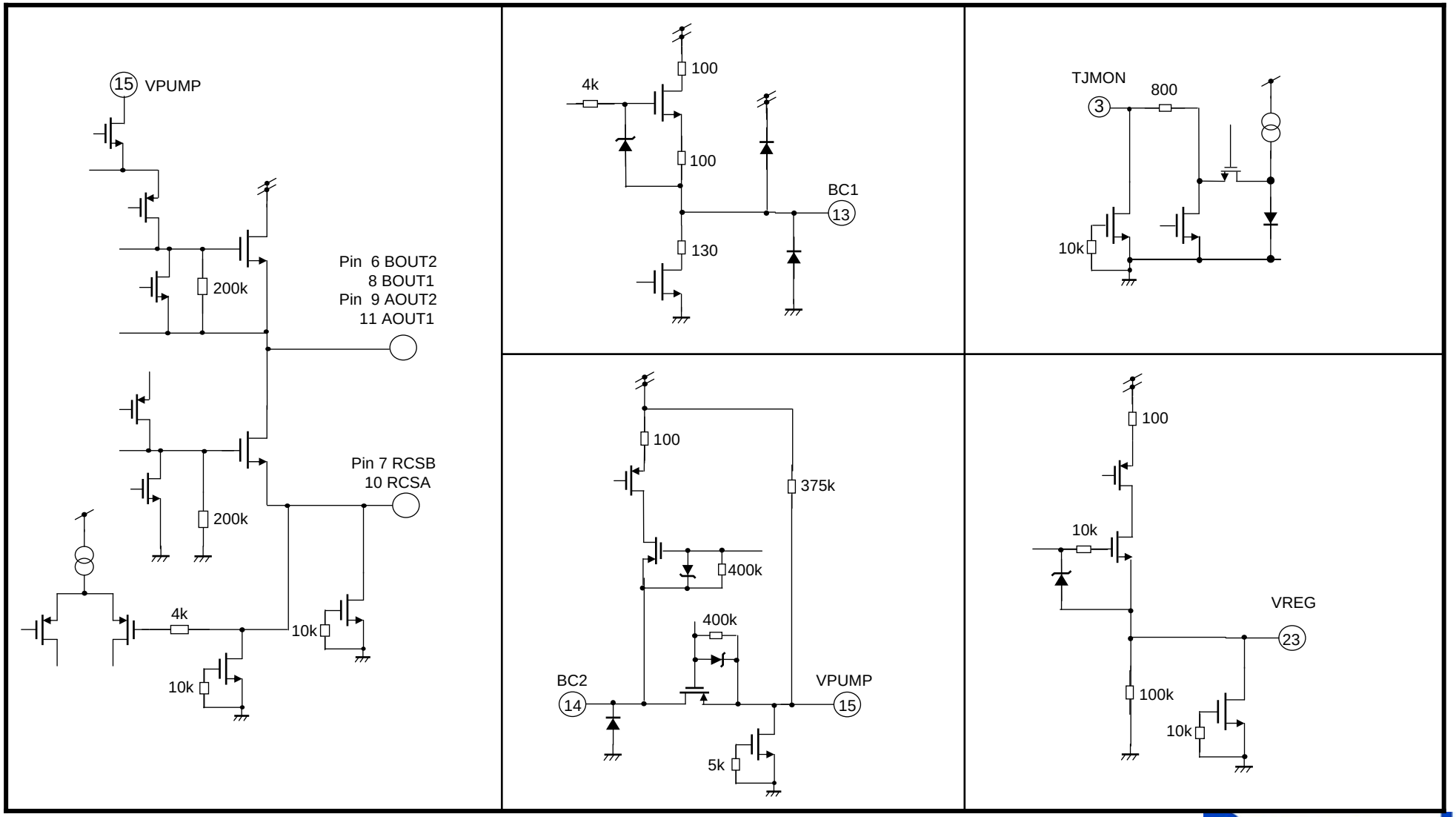
Ground

Input/Output block Circuits are as follows.



# 4-5. Input/Output Block Circuits

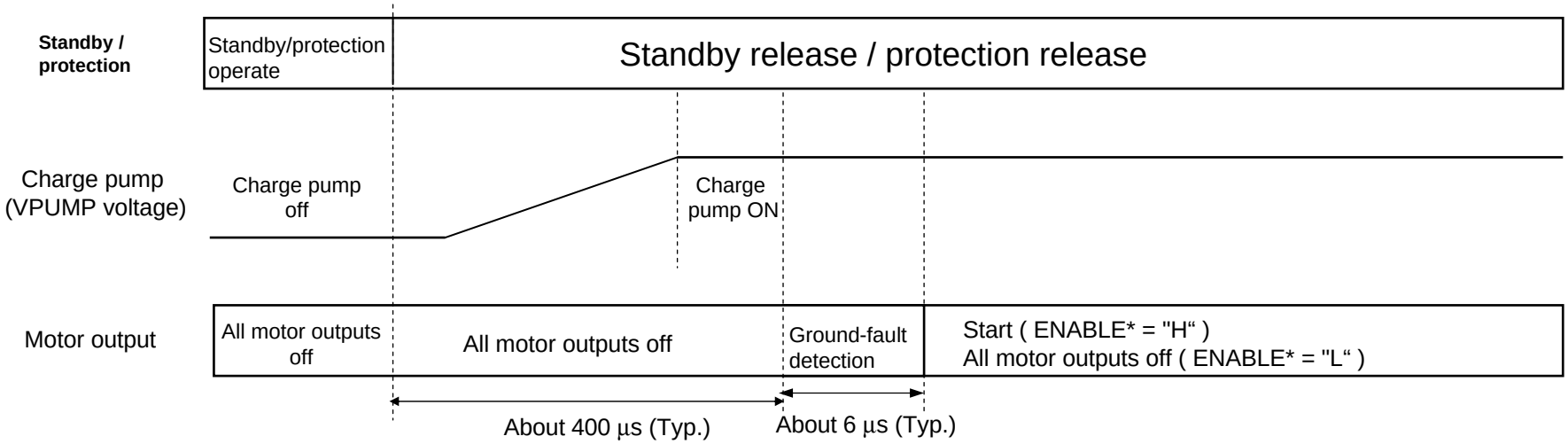
Input/Output block Circuits are as follows.



# 5. Off Timer Function

The charge pump circuit is stopped when standby mode activates or UVLO is detected.
This LSI has the Off timer function that all motor outputs are turned off during constant period (typ. : about 400 µs) after standby state or each protection release.
The purpose of "Off-timer" is that it starts motor after charge pump voltage increases enough.

And this LSI has the period to detect the ground-fault of motor outputs after the Off timer function operates.
This period is about 6µs. All upper output MOS transistors are turned on while this period, and it checks whether that motor outputs shorts or does not short to the ground (refer to the following).
All motor outputs are turned off and motor is stopped if it detects the ground-fault.




*** : A or B**

# 6. Internal Voltage Source

## 6-1. VREG Output Capacitance

Set capacitance 0.1uF(recommended value) between VREG and GND to stabilize VREG output voltage.

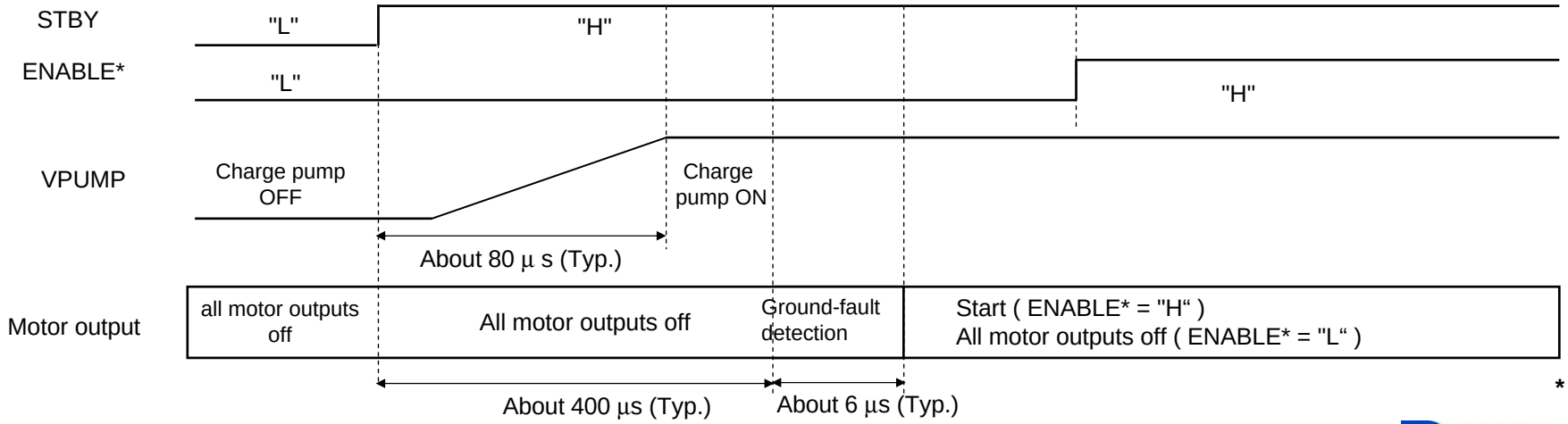
## 6-2. Charge Pump Voltage

In case of Standby or UVLO, the charge pump circuit is stopped, as described in “5.OFF Timer Function”.
This LSI has all motor outputs OFF period of about 400µs(typ) to ensure the start-up time of charge pump.

The rising time of change pump is about 80µs under the following condition.
Condition ⇒ BC1-BC2 capacitance : 0.01µF, VPUMP-GND capacitance : 0.01µF, VREG-GND capacitance : 0.1µF

The rising time of charge pump voltage depend on external capacitance value. When the capacitance of between VPUMP and GND is large, the rising time of charge pump might be longer than all motor outputs off period. At this time, the LSI overheating and abnormal operation may be caused by the motor start-up before the charge pump voltage rises. Therefore, release Standby and UVLO at ENABLE = "L“.
Restart at ENABLE ="H" after the charge pump voltage increases enough.

● **standby release**




*** : A or B**

# 7. Torque Control

## 7-1. Current Calculation Formula

In this LSI, $I_{PEAK}$ is a current value flowing through the motor (at 100%) , it can be determined by detection resistance (Rcs) and reference voltage (VREF).

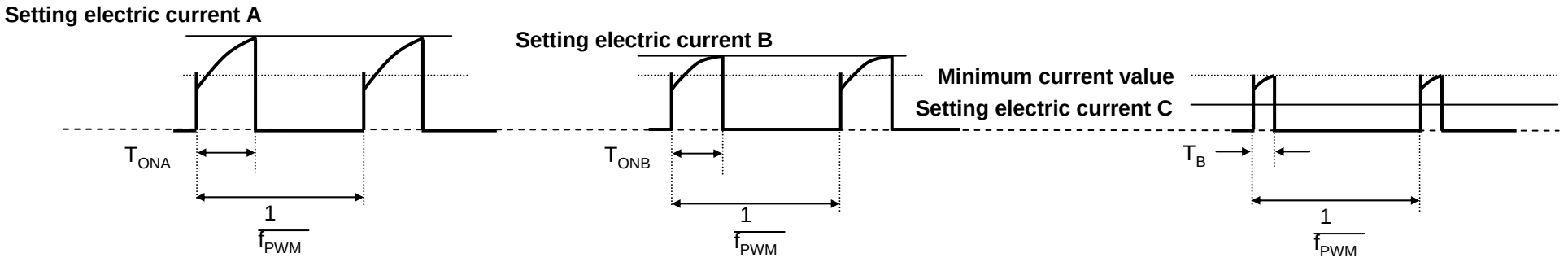
$$I_{PEAK} = \frac{1}{10} \times VREF \times \frac{1}{Rcs}$$

- For example , if you want to set $I_{PEAK}$ = 1.0A in VREF = 2.0V, from the above expression, it is obtained as the following calculation formula.

$$Rcs = \frac{1}{10} \times 2.0(V) \times \frac{1}{1.0(A)} = 0.20(\Omega)$$

# 7-2. Min-Duty

- This LSI adopts current mode PWM.
  The setting current depends on ON-Duty of chopping on time, but it has pulse blanking time (forced ON time: 0.75 µs (Typ.)) to prevent current false detection from noise.
- The minimum value of the current control is limited by ON-Duty (Min-Duty) decided from pulse blanking time and the PWM period. Therefore even if VREF is set to 0V, the current does not become "0".



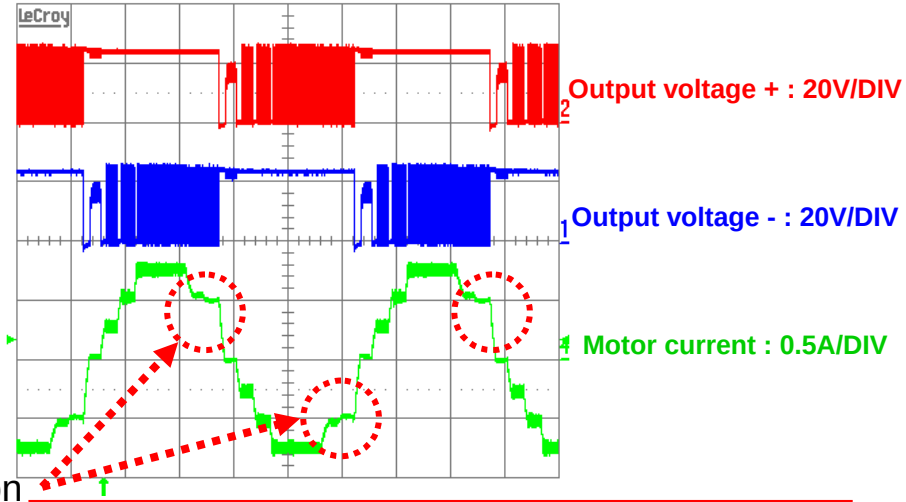

$f_{PWM}$ : PWM frequency
$T_{ON}$ : Chopping ON time
$T_B$ : Pulse blacking time ( Typ. = 0.75 us )

- In the figure above, the electric current is controlled normally in setting electric current A, B because ON-Duty is more larger than Min-Duty. But the electric current is limited because ON-Duty reaches Min-Duty in setting electric current C.

# 8. PWM Drive (Current Waveform Improvement by Mix Decay Function )

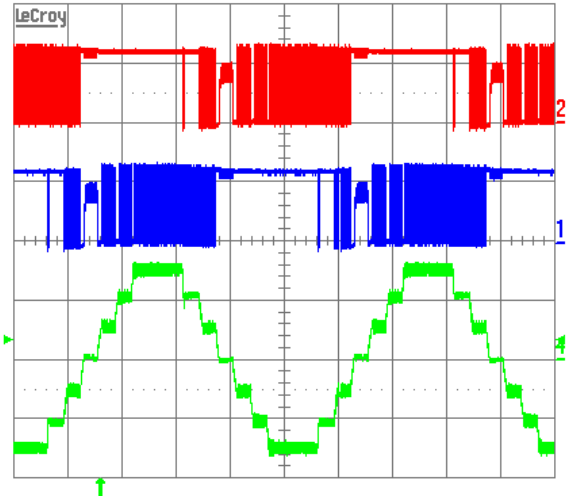
The following figures are motor waveforms comparing Slow Decay and Mix Decay in W1-2 phase excitation drive.
As shown in the figure below, when motor current is reduction side in Slow Decay mode, waveform distortions may occur by motor current flowing in excess. When motor current flows in excess in Slow Decay, it is not possible to decrease the current sufficiently, because the current decrement in the OFF interval is gradual. This is why a motor current waveform continues flowing in excess.
This phenomenon tends to occur during high-speed rotation.
On the other hand, there is no distortion in Mix Decay mode, the current waveform becomes the sine wave.
When the motor current is flowing in excess, it is possible to decrease the current sharply by Mix Decay( Fast Decay) control, and it can improve the waveform immediately.
Note) Heating surface in Mix Decay get worse than in Slow Decay.
At first, confirm the current waveform in DECAY1/2=L Slow Decay.
Then if there is a distortion in the current waveform, reconfirm Mix Decay 25% or 50%, and reset.

**Slow Decay : DECAY1/2=L**




There is distortion in the motor current

**Mix Decay 25% : DECAY1=L,DECAY=H**



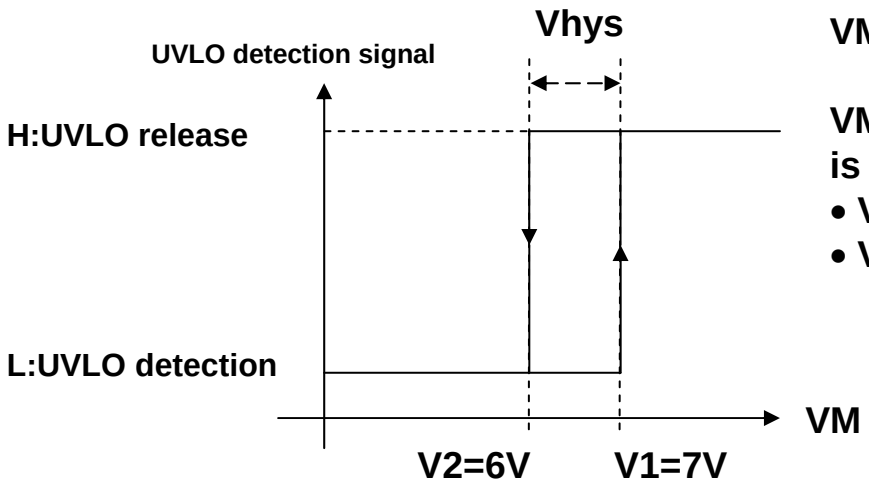

No distortion in the motor current

# 9. Protection Circuit

## 9-1. Under–voltage Lockout (UVLO)

**This LSI has under-voltage lockout (UVLO) circuit.**
**In case of UVLO detection, all motor outputs are turned off.**

**UVLO Operation**




**VM : 24V → 0V threshold value (V2)= 6V (Typ.)**
**VM : 0V → 24V threshold value (V1)= 7V (Typ.)**

**VM voltage range that all outputs are turned off is as follows.**
- **VM Power supply rise edge : 0V to 7V(typ.)**
- **VM Power supply fall edge : ≤ 6V (typ.)**

## 9-2. Thermal Protection

Thermal protection (Thermal Shut Down : TSD) circuit is incorporated in this LSI. All motor outputs are turned off in thermal protection operation.
In thermal protection operation, when the chip temperature reaches 150 °C (typ.). The TSD circuit turns off the all motor outputs and latches.
The latch state for all motor outputs OFF is released by standby and UVLO (power supply : restart).

# 9 .Protection Circuit

## 9-3. Over-current Protection (OCP)

This LSI is equipped with over-current protection circuit for destruction measures against ground fault of motor output. When flowing the setting electric current of 5A or more through power MOS during approximately 5µs (typ) by ground fault, all motor outputs becomes turned off by latch circuit . This latch state can be released by standby or Under Voltage Lockout (restarts power supply). The OCP circuit doesn‘t guarantee the protection of set. Don’t design the protection circuit of the set using this OCP function. Note that there is a possibility that this LSI breaks before the protection function operates when it instantaneously exceeds the safe operation area and the maximum rating of the device. When the line of ground fault is long and the inductor element is large, there is a possibility that this LSI broken. Because the motor output voltage falls on a negative voltage or rises excessively after over-current flows.

## 9-4. Protection for Interface Pins

This LSI offers the malfunction measures of signal input to the interface pins(*1) of the power supply not turned on. Therefore, the LSI doesn't cause to break and malfunction by the input voltage to the interface pins when its power voltage isn’t supplied.

*1 : (ENABLEA,ENABLEB,IN0 to IN3,PHA,PHB,STBY,VREFA,VREFB)

## 9-5. Abnormal Detection Output Pin (NFAUT)

This LSI outputs the operation state of TSD (Thermal Shut Down) and OCP (Over Current Protection) through the abnormal detection output pin (NFAULT). Each protection operation is shown in the table below. In addition, this terminal is open-drain output. In case of use, the pull-up resistance to a power supply is necessary.

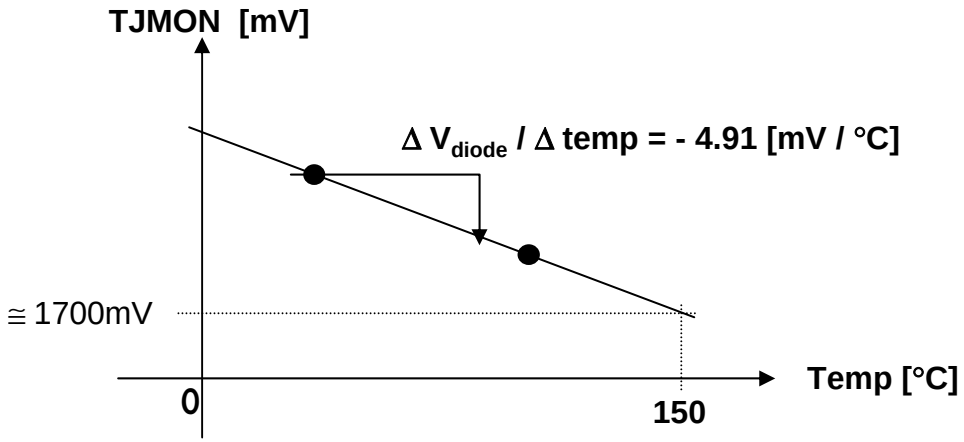
Truth table (NFAULT output)

| TSD(*1) | OCP(*2) | NFAULT | Output transistor |
|---|---|---|---|
| Detection | - | "L" | OFF |
| - | Detection | "L" | OFF |
| Release | Release | Hi-Z | ON |

Note) *1: TSD is latch type. ⇒ Protection operates when the chip temperature reaches 150 °C (latch for All power OFF). The latch is released by STBY or UVLO .
*2: OCP is latch type. ⇒ Latch for All power OFF by over current detection. The latch is released by STBY or UVLO .
All motor outputs OFF when UVLO operates.

# 10. Thermal Evaluation Method

This LSI has the terminal(PIN32:TJMON) for measurement chip temperature and the diode voltage is output at TJMON.
it is possible to estimate chip temperature of the LSI in below reference figure.




**The temperature characteristics of TJMON**

Evaluation Method
Open TJMON , when measuring chip temperature.

In estimating chip temperature, calculate it by the difference of TJMON voltage before motor operating (time : t1) and TJMON voltage after motor operating (time : t2) .

$$\Delta\ \text{Temp} = \frac{V_{diode}(t_1) - V_{diode}(t_2)}{4.91 \times 10^{-3}}$$

**Notes)**

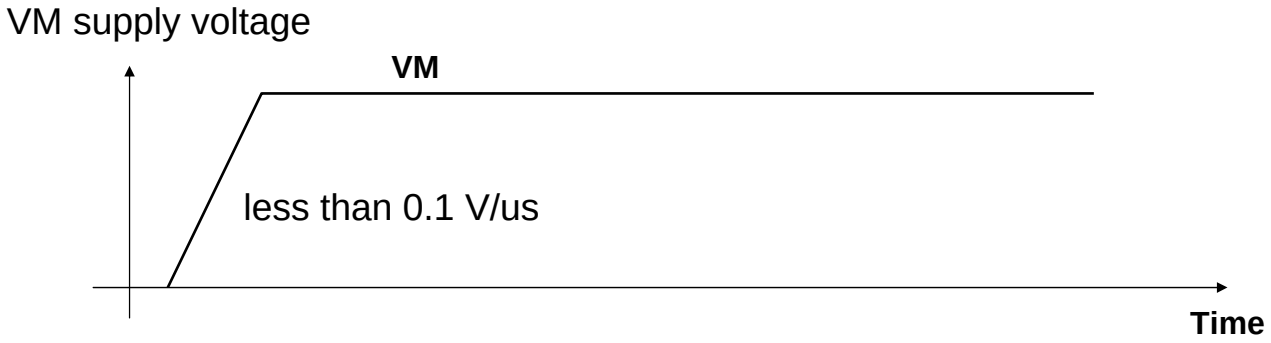
- The estimate value of chip temperature by $\Delta V_{diode}$ measurement methcd is technical reference data, is not guaranteed. Conduct a sufficient reliability test of the LSI and evaluate the product with the LSI incorporated.
- The recommended derating value is 70% to 80 % of maximum rating (Tjmax =150 °C).

# 11. Precaution for Power-up and Power Supply Change

When supplying to VM (Pin1, 16) , set the rise speed of VM voltage to less than 0.1 V/µs . If the rise speed of supply voltage is too rapid, that might cause error of operation and destruction of the LSI. If the rise speed of VM voltage is more rapid than 0.1V/µs, conduct a sufficient reliability test and also check a sufficient evaluation for a product.

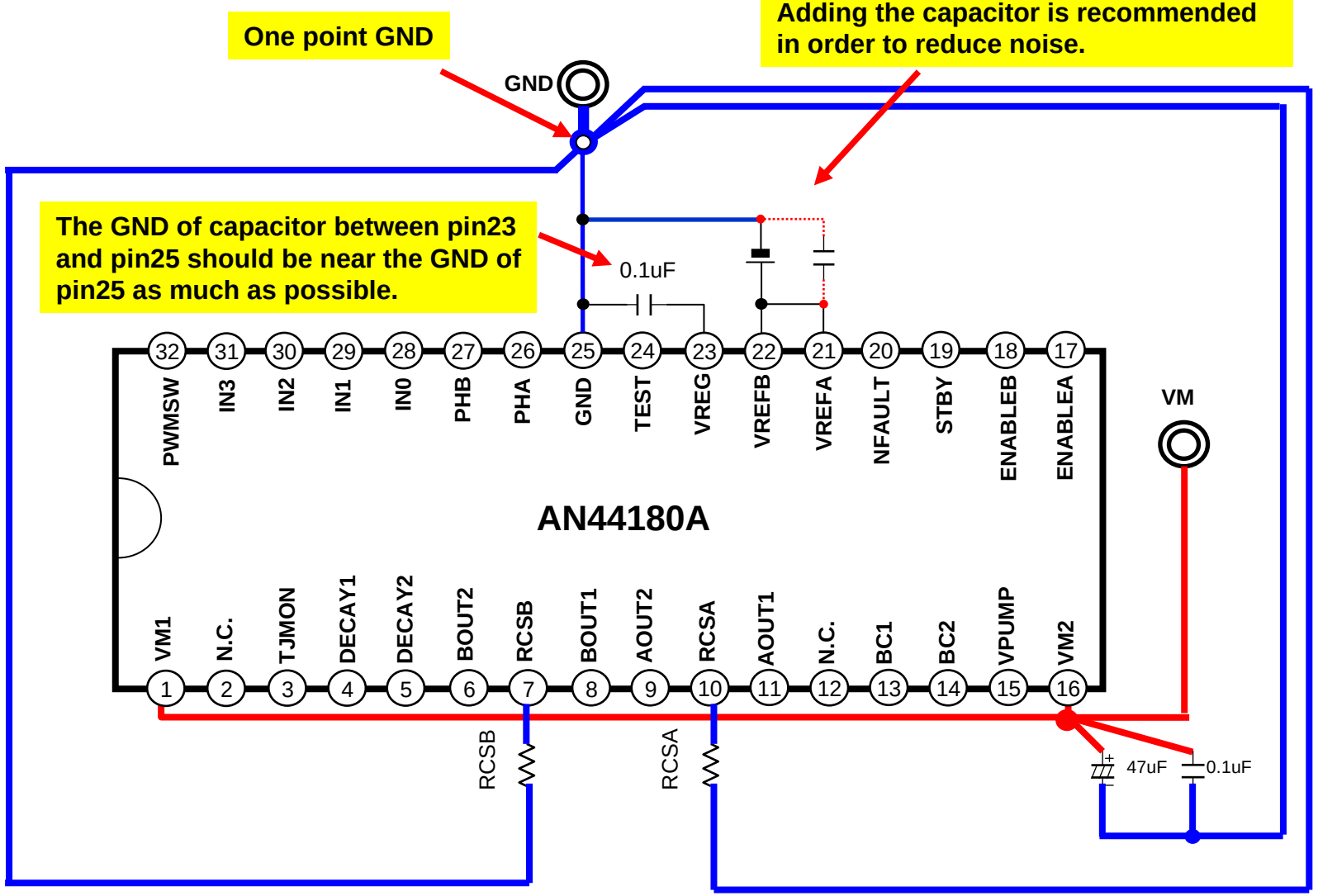
In addition, rise the VM supply voltage in an ENABLE=L state when changing VM supply voltage from low voltage to high voltage in the operating supply voltage range.
Because there is not OFF interval by the OFF-timer function shown in Page12 for the changing supply voltage in the operating supply voltage range, the VPUMP voltage is in the low voltage state due to not following the rise in the VM supply voltage enough and the LSI might not operate normally.

Therefore restart it by ENABLE = "H" after the VPUMP voltage rises enough.
In addition, when falling the VM voltage, it is recommended that it is fallen in a motor stop state (ENABLE= "L" or STBY= "L" ) for the stable fall of supply voltage.



# 12. Precaution on Board Pattern Design

## 12-1. Recommended Pattern No.1



# 12. Precaution on Board Pattern Design

## 12-2. Recommended Pattern No.2

■Stabilization in LSI operation

(1)Design GND and VM pattern of the bold line shortly and widely for lower impedance as much as possible and lay them out individually. (for GND stabilization of the LSI)

(2)Design GND line of the capacitor between VREG(PIN23) and GND(PIN25) for GND of PIN25 as short as possible and lay it out individually. (for stabilization of the regulator voltage )

(3)Design GND line of the voltage source generating VREF voltage for GND of PIN25 as short as possible and lay it out individually. (for stabilization of VREFA/B voltage )

■Reduction in heating

This package radiates heat mainly from the lead and the back side of PKG. Therefore, design the circuit pattern in consideration of the following points

(1)Secure the wide pattern space of VCC and GND for heat radiation as much as possible.

⇒ In the vicinity of the lead connection points, connect them to the back side of PCB and the middle layers through " Via ".

⇒ Secure the wide pattern space for plane wiring as much as possible.

(2)Connect N.C. pin and unused pin (for example: TJMON pin) to GND pin.

⇒ It promotes the heat radiation from the lead.

(3) Lay the ground plane for the wide pattern right under PKG as much as possible.

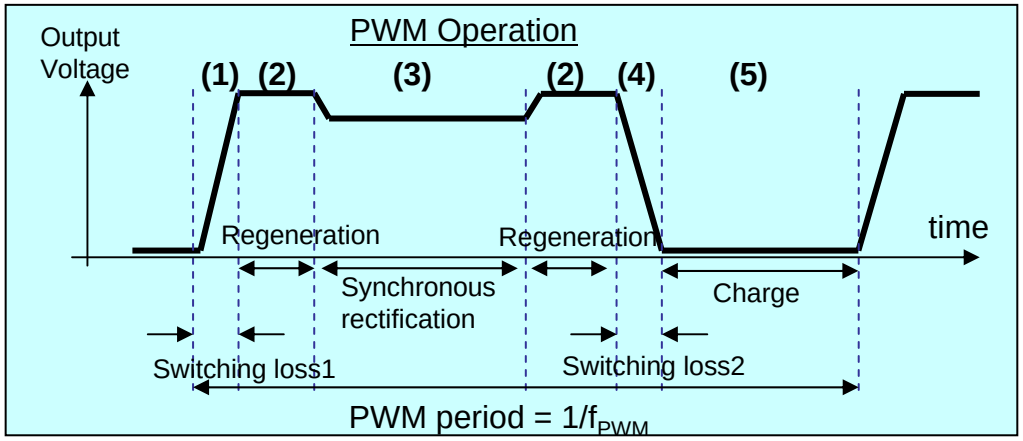
⇒ The back side of LSI don't touch PCB directly, but the heat diffuses to PCB from the back side of PKG, because it comes close in about 0.1mm.

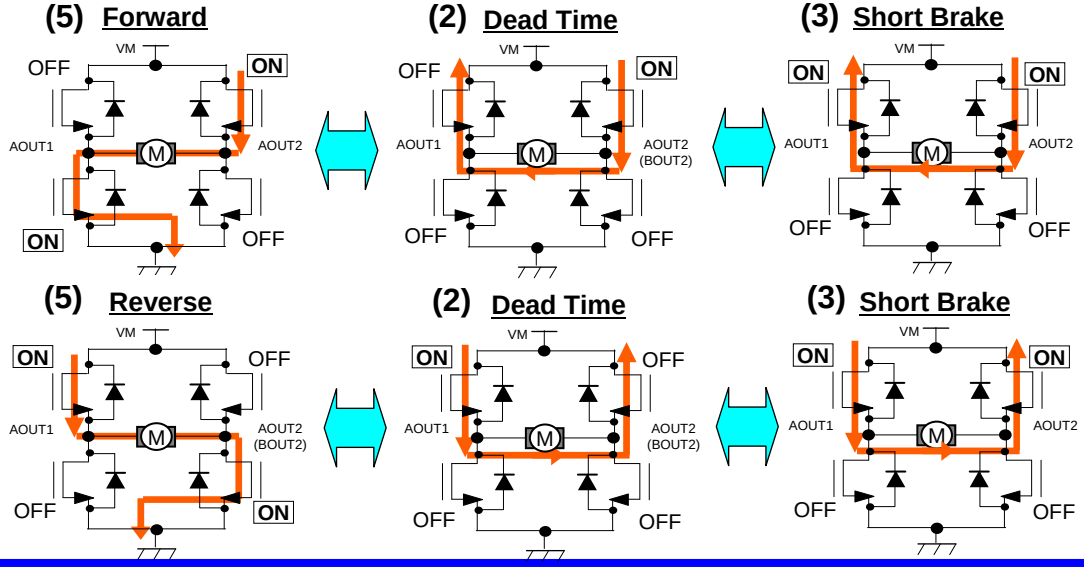
(4) Put the high heating components from LSI apart as much as possible.

⇒ Because if they are near LSI, temperature of LSI rises under the influence of it.

# 13. Power Consumption during PWM Operating

Power consumption during PWM operation is the sum of (1) to (5) in figure below.
About power consumption of each item, refer to the expression of the lower right.
Notes (1) The following expression is for the simplified calculation and not guaranteed.
(2) Conditions of calculation expression, assumes the electric current of rectangular wave in 2-phase excitation.
(3) Some items for the simplified calculation like PWM Duty are fixed values that are different from the actual.




■ Switching loss : **(1)+(4)**

$$P_{Switch} = \frac{1}{2} VM \times I_{Motor} \times (t_{Switch1} + t_{Switch2}) \times f_{PWM}$$

■ Regeneration : **(2)**

$$P_{Rege} = 2 \times (V_{DI} \times I_{Motor} + I^2_{Motor} \times R_{Up}) \times t_{Dead} \times f_{PWM}$$

■ Synchronous rectification : **(3)**

$$P_{Sync} = 2 \times I^2_{Motor} \times R_{Up} \times t_{Sync} \times f_{PWM}$$

■ Charge : **(5)**

$$P_{Gene} = I^2_{Motor} \times (R_{Up} + R_{Lo}) \times t_{Gene} \times f_{PWM}$$

■Power consumption

$$P_{PWM} = (P_{Switch} + P_{Rege} + P_{Sync} + P_{Gene})$$

VM : Motor voltage
IMotor : Motor current
(IMotor is considered constant approximately during PWM operating.)
Rup : On resistance of upper power transistor
Rlo : On resistance of lower power transistor
VDI : Diode forward direction voltage
tDead : Synchronous rectification dead time
fPWM : PWM frequency

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