Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

Application Note

Part No.	AN41908A
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Semiconductor Business Group
Industrial Devices Company
Panasonic Corporation

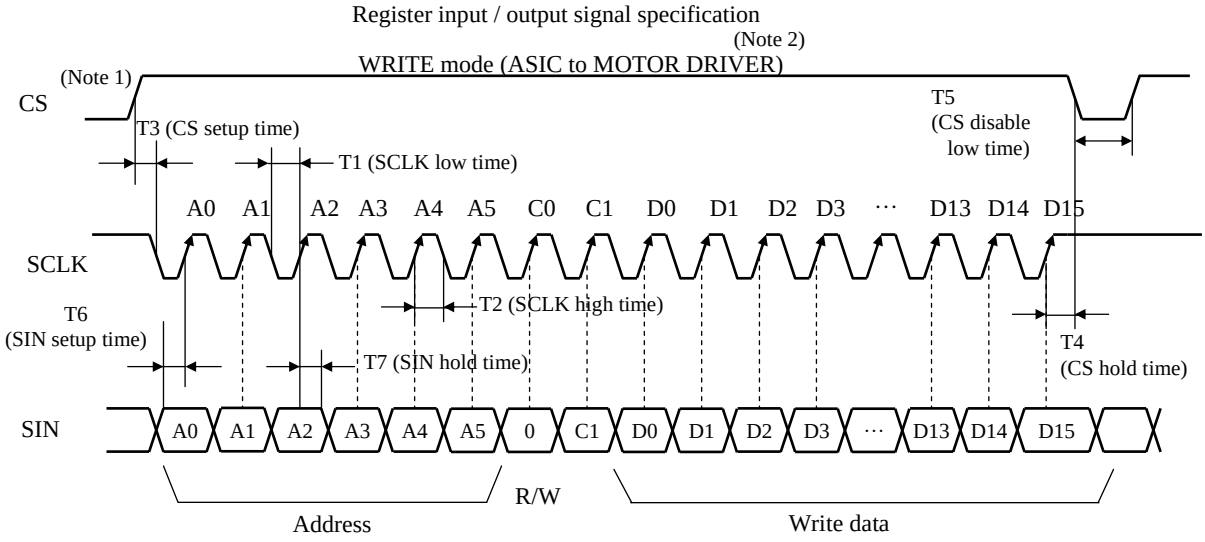
Established by	Applied by	Checked by	Prepared by
			A.Chigira

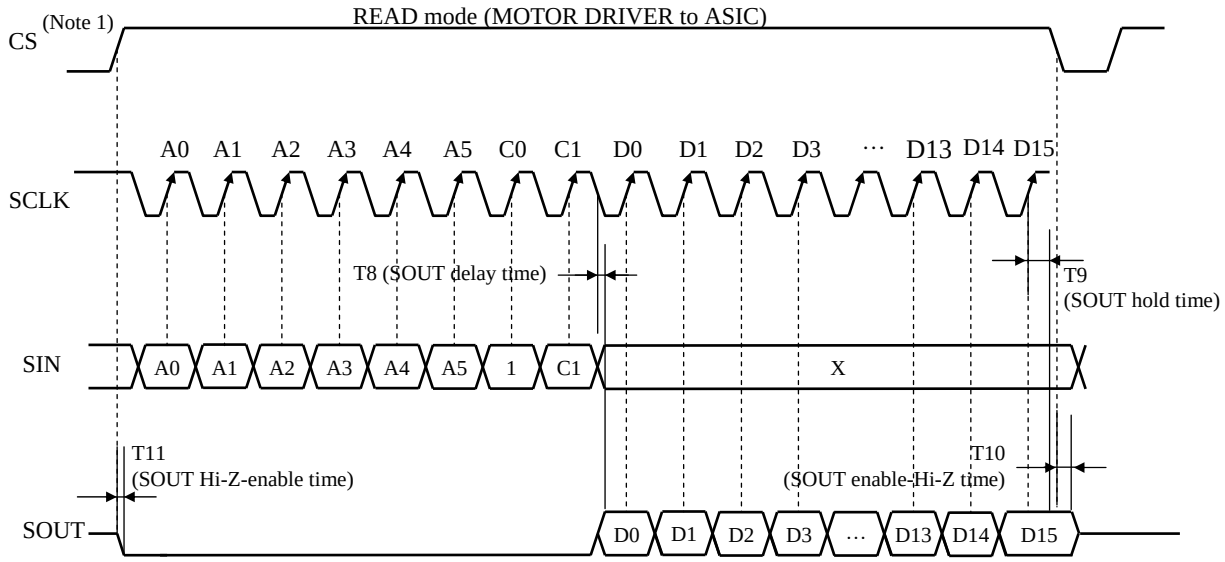
Contents

Serial Interface

■ Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.





Note 1) CS default value of each cycle (Write / Read mode) starts from Low-level.
Note 2) It is necessary to input the system clock OSCIN at write mode.

■Electrical Characteristics (Reference values for design) at AVDD5, MVCCx = 4.8 V, DVDD, AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Reference values			Unit
				Min	Typ	Max	
S1	Serial clock	Sclock	—	1	—	5	MHz
S2	SCLK low time	T1	—	100	—	—	ns
S3	SCLK high time	T2	—	100	—	—	ns
S4	CS setup time	T3	—	60	—	—	ns
S5	CS hold time	T4	—	60	—	—	ns
S6	CS disable low time	T5	—	100	—	—	ns
S7	SIN setup time	T6	—	50	—	—	ns
S8	SIN hold time	T7	—	50	—	—	ns
S9	SOUT delay time	T8	—	—	—	60	ns
S10	SOUT hold time	T9	—	60	—	—	ns
S11	SOUT enable-Hiz time	T10	—	—	—	60	ns
S12	SOUT Hiz-enable time	T11	—	—	—	60	ns
S13	SOUT Cload	Tsc	—	—	—	40	pF

■ Register Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00H							IRS_TGT[9:0]									
01H	DGAIN[6:0]							ASOUND_LPF_FC[2:0]			AS_FLT _OFF	DEC _AVE	OVER_LPF_FC _2ND[1:0]		OVER_LPF_FC _1ST[1:0]	
02H	PID_POLE[3:0]				PID_ZERO[3:0]				IRIS_ROUND[3:0]				IRIS_CALC_NR[3:0]			
03H			DT_ADJ_IRIS[1:0]		PWM_IRIS[2:0]			PWM_LPF_FC[2:0]			PWM_FLT _OFF	LMT _ENB	ARW[3:0]			
04H	HALL_OFFSET_DAC[7:0]								HALL_BIAS_DAC[7:0]							
05H				AAF_FC	HALL_GAIN[3:0]						PID_INV	TGT_FLT _OFF	TGT_LPF_FC[3:0]			
06H							START1[9:0]									
07H	P1EN				WIDTH1[11:0]											
08H							START2[9:0]									
09H	P2EN										WIDTH2[5:0]					
0AH						DUTY _TEST	TGT_IN_TEST[9:0]									
0BH	PID_CLIP[3:0]				ADC _TEST	PDWNB	MODESEL _FZ	MODESEL _IRIS	TESTEN1			ASWMODE[1:0]				
0CH							IRSAD[9:0] (Read Only)									
0DH																
0EH				AVE_SPEED[4:0]					TGT_UPDATE[7:0]							
0FH						Reserved	Reserved									
10H																
20H		PWMRES[1:0]		PWMMODE[4:0]					DT1[7:0]							
21H									TESTEN2			FZTEST[4:0]				
22H			PHMODAB[5:0]						DT2A[7:0]							
23H	PPWB[7:0]								PPWA[7:0]							
24H			MICROAB[1:0]		LEDB	ENDISAB	BRAKE AB	CCWCW AB	PSUMAB[7:0]							
25H	INTCTAB[15:0]															
26H																
27H			PHMODCD[5:0]						DT2B[7:0]							
28H	PPWD[7:0]								PPWC[7:0]							
29H			MICROCD[1:0]		LEDA	ENDISCD	BRAKE CD	CCWCW CD	PSUMCD[7:0]							
2AH	INTCTCD[15:0]															
2BH																
2CH														Reserved	Reserved	Reserved

■ Register List

Address	Register name / Bit wide	Function	Page
00h	IRS_TGT[9:0]	Iris target	40
01h	OVER_LPF_FC_1ST[1:0]	ADC feedback filter (1) cut-off frequency	41
	OVER_LPF_FC_2ND[1:0]	ADC feedback filter (2) cut-off frequency	41
	DEC_AVE	Moving average of Iris target	42
	AS_FLT_OFF	Filter before PID controller enable / disable	42
	ASOUND_LPF_FC[2:0]	Filter cut-off frequency before PID controller	43
	DGAIN[6:0]	PID controller digital gain	43
02h	IRIS_CALC_NR[3:0]	PID controller integral error cumulative prevention level	45
	IRIS_ROUND[3:0]	PID controller differential error cumulative prevention level	45
	PID_ZERO[3:0]	PID controller zero point	46
	PID_POLE[3:0]	PID controller pole	46
03h	ARW[3:0]	Number of bits in PID controller integrator	49
	LMT_ENB	PID controller integral stop	49
	PWM_FLT_OFF	LPF after PID controller enable / disable	50
	PWM_LPF_FC[2:0]	LPF cut-off frequency after PID controller	50
	PWM_IRIS[2:0]	PWM frequency of Iris block output	51
	DT_ADJ_IRIS[1:0]	Dead time correction of Iris block output	51
04h	HALL_BIAS_DAC[7:0]	Drive current value for hall element	63
	HALL_OFFSET_DAC[7:0]	Offset adjustment for hall element output amplifier	63
05h	TGT_LPF_FC[3:0]	Iris target value LPF cut-off frequency	52
	TGT_FLT_OFF	Iris target value LPF function enable / disable	52
	PID_INV	PID controller polarity	53
	HALL_GAIN[3:0]	Hall element output amplifier gain	64
	AAF_FC	Cut-off frequency of hall element output amplifier	64
06h	START1[9:0]	Pulse 1 start time	54
07h	WIDTH1[11:0]	Pulse 1 width	54
	P1EN	Pulse 1 output enable	54
08h	START2[9:0]	Pulse 2 start time	56
09h	WIDTH2[5:0]	Pulse 2 width	56
	P2EN	Pulse 2 output enable	56

■ Register List (continued)

Address	Register name / Bit wide	Function	Page
0Ah	TGT_IN_TEST[9:0]	Iris output duty direct specified value	58
	DUTY_TEST	Iris output duty direct specification enable	59
0Bh	ASWMODE[1:0]	ADTESTIN pin connection selection	65
	TESTEN1	Test mode enable 1	31
	MODESEL_IRIS	VD_IS polarity selection	13
	MODESEL_FZ	VD_FZ polarity selection	13
	PDWNB	Power down of Iris block	65
	ADC_TEST	ADC read value updated timing	65
	PID_CLIP[3:0]	Iris output PWM maximum duty	67
0Ch	IRSAD[9:0]	ADC output for Iris (read only)	68
0Eh	TGT_UPDATE[7:0]	IRS_TGT (iris target) update delay time	60
	AVE_SPEED[4:0]	Iris target moving average speed	61

■ Register List (continued)

Address	Register name / Bit wide	Function	Page
20h	DT1[7:0]	Start point wait time	18
	PWMMODE[4:0]	Micro step output PWM frequency	20
	PWMRES[1:0]	Micro step output PWM resolution	20
21h	FZTEST[4:0]	PLS1/2 pin output signal selection	29
	TESTEN2	Test mode enable 2	31
22h	DT2A[7:0]	α motor start point excitation wait time	19
	PHMODAB[5:0]	α motor phase correction	21
23h	PPWA[7:0]	Driver A peak pulse width	22
	PPWB[7:0]	Driver B peak pulse width	22
24h	PSUMAB[7:0]	α motor step count number	23
	CCWCWAB	α motor rotation direction	24
	BRAKEAB	α motor brake	25
	ENDISAB	α motor enable/disable control	26
	LEDB	LED B output control	69
	MICROAB[1:0]	α motor sine wave division number	27
25h	INTCTAB[15:0]	α motor step cycle	28
27h	DT2B[7:0]	β motor start point excitation wait time	19
	PHMODCD[5:0]	β motor phase correction	21
28h	PPWC[7:0]	Driver C peak pulse width	22
	PPWD[7:0]	Driver D peak pulse width	22
29h	PSUMCD[7:0]	β motor step count number	23
	CCWCWCD	β motor rotation direction	24
	BRAKECD	β motor brake	25
	ENDISCD	β motor enable/disable control	26
	LEDA	LED A output control	69
	MICROCD[1:0]	β motor sine wave division number	27
2Ah	INTCTCD[15:0]	β motor step cycle	28

■ Serial Interface Specifications

Data transfer starts at the rising edge of CS, and stops at the falling edge of CS.
One unit of data is 24 bits. (24 bits of the following format are called a data set in this book.)
Address and data are serially input from SIN pin in synchronization with the data clock SCK at CS = 1.
Data is retrieved at the rising edge of SCK.
Moreover, data is output from SOUT pin at data readout. (Data is output at the rising edge of SCK.)
SOUT outputs Hi-Z at CS = 0, and outputs "0" except data readout at CS = 1.
The control circuit of serial interface is reset at CS = 0.

■ Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

C0 : Register write / read selection 0 : write mode, 1 : read mode
C1 : Unused
A5 to A0 : Address of register
D15 to D0 : Data written in register

When C0 bit is "0", the write mode is selected. The address and data are retrieved from SIN in synchronization with the rising edge of data clock SCLK, and the data is stored in internal register in synchronization with the rising edge of CS.
SOUT outputs "0" in the write mode.

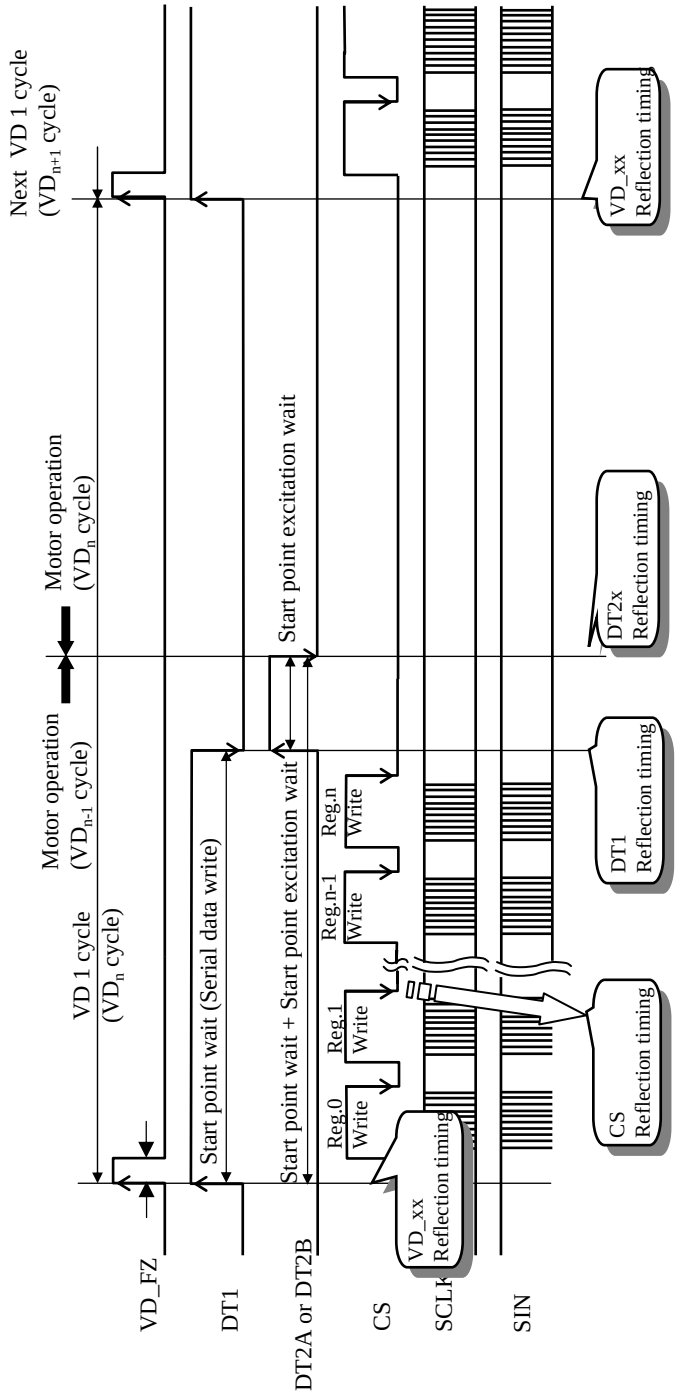
When the data which is 23 or less bits per 1 processing is received in the write mode, the received data becomes invalid.
The data of 25 or more bits is regarded as the continuous write mode, and the write operation is performed whenever the data of 24 bits is received. When the last data set is less than 24 bits in the continuous write mode, it becomes invalid. (The previous data set is valid.)
Even if noise occurs on SCK signal in the continuous write mode and the shifted data is received, pay attention to continue receiving or updating the shifted data.

When C0 bit is "1", the read mode is selected. The address is retrieved from SIN in synchronization with the rising edge of SCK, and then the register value of the address specified is output as LSB first from SOUT, in synchronization with the rising edge of SCK.
When C0 bit is "1", the values of D15 to D0 of SIN do not be cared.

■ Formatting

All the SIF functions containing a data register are formatted at RSTB = 0.

■ Register Setup Timing



■ Register Setup Timing (continued)

Address	Register Name	Setup Timing
00h	IRS_TGT[9:0]	VD_IS+Adjusted value
01h	OVER_LPF_FC_1ST[1:0]	VD_IS
	OVER_LPF_FC_2ND[1:0]	VD_IS
	DEC_AVE	VD_IS
	AS_FLT_OFF	VD_IS
	AS_LPF_FC[2:0]	VD_IS
	DGAIN[6:0]	VD_IS
02h	IRIS_CALC_NR[3:0]	VD_IS
	IRIS_ROUND[3:0]	VD_IS
	PID_ZERO[3:0]	VD_IS
	PID_POLE[3:0]	VD_IS
03h	ARW[3:0]	VD_IS
	LMT_ENB	VD_IS
	PWM_FLT_OFF	VD_IS
	PWM_LPF_FC[2:0]	VD_IS
	PWM_IRIS[2:0]	VD_IS
	DT_ADJ_IRIS[1:0]	VD_IS
04h	HALL_BIAS_DAC[7:0]	VD_IS
	HALL_OFFSET _DAC[7:0]	VD_IS
05h	TGT_LPF_FC[3:0]	VD_IS
	TGT_FLT_OFF	VD_IS
	PID_INV	VD_IS
	HALL_GAIN[3:0]	VD_IS
	AAF_FC	VD_IS
06h	START1[9:0]	VD_IS
07h	WIDTH1[11:0]	VD_IS
	P1EN	VD_IS
08h	START2[9:0]	VD_IS
09h	WIDTH2[5:0]	VD_IS
	P2EN	VD_IS
0Ah	TGT_IN_TEST[9:0]	CS
	DUTY_TEST	CS
0Bh	ASWMODE[1:0]	CS
	TESTEN1	CS
	MODESEL_IRIS	CS

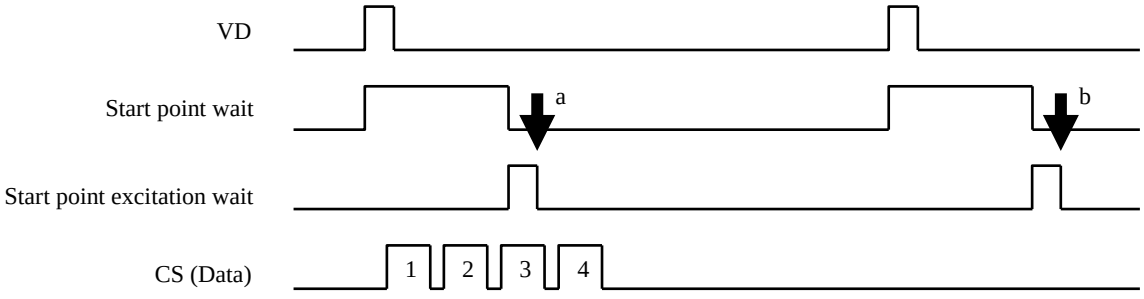
Address	Register Name	Setup Timing
0Bh	MODESEL_FZ	CS
	PDWNB	CS
	ADC_TEST	CS
	PID_CLIP[3:0]	VD_IS
0Ch	IRSAD[9:0]	Read Only
0Eh	TGT_UPDATE[7:0]	CS
	AVE_SPEED[4:0]	VD_IS
20h	DT1[7:0]	VD_FZ
	PWMMODE[4:0]	DT1
	PWMRES[1:0]	DT1
21h	FZTEST[4:0]	CS
	TESTEN2	CS
22h	DT2A[7:0]	DT1
	PHMODAB[5:0]	DT2A
23h	PPWA[7:0]	DT1
	PPWB[7:0]	DT1
24h	PSUMAB[7:0]	DT2A
	CCWCWAB	DT2A
	BRAKEAB	DT2A
	ENDISAB	DT1 or DT2A ※
	LEDB	CS
	MICROAB[1:0]	DT2A
25h	INTCTAB[15:0]	DT2A
27h	DT2B[7:0]	DT1
	PHMODCD[5:0]	DT2B
28h	PPWC[7:0]	DT1
	PPWD[7:0]	DT1
29h	PSUMCD[7:0]	DT2B
	CCWCWCD	DT2B
	BRAKECD	DT2B
	ENDISCD	DT1 or DT2B ※
	LEDA	CS
	MICROCD[1:0]	DT2B
2Ah	INTCTCD[15:0]	DT2B

※ 0 → 1: reflected at DT1 1 → 0: reflected at DT2x

■ Register Setup Timing (continued)

In principle, the setup of registers for micro step should be performed during the interval of start point wait (Refer to the figure in page 10). The data which is written at timing except the interval of start point wait can be also received. However, if the write operation continues after the reflecting timing such as the end of start point excitation wait, the setup reflection timing may not be performed at the intended timing (Refer to the following figure). For example, if the data 1 to 4 which is updated at the end of start point excitation wait are written as the following figure, data 1 and 2 is updated at the timing a, and data 3 and 4 is updated at the timing b. Even if the data is written continuously like this, the update timing may be shifted to 1 VD.

Due to the above reason, the setup of registers should be performed during the interval of start point wait in order to reflect the updated content certainly.



VD signal internal processing

■ Specifications

In this LSI, reflection timing and rotation timing of a stepping motor are based on the rising edge of VD_IS and VD_FZ respectively. The polarities of VD_IS and VD_FZ which are used for the internal processing can be set by the following setup.

■ Register detail description

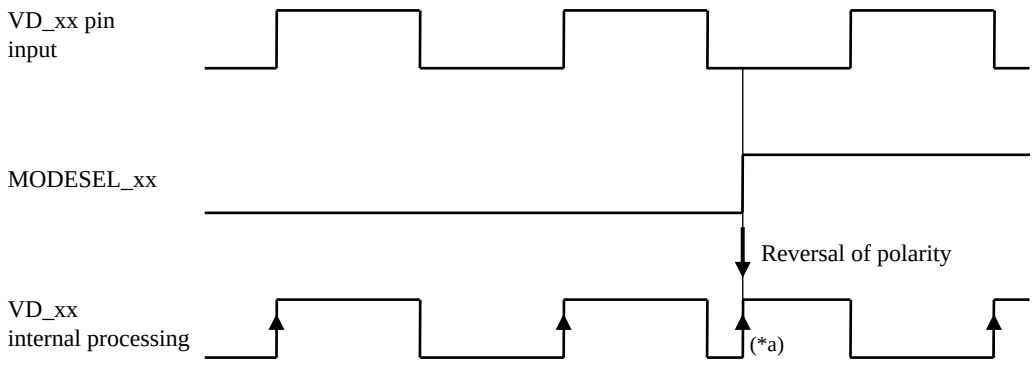
- MODESEL_IRIS (VD_IS polarity selection)
- MODESEL_FZ (VD_FZ polarity selection)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				MODESEL_IRIS		MODESEL_FZ									

MODESEL_IRIS and MODESEL_FZ respectively set the polarities of VD_IS and VD_FZ signals which is input to this IC.
When setting to "0", the polarity is based on the rising edge of VD_xx inputted.
When setting to "1", the polarity is based on the falling edge of VD_xx inputted.

MODESEL_xx selects the polarity of VD_xx inputted. Therefore, depending on the selection timing of MODESEL_xx, the timing which is not related to the edge (*a) of VD_xx which is input as the following figure may be regarded as an edge.

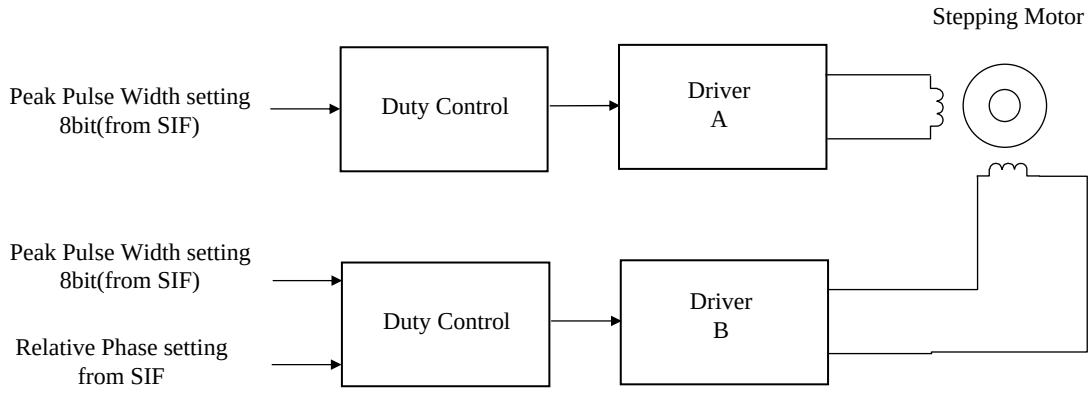
Setup value	VD polarity
0	Non-inverting
1	Inverting



Based on the rising edge of VD_xx internal processing

Micro Stepping Motor Driver

■ Block Diagram



- This block is a stepping motor driver for focus and zoom, and the following setup can be performed by serial control.
  (The following description is for α motor: driver A/B. β motor: driver C/D is the same function as α motor .)

- Main setup parameters
  1) Phase correction : The phase difference between a driver A and a driver B is on the basis of 90 degree, and can be adjusted from –22.5 degree to +21.8 degree. ・・・PHMODAB[5:0]
  2) Amplitude correction : It is possible to set the load current of driver A/B independently. ・・・PPWA[7:0], PPWB[7:0]
  3) PWM frequency : PWM driver chopping frequency is set. ・・・PWMMODE[4:0], PWMRES[1:0]
  4) Quasi-sine wave : Number of divisions can be set to 64, 128 and 256. ・・・MICROAB[1:0]
  5) Stepping cycle : Motor rotation speed is set. The rotation speed is constant regardless of number of divisions of quasi-sine wave. ・・・INTCTAB[15:0]

■ Electrical Characteristics at AVDD5, MVCCx = 4.8 V, DVDD, AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.

No.	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Motor driver 1 (Focus, Zoom)							
1	H bridge ON-resistance	R_{onFZ}	IM = 100 mA	—	—	2.5	Ω
2	H bridge leak current	I_{leakFZ}	—	—	—	0.8	μA

■ Setup Timing for Each Setup

Setup timing and number of times are shown as follows.
Since the setups for address 27h to 2Ah are the same as those of 22h to 25h, the descriptions for address 27h to 2Ah are omitted.
If each setup is set once, the setup is reflected at every VD pulses. Therefore, when the same setup is performed at two or more VD pulses, it is unnecessary to write at every VD pulse.

DT1[7:0] (Start point wait, Address 20h)
Update timing is set. After hard reset release (Pin 39 RSTB : Low → High), this setup should be performed before starting to excite and drive a motor.
Since this setup is updated by the start of VD, it is unnecessary to write during the start point wait.

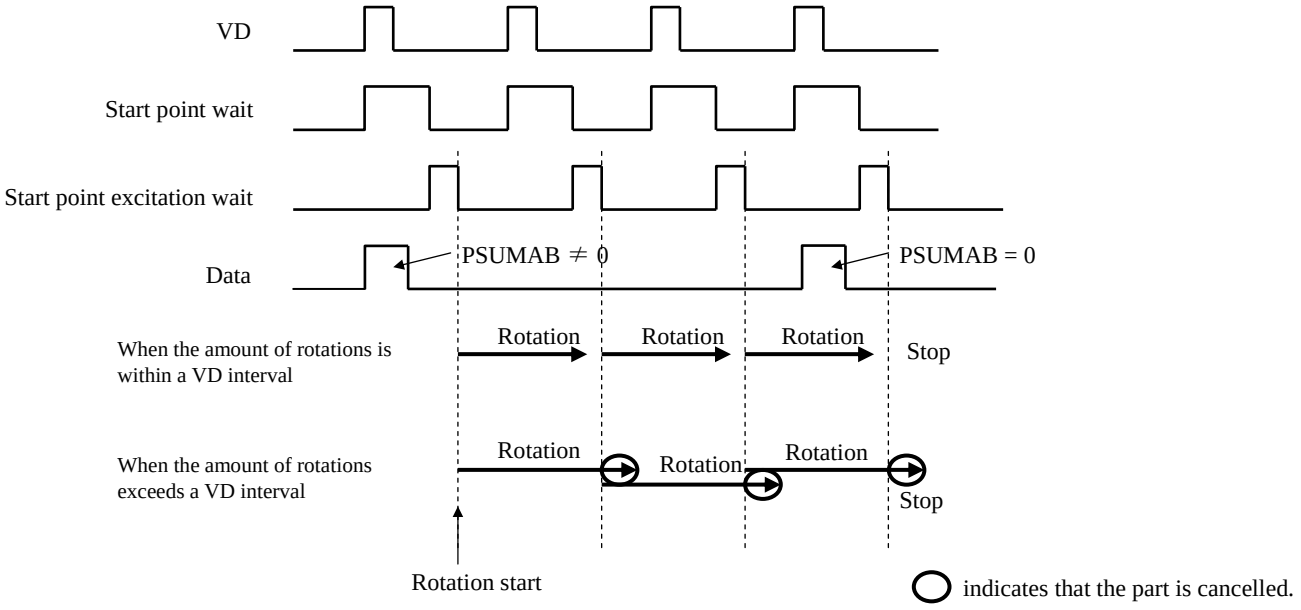
PWMMODE[4:0]，PWMRES[1:0] (Micro step output PWM frequency setup，Address 20h)
Micro step output PWM frequency is set. After hard reset release (Pin 39 RSTB : Low to High), this setup should be performed before starting to excite and drive a motor (DT1 ends).

DT2A[7:0] (Start point excitation wait, Address 22h)
Updated timing is set. After hard reset release (Pin 39 RSTB : Low → High), this setup should be performed before starting to excite and drive a motor (DT1 ends).

PHMODAB[5:0] (Phase correction, Address 22h)
The correlation phase difference between coil A and B is corrected, and the driving noise is reduced. Since the amount of suitable phase correction depends on the rotation direction or rotation speed, the change of this setup should be performed simultaneously with the changes of the rotations direction (CCWCWAB) or rotation speed (INTCTAB), or it should be performed when a motor does not rotate.

PPWA[7:0]，PPWB[7:0] (Peak pulse width, Address 23h)
PWM maximum duty is set. This setup should be performed before starting to excite and drive a motor (DT1 ends).

PSUMAB[7:0] (Step count number, Address 24h)
The amount of motor rotations in 1 VD interval is set.
Every time VD pulse is input, the motor keeps rotating depending on the amount of rotations. Therefore, set to "0" in order to stop rotation of the motor.
When the amount of rotations which exceeds 1 VD interval is set, the amount of rotations of a part which exceeds 1 VD interval is cancelled.



■ Setup Timing of Each Setup (continued)

CCWCWAB (Rotation direction, Address 24h)
Rotation direction is set. This setup should be performed just before switching the rotation direction.

BRAKEAB (Brake setup, Address 24h)
A current is set to 0 by braking. Since it becomes impossible to get the excitation position of a motor by braking, this setup should not be preformed except for the case of stopping immediately.

ENDISAB (Motor enable/disable setup, Address 24h)
Enable of a motor is set. Since a motor pin is Hi-Z when it is set to "Disable", do not set to "Disable" while a motor keeps rotating.

LEDA (LED setup, Address 24h)
LED ON/OFF is set. The setup is performed at the falling edge of CS.
(It is understood that it is not related to driving a motor. It is possible to turn ON/OFF independently.)

MICROAB[1:0] (Number of sine wave divisions, Address 24h)
Number of sine wave divisions is set. Even if this setup is changed, the amount of rotations and rotation speed do not vary.
If only the control which the number of divisions varies depending on the rotation speed is not performed, the problem dose not occur if it is set once after hard reset release (Pin 39 RSTB : Low → High).

INTCTAB[15:0] (Pulse cycle, Address 25h)
Pulse cycle is set. Rotation speed is determined by this setup.

■ How to adjust register setting for micro stepping motor driver

In order to control lens, it is required to set motor rotation speed and amount of rotation per VD. Register settings relating to speed and amount of rotation are:

INTCTxx[15:0]: set time of each step (that is, the rotation speed)

PSUMxx[7:0]: amount of rotation per VD period

When driving the motor continuously for several VD period, it is best to match rotation time (per VD) to VD period.
Below is a method to calculate INTCTxx[15:0] and PSUMxx[7:0] for smooth motor rotation.

1) Calculate INTCTxx[15:0] from desired rotation speed.

$$INTCTxx[15:0] \times 768 = OSCIN\ frequency / rotation\ frequency$$

2) Calculate PSUMxx[7:0] from INTCTxx[15:0]. Round off if the result of PSUMxx[7:0] is not integer.
When the below equation is satisfied, the rotation time is equal to VD period, and smooth rotation is realized.

$$INTCTxx[15:0] \times PSUMxx[7:0] \times 24 = OSCIN\ frequency / VD\ frequency$$

3) If PSUMxx[7:0] is rounded off, recalculate INTCTxx[15:0] from the equation in 2).

Example) OSCIN frequency = 27 MHz, VD frequency = 60 Hz
Calculate PSUMxx[7:0] and INTCTxx[15:0] to rotate motor at 800 pps (1-2 phase).
800 pps = 100 Hz, so from equation in 1),

$INTCTxx[15:0] = 27\ MHz / (100\ Hz \times 768) = 352$

Next, calculate PSUMxx[7:0] from equation in 2):

$PSUMxx[7:0] = 1/(60\ Hz) \times 27\ MHz / (352 \times 24) = 53$

Since PSUMxx[7:0] is rounded off, recalculate INTCTxx[15:0] from equation in 2):

$INTCTxx[15:0] = 1/(60\ Hz) \times 27\ MHz / (53 \times 24) = 354$

Refer to pages 23 and 28 for detail of PSUMxx[7:0] and INTCTxx[15:0].

If the value of left-hand side in 2) is smaller than right-hand side, the rotation time will be shorter than VD period and will cause discontinuous rotation. If left-hand side is smaller, the rotation time that exceeds 1 VD will be cancelled.

■ Detail descriptions of register

• DT1[7:0] (Start point wait time)

Address			20h			Initial Value		0Ah							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT1[7:0]							

DT1[7:0] sets the delay time (start point wait time) until the data written in the serial data communication sends to the output.
It becomes possible to excite a motor after a start point wait switches "1" to "0". The start point wait starts to count after the rising edge of video sync signal (VD_FZ).

Since start point wait time is the trigger required for data acquisition, be sure to set to other than "0". When the value of register is "0", the data cannot be updated.
Refer to page 10 for the relationship of VD_FZ and start point wait time.

DT1	Start point wait
0	Prohibition
1	303.4 µs
255	77.4 ms
n	n×8192/27 MHz

■ Detail descriptions of register (continued)

• DT2A[7:0] (Start point excitation wait α motor)

Address			22h			Initial Value		03h							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2A[7:0]							

• DT2B[7:0] (Start point excitation wait β motor)

Address			27h			Initial Value		03h							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2B[7:0]							

DT2A[7:0] and DT2B[7:0] set the delay time (start point excitation wait) until α motor and β motor start rotation. Motor rotation starts after start point excitation wait switches "1" to "0". The start point excitation wait starts to count after the falling edge of start point wait.

Since the falling edge is the trigger pulse which is required for data acquisition, be sure to input the data of other than "0". When the value of register is "0", the data cannot be updated.
Refer to page 10 for the relationship of VD_FZ and start point excitation wait time.

Setup value	Start point excitation wait
0	Prohibition
1	303.4 μs
255	77.4 ms
n	n × 8192/27 MHz

■ Detail descriptions of register (continued)

• PWMMODE[4:0] (Micro step output PWM frequency)

Address			20h			Initial Value			1Ch						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			PWMMODE[4:0]												

• PWMRES[1:0] (Micro step output PWM frequency resolution)

Address			20h			Initial Value			1						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	PWMRES														

PWMMODE[4:0] sets the frequency division value of system clock, OSCIN, which is used as the standard of PWM signal for micro step output. PWMMODE[4:0] can set in the range from 1 to 31. PWM frequency at PWMMODE = 0 is the same as that at PWMMODE = 1.

PWMRES[1:0] sets the resolution of frequency division value set by PWMMODE[4:0].

PWM frequency is calculated by the following formula.

$$\text{PWM frequency} = \text{OSCIN frequency} / ((\text{PWMMODE} \times 2^3) \times 2^{\text{PWMRES}})$$

Refer to page 32 for the specific PWM frequency set by PWMMODE[4:0] and PWMRES[1:0] at OSCIN = 27 MHz..

■ Detail descriptions of register (continued)

- PHMODAB[5:0] (Phase correction α motor)

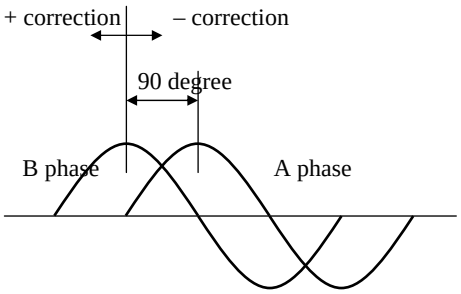
Address			22h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODAB[5:0]													

- PHMODCD[5:0] (Phase correction β motor)

Address			27h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODCD[5:0]													

Current phase differences of α motor and β motor shifts from 90 degree by PHMODAB[5:0] and PHMODCD[5:0] respectively. Setup resolution is 0.7 degree, and data is set in two's complement.

PHMODAB	Amount of phase correction
000000	±0 degree
000001	+0.70 degree
011111	+21.80 degree
100000	−22.50 degree
111111	−0.70 degree
Resolution	360 degree /512＝0.70 degree



Stepping motor is configured so that phase difference between coils becomes 90 degree. However, the phase difference may shift from 90 degree due to the variation of a motor.
Therefore, even if phase difference in current waveform is exactly 90 degree, driving noise may occur due to the occurrence of rotation torque ripple.
This setup is for reducing the torque ripple which is occurred by the variation of a motor.

■ Detail descriptions of register (continued)

- PPWA[7:0] (Driver A peak pulse width)
- PPWB[7:0] (Driver B peak pulse width)

Address			23h			Initial Value			0, 0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWB[7:0]								PPWA[7:0]							

- PPWC[7:0] (Driver C peak pulse width)
- PPWD[7:0] (Driver D peak pulse width)

Address			28h			Initial Value			0, 0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWD[7:0]								PPWC[7:0]							

PPWA[7:0] to PPWD[7:0] set the maximum duty of PWM at the position which the currents in driver A to D are peak value respectively. The maximum duty is calculated by the following formula.

$$\text{Driver X Maximum duty} = PPWx / (PWMMODE \times 8)$$

When PPWx = 0 is set, coil current becomes 0.

Refer to page 34 for the operation at the time when the duty exceeding 100% is set.

Example) When PPWA[7:0] = 200, PWMMODE[4:0] = 28 is set, maximum duty of driver A will be

$200 / (28 \times 8) = 0.89$

■ Detail descriptions of register (continued)

- PSUMAB[7:0] (α motor step count number)

Address			24h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMAB[7:0]							

- PSUMCD[7:0] (β motor step count number)

Address			29h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMCD[7:0]							

PSUMAB[7:0] and PSUMCD[7:0] set the number of step counts of α motor and β motor respectively.
Since the number of setup step counts is converted to 256-step inside, the amount of rotation becomes the same regardless of the number of divisions.

To stop the rotation of a motor, set PSUMxx[7:0] = 0.

Setting value	Number of steps		
	64-step conversion	128-step conversion	256-step conversion
0	0	0	0
1	2	4	8
255	510	1 020	2 040
n	2n	4n	8n

If maximum duty is set to other than "0" at PSUMxx[7:0] = 0, the position is held in the state of excitation.
If a motor can hold the position by cogging torque without motor current, the position is held even if the maximum duty is set to 0.

Example) When PSUMAB[7:0] = 8 is set, the amount of rotation is 16 steps (64-step conversion). This is 16/64 = 1/4 of a sine wave. The amount of rotation becomes 1/4 of a sine wave also in 128 and 256-step conversion.

■ Detail descriptions of register (continued)

• CCWCWAB (α motor rotation direction)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						CCWCWAB									

• CCWCWCD (β motor rotation direction)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						CCWCWCD									

CCWCWAB and CCWCWCD set the rotation direction of α motor and β motor respectively.
Refer to page 35 for the definition of rotation direction.

Setup value	Motor rotation direction
0	Forward
1	Reverse

■ Detail descriptions of register (continued)

• BRAKEAB (α motor brake)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKEAB									

• BRAKECD (β motor brake)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKECD									

BRAKEAB and BRAKECD set the brake mode of α motor and β motor respectively.

Setup value	α motor brake
0	Normal operation
1	Brake mode

Both of upper-side P-ch MOSs of output H bridge turn on in brake mode. The brake mode is not used in normal operation, and is used for emergency shutdown. It is recommended to use only in abnormal state.

■ Detail descriptions of register (continued)

• ENDISAB (α motor Enable/Disable)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISAB										

• ENDISCD (β motor Enable/Disable)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISCD										

ENDISAB and ENDISCD configure the setting for output stage control of α motor and β motor respectively.
The output becomes the state of OFF (Hi-Z) at ENDISxx = 0. However, internal excitation position counter keeps counting even ENDISxx = 0. Therefore, when stopping the motor during normal operation, set PSUMxx[7:0] = 0 (not ENDISxx = 0).

Setup value	Motor output condition
0	Output OFF (Hi-Z)
1	Output ON

■ Detail descriptions of register (continued)

• MICROAB[1:0] (α motor quasi-sin wave division number)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROAB													

• MICROCD[1:0] (β motor quasi-sine wave division number)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROCD													

MICROAB[1:0] and MICROCD[1:0] set the number of quasi-sine wave divisions for α motor and β motor respectively. Waveform example for 64 divisions is on page 35.

MICROAB	Number of divisions
00	256
01	256
10	128
11	64

■ Detail descriptions of register (continued)

• INTCTAB[15:0] (α motor step cycle setup)

Address			25h			Initial Value			0080h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTAB[15:0]															

• INTCTCD[15:0] (β motor step cycle setup)

Address			2Ah			Initial Value			0080h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTCD[15:0]															

INTCTAB[15:0] and INTCDCD[15:0] set the step cycle of α motor and β motor respectively. Since the step cycle is converted to 64-step inside, motor rotation speed becomes the same regardless of the number of divisions set by MICROxx[1:0].

Setup value	Step cycle		
	64-step	128-step	256-step
0	0	0	0
1	444 ns	222 ns	111 ns
Max	29.1 ms	14.6 ms	7.3 ms
n	12n/27 MHz	6n/27 MHz	3n/27 MHz

If maximum duty is set to other than "0" at INTCTxx[15:0] = 0, the position is held in the state of excitation.
If a motor can hold the position by cogging torque without motor current, the position is held even if the maximum duty is set to 0.

e. g.) If ITCTAB[15:0] = 400 is set, time of 1 step for 64-step is

$12 \times 400 / 27\ \text{MHz} = 0.178\ \text{ms}$

Therefore, period of one sinusoidal wave cycle is 11.4 ms (87.9 Hz).
This is the same for 128-step and 256-step.

■ Detail descriptions of register (continued)

- FZTEST[4:0] (Test signal output setup)

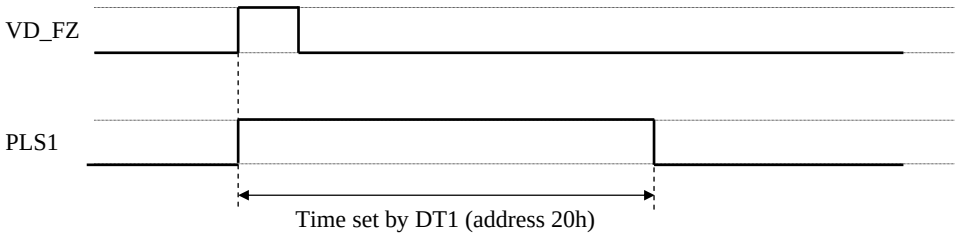
Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											FZTEST[4:0]				

FZTEST[4:0] makes a choice of the test signal which is output to PLS1 and PLS2 pins.
TESTEN1 (0Bh) and TESTEN2 (21h) should be set to "1" in order to enable the test signal.
Since the test signal used in our company is output, do not set other than the setups described in the following table.

Setup value	Step cycle		Description
	PLS1	PLS2	
0	PLS1	PLS2	Pulse 1/2 normal function
1	Start point wait	0	“H” output during start point wait
2	Start point excitation wait A	Start point excitation wait B	“H” output during start point excitation wait
3	ENDISAB	ENDISCD	ENDISxx setting
4	CCWCWAB	CCWCWCD	CCWCWxx setting
5	Pulse output monitor A	Pulse output monitor B	During motor rotation, “H”/”L” changes at the speed of 64-step
6	PWM cycle monitor	0	PWM frequency signal for micro step
7	Pulse completion output A	Pulse completion output B	“H” output during motor rotation

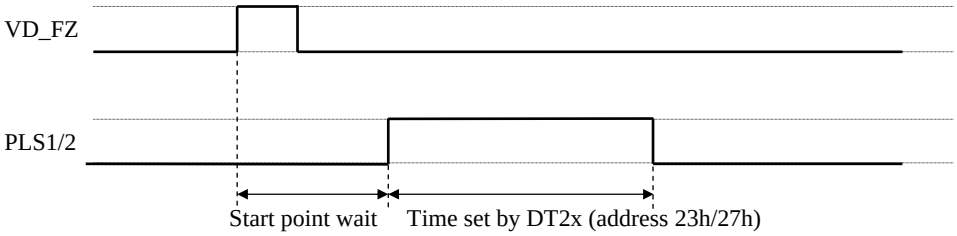
Waveform for each test signal is described below.

Start point wait

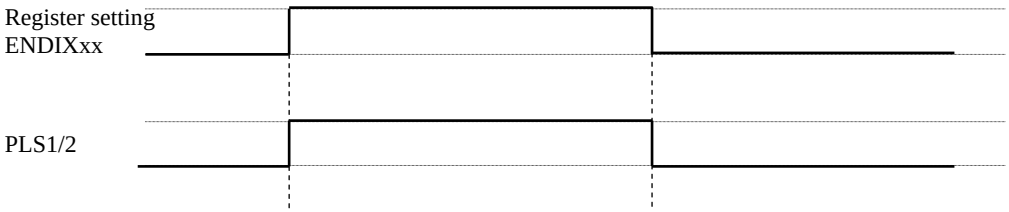


■ Detail descriptions of register (continued)

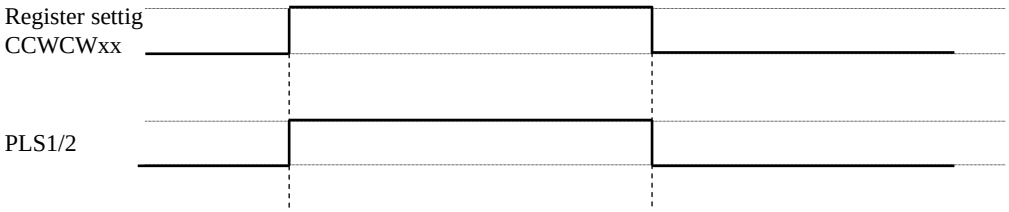
Start point excitation wait



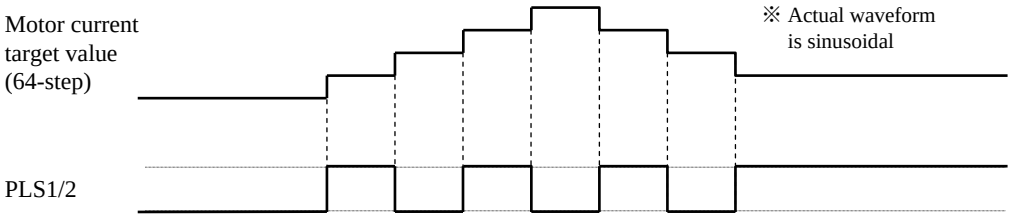
ENDISxx



CCWCWxx



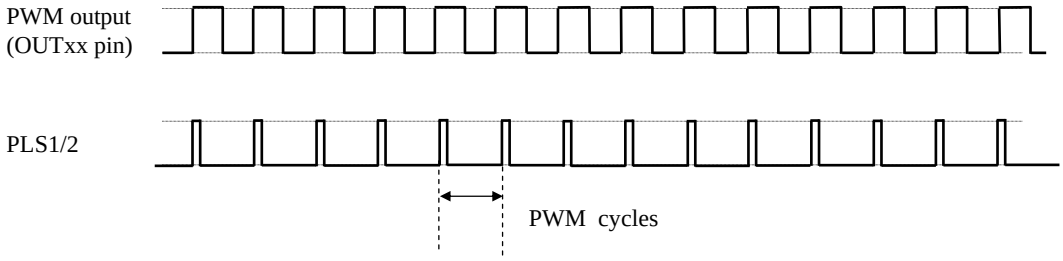
Pulse output monitor



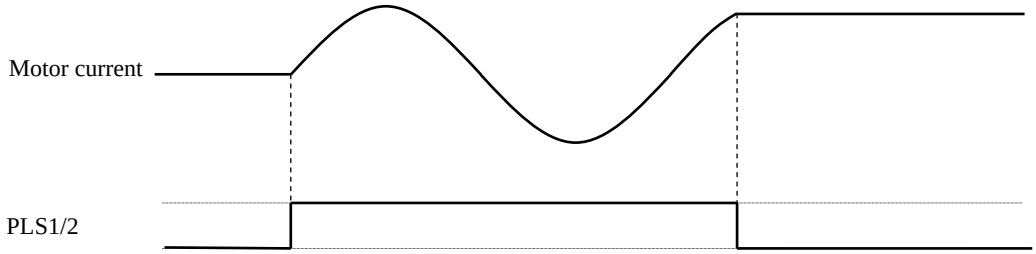
For 128-step and 256-step, “H”/“L” of PLS1/2 changes every 2 and 4 steps respectively.

■ Detail descriptions of register (continued)

PWM cycle monitor



Pulse completion output



• TESTEN1 (Test setting 1)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN1							

• TESTEN2 (Test setting 2)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN2							

By setting TESTEN1=TESTEN2=1, above PLS1(37pin) and PLS2(38pin) test signal output is available.
Also, some settings can be used.

■ PWM frequency setup

PWM frequency for OSCIN = 27 MHz is shown in below table.

PWMMODE	PWMRES		
	0	1	2
1	3375.0	1687.5	843.8
2	1687.5	843.8	421.9
3	1125.0	562.5	281.3
4	843.8	421.9	210.9
5	675.0	337.5	168.8
6	562.5	281.3	140.6
7	482.1	241.1	120.5
8	421.9	210.9	105.5
9	375.0	187.5	93.8
10	337.5	168.8	84.4
11	306.8	153.4	76.7
12	281.3	140.6	70.3
13	259.6	129.8	64.9
14	241.1	120.5	60.3
15	225.0	112.5	56.3
16	210.9	105.5	52.7
17	198.5	99.3	49.6
18	187.5	93.8	46.9
19	177.6	88.8	44.4
20	168.8	84.4	42.2
21	160.7	80.4	40.2
22	153.4	76.7	38.4
23	146.7	73.4	36.7
24	140.6	70.3	35.2
25	135.0	67.5	33.8
26	129.8	64.9	32.5
27	125.0	62.5	31.3
28	120.5	60.3	30.1
29	116.4	58.2	29.1
30	112.5	56.3	28.1
31	108.9	54.4	27.2

(kHz)

■ PWM frequency setup and Maximum duty setup

The setups method example of PWM frequency and maximum duty are shown as follows.

- PWM frequency setup

PWM frequency is calculated by the following formula with PWMMODE[4:0] and PWMRES[1:0] as shown in page 20 of this book.

$$\text{PWM frequency} = \text{OSC frequency} / ((\text{PWMMODE} \times 2^3) \times 2^{\text{PWMRES}})$$

PWM frequency corresponding to the each setup value of PWMMODE and PWMRES is shown in page 28 of this book. Note that there may be two kinds of combination of the setup value corresponding to PWM frequency. For example, there are two kinds of setup to realize that PWM frequency is 56.3 kHz.

PWMMODE = 30, PWMRES = 1

PWMMODE = 15, PWMRES = 2

In such a case, PWMMODE should be set so that it is a larger value as described hereinbelow.

- Maximum duty setup

PWM output maximum duty is calculated by the following formula as shown in page 22 of this book.

$$\text{Maximum duty} = \text{PPWx} / (\text{PWMMODE} \times 8)$$

For example, when PWM frequency is set as follows,

PWMMODE = 30, PWMRES = 1 → PWM frequency = 56.3 kHz

maximum duty becomes the following value by setting to PPWx = 200.

200 / (30 × 8) = 0.83

Since resolution of sine wave amplitude is determined by PPW setup, PWMMODE should be also set to as large a value as possible so that PPW becomes as large as possible.

■ Peak duty setup which exceeds 100%

PWM maximum duty at peak position of micro step current is determined by PWMMODE[4:0] and PPWx[7:0].

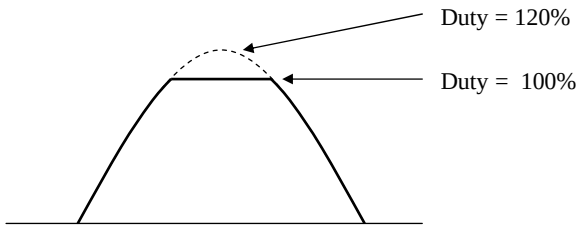
$$\text{Maximum duty} = \text{PPWx} / (\text{PWMMODE} \times 8)$$

Maximum duty may exceed 100% depending on the setup values of PWMMODE and PPWx.
Since the duty does not certainly exceed 100% at PWM operation in this case, the peak point of sine wave (current waveform) becomes flat as follows.

Example 1） When PWMMODE＝10, PPWx＝96,

Maximum duty = 96 / (10 × 8) ＝120%

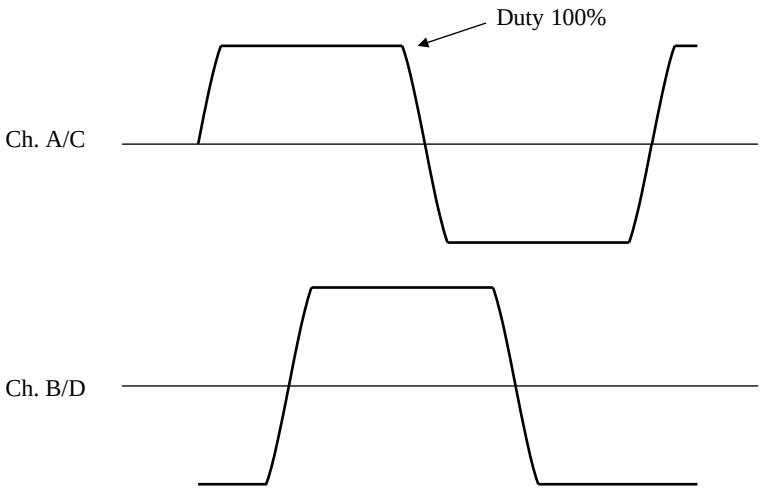
The target current waveform is indicated as the following full line.



Example 2） When PWMMODE = 5, PPWx = 255,

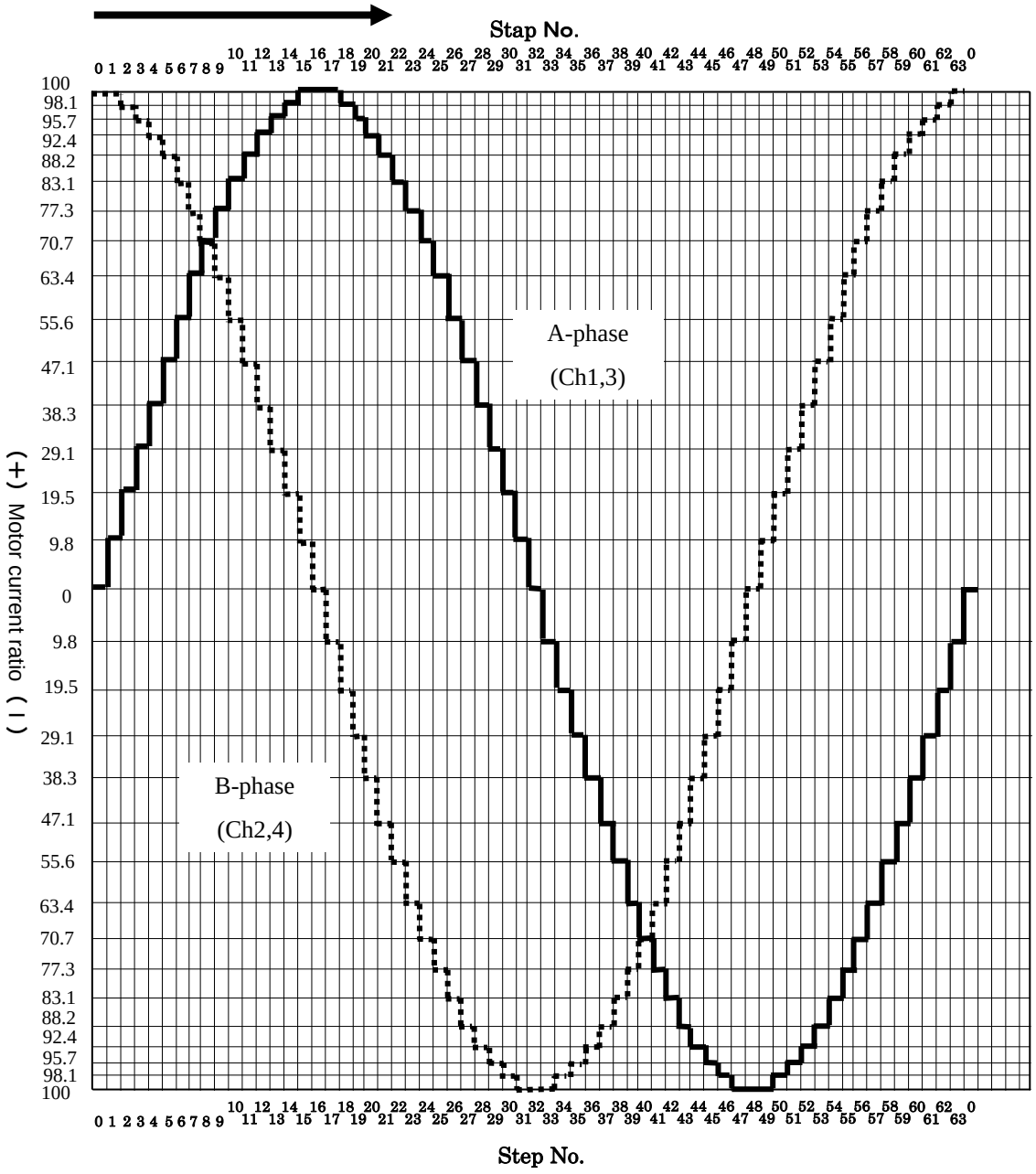
Maximum duty = 255 / (5 × 8) = 638%

The target current waveform becomes close to 2-phase drive.



Micro step drive (64-step)

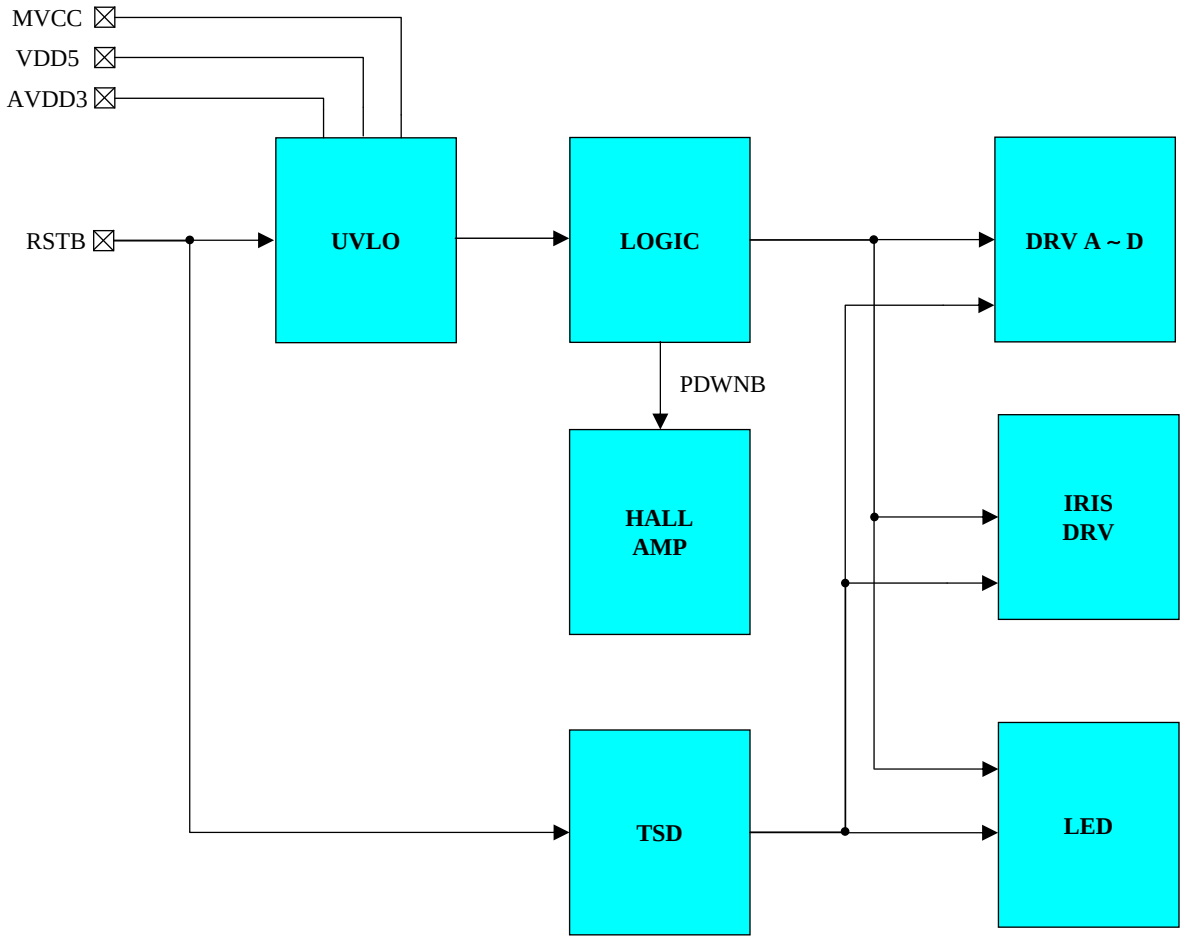
(1) Forward rotation



The direction of current which flows into OUTx2 pin from OUTx1 pin is defined as positive direction.

Reset / Protection circuit

■ Block Diagram / Specifications



Stop direction (Enable → Disable) is shown as above. The specifications are shown as follows.

	COMMON	HALL_AMP	FZ output	Iris output	LED
RSTB pin	Disable	Logic reset → Disable	Logic reset → Output OFF		
Thermal shutdown (TSD)	×	×	Output OFF		
Under-voltage lock-out (UVLO)	×	Logic reset → Disable	Logic reset → Output OFF		

※Note 1 ×: Don't care

※Note 2 The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to V_{CC} short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

■Electrical Characteristics (Reference values for design) at AVDD5, MVCCx = 4.8 V, DVDD, AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

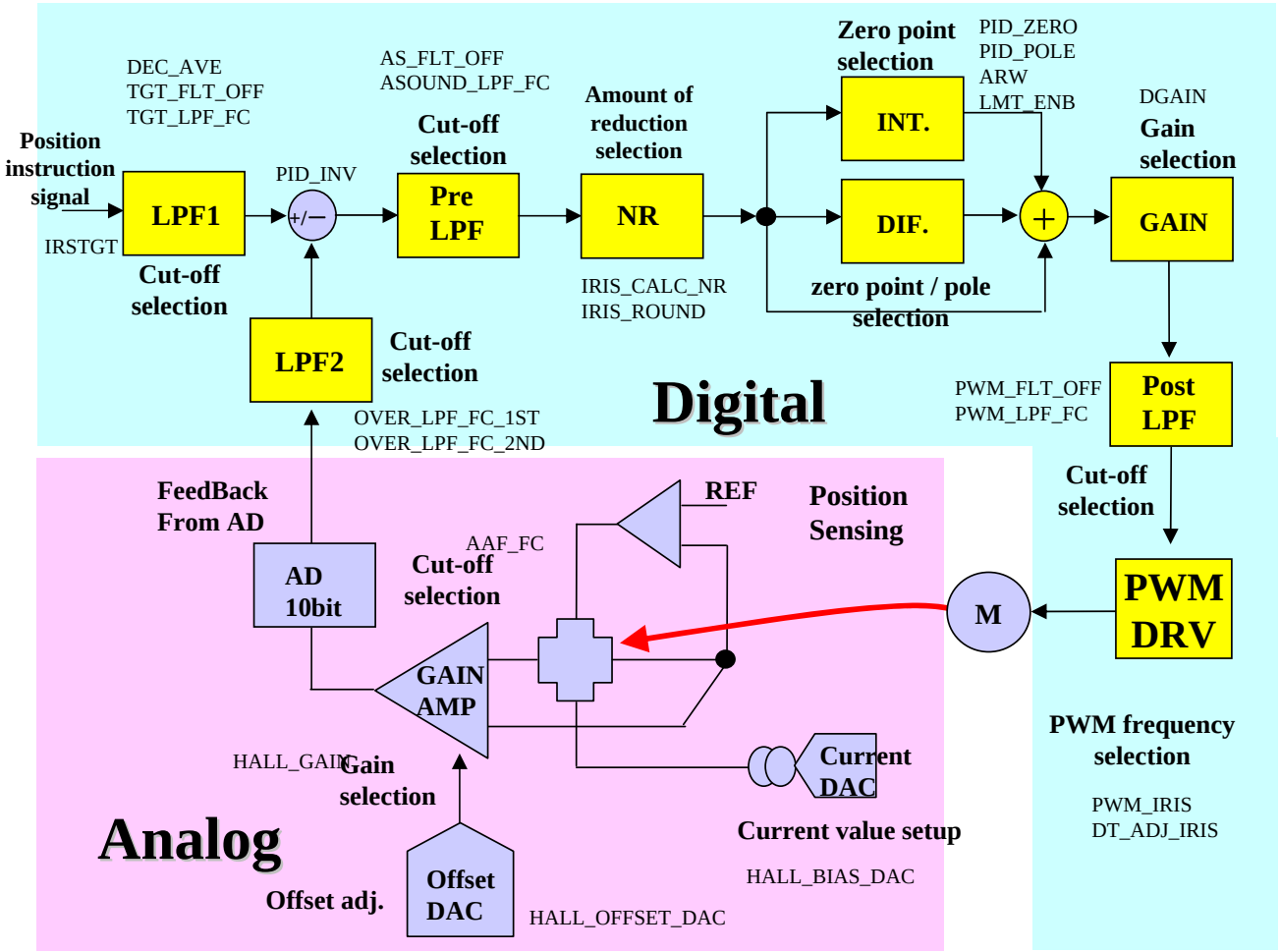
No.	Parameter	Symbol	Conditions	Reference values			Unit
				Min	Typ	Max	
Thermal shutdown							
1	Thermal shutdown circuit Operating temperature	Ttsd	—	—	150	—	°C
2	Thermal shutdown circuit Hysteresis width	DTtsd	—	—	40	—	°C
Power supply voltage monitor circuit							
3	3.3 V Reset operation	Vrston	—	—	2.27	—	V
4	3.3 V Reset hysteresis width	Vrsthys	—	—	0.2	—	V
5	MVCCx Reset operation	$V_{rstFZon}$	—	—	2.2	—	V
6	MVCCx Reset hysteresis width	$V_{rstFZhys}$	—	—	0.2	—	V
7	VDD5 Reset operation	$V_{rstISon}$	—	—	2.2	—	V
8	VDD5 Reset hysteresis width	$V_{rstIShys}$	—	—	0.2	—	V
Digital input							
9	High-level input threshold voltage	$V_{in(H)}$	—	—	1.36	—	V
10	Low-level input threshold voltage	$V_{in(L)}$	—	—	1.02	—	V
11	Input hysteresis width	Vhysin	—	—	0.34	—	V
12	Input pull-down resistance	$R_{pullret}$	—	—	100	—	kΩ

Iris control

■ Features

- PWM drive → Low power consumption
- Each filter can be set by serial input. → Low noise drive
- Build-in passive parts around a gain amplifier → Reduction of external parts
- Built-in 8-bit DAC for adjusting hall offset
- Built-in current DAC for adjusting hall bias

■ Block Diagram



■Electrical Characteristics at AVDD5, MVCCx = 4.8 V, DVDD, AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.

No.	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Motor driver (Iris)							
1	H bridge ON resistance	R_{onIR}	IM = 50 mA	—	—	5	Ω
2	H bridge leak current	I_{leakIR}	—	—	—	0.8	mA
OPAMP3 (Hall Sensor Amp. for output amplification)							
3	Input voltage range	V_{IN}	—	½ AVDD3 – 0.5	½ AVDD3	½ AVDD3 + 0.5	V
4	Input offset voltage	V_{OF}	—	– 15	—	15	mV
5	Output voltage Low-level	V_{OL}	ILOAD = – 100 mA	0	0.1	0.2	V
6	Output voltage High-level	V_{OH}	ILOAD = 100 mA	AVDD3 – 0.2	AVDD3 – 0.1	AVDD3	V
7	Gain	V_{OG}	Setup value of gain : 0h	20.8	21.9	23	V/V
OPAMP4 (Hall Sensor Amp. for eliminating common-mode voltage)							
8	Input voltage range	V_{IN}	—	½AVDD3 – 0.1	½ AVDD3	½AVDD3 + 0.1	V
9	Input offset voltage	V_{OF}	—	– 10	—	10	mV
10	Output voltage Low-level	V_{OL}	ILOAD = – 10 mA	0	0.1	0.2	V
11	Output voltage High-level	V_{OH}	ILOAD = 3 mA	AVDD3 – 0.5	AVDD3 – 0.2	AVDD3	V
Reference voltage output block							
12	Output voltage 1	VREF	ILOAD = 0 A, CVREF = 100 pF	½ AVDD3 – 0.1	½ AVDD3	½ AVDD3 + 0.1	V
13	Output voltage 2	VREFL	ILOAD = ± 100 mA, CVREF = 100 pF	VREF – 0.1	VREF	VREF + 0.1	V
Hall bias control block (SENS pin output)							
14	Minimum output current	IBL	REF = 10 kΩ, SENS = 0.7 V Setup value : 00 h	—	0	0.1	mA
15	Output current precision 1	IB40H	REF = 10 kΩ, SENS = 0.7 V Setup value : 40 h	0.91	1.02	1.13	mA
16	Output current precision 2	IBBFH	REF = 10 kΩ, SENS = 0.7 V Setup value : BE h	2.69	3.02	3.35	mA

■ Detail descriptions of register

- IRSTGT[9:0] (Iris desired value)

Address			00h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						IRSTGT[9:0]									

IRSTGT[9:0] sets the desired value of ADC input for using in Iris control block.

Setup value	AD input desired value
0	AVDD3 × 0/1023
1	AVDD3 × 1/1023
1023	AVDD3 × 1023/1023
n	AVDD3 × n/1023

■ Detail descriptions of register (continued)

• OVER_LPF_FC_1ST[1:0] (ADC feedback filter (1) cut-off frequency)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												OVER_LPF_FC_1ST[1:0]			

LPF(1) cut-off frequency in AD feedback block is set.
Lower cut-off frequency is more effective to remove noise from ADC.
Basically, use OVER_LPF_FC_1ST[1:0] = 0.

Setup value	Cut-off frequency
0	2 600 Hz
1	3 600 Hz
2	5 200 Hz
3	8 000 Hz

• OVER_LPF_FC_2ND[1:0] (ADC feedback filter (2) cut-off frequency)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											OVER_LPF_FC_2ND[1:0]				

LPF(2) cut-off frequency in AD feedback block is set.
Lower cut-off frequency is more effective to remove noise from ADC.
Basically, use OVER_LPF_FC_2ND[1:0] = 0.

Setup value	Cut-off frequency
0	2 600 Hz
1	3 600 Hz
2	5 200 Hz
3	8 000 Hz

■ Detail descriptions of register (continued)

• DEC_AVE (Moving average of iris target)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										DEC_AVE					

Moving average of target value for Iris is set.
Iris target changes more smoothly with larger moving average.
Basically, use DEC_AVE = 0.

Setup value	Moving average
0	8
1	4

• AS_FLT_OFF (Filter before PID controller enable / disable)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									AS_FLT_OFF						

Whether filtering-function before PID controller is enabled or disabled is set.
When the function is enabled, LPF is inserted to the controller.
LPF removes noise that reaches PID controller, so basically set AS_FLT_OFF = 0.
If phase margin in closed-loop frequency characteristic is not enough, iris may have a ringing when iris target changes. In that case, setting AS_FLT_OFF = 1 will improve phase margin and may prevent ringing.

Setup value	Filter before PID
0	Enable
1	Disable

■ Detail descriptions of register (continued)

- ASOUND_LPF_FC[2:0] (Filter cut-off frequency before PID controller)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							ASOUND_LPF_FC[2:0]								

Filter cut-off frequency before PID controller is set.
Lower cut-off frequency is more effective to remove noise to PID controller.
Basically, use ASOUND_LPF_FC[2:0] = 0.
If phase margin in closed-loop frequency characteristic is not enough, iris may have a ringing when iris target changes. In that case, setting higher cut-off frequency will improve phase margin and may prevent ringing.

Setup value	Cut-off frequency
0	900 Hz
1	1 300 Hz
2	1 600 Hz
3	2 000 Hz
4	2 600 Hz
5	3 200 Hz
6	4 000 Hz
7	禁止

- DGAIN[6:0] (PID controller digital gain)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DGAIN[6:0]															

Digital gain of PID controller is set. The setup gain is defined as the gain between AD input at 35 Hz and motor input under the conditions of PID zero point = 35 Hz, pole = 900 Hz, PWM frequency = 31.25 kHz.
Refer to the next page for the details of setup value.

Setup value	Gain
00h	0
01h ~ 7Fh	{ 0.125 × { 2^(MSB 3 bit – 3'd3)} × [16 + LSB 4 bit] } + 3 dB

■ Register bit epexegesis (Gain table)

DGAIN[3:0]	DGAIN[6:4]															
	000		001		010		011		100		101		110		111	
	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB
0h	0	-	0.5	– 3.0	1	3.0	2	9.0	4	15.0	8	21.1	16	27.1	32	33.1
1h	0.265625	– 8.5	0.53125	– 2.5	1.0625	3.5	2.125	9.5	4.25	15.6	8.5	21.6	17	27.6	34	33.6
2h	0.28125	– 8.0	0.5625	– 2.0	1.125	4.0	2.25	10.0	4.5	16.1	9	22.1	18	28.1	36	34.1
3h	0.296875	– 7.5	0.59375	– 1.5	1.1875	4.5	2.375	10.5	4.75	16.5	9.5	22.6	19	28.6	38	34.6
4h	0.3125	– 7.1	0.625	– 1.1	1.25	4.9	2.5	11.0	5	17.0	10	23.0	20	29.0	40	35.0
5h	0.328125	– 6.7	0.65625	– 0.7	1.3125	5.4	2.625	11.4	5.25	17.4	10.5	23.4	21	29.4	42	35.5
6h	0.34375	– 6.3	0.6875	– 0.3	1.375	5.8	2.75	11.8	5.5	17.8	11	23.8	22	29.8	44	35.9
7h	0.359375	– 5.9	0.71875	0.1	1.4375	6.2	2.875	12.2	5.75	18.2	11.5	24.2	23	30.2	46	36.3
8h	0.375	– 5.5	0.75	0.5	1.5	6.5	3	12.5	6	18.6	12	24.6	24	30.6	48	36.6
9h	0.390625	– 5.2	0.78125	0.9	1.5625	6.9	3.125	12.9	6.25	18.9	12.5	24.9	25	31.0	50	37.0
Ah	0.40625	– 4.8	0.8125	1.2	1.625	7.2	3.25	13.2	6.5	19.3	13	25.3	26	31.3	52	37.3
Bh	0.421875	– 4.5	0.84375	1.5	1.6875	7.5	3.375	13.6	6.75	19.6	13.5	25.6	27	31.6	54	37.6
Ch	0.4375	– 4.2	0.875	1.8	1.75	7.9	3.5	13.9	7	19.9	14	25.9	28	31.9	56	38.0
Dh	0.453125	– 3.9	0.90625	2.1	1.8125	8.2	3.625	14.2	7.25	20.2	14.5	26.2	29	32.2	58	38.3
Eh	0.46875	– 3.6	0.9375	2.4	1.875	8.5	3.75	14.5	7.5	20.5	15	26.5	30	32.5	60	38.6
Fh	0.484375	– 3.3	0.96875	2.7	1.9375	8.7	3.875	14.8	7.75	20.8	15.5	26.8	31	32.8	62	38.8

Example) Gain for DGAIN[6:0] is 13.2 dB.

■ Detail descriptions of register (continued)

• IRIS_CALC_NR[3:0] (PID controller integral error cumulative prevention level)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												IRIS_CALC_NR[3:0]			

Error accumulation prevention level of PID controller integrator is set. When the function is enabled, error accumulation generated by integration in the PID controller can be decreased. However, the integral function may fall. Basically use IRIS_CALC_NR[3:0] = 0.

Setup value	Error accumulation prevention level
0	Disable
1 to 14	$\pm 1/2^{(15-n)}$ LSB
15	± 1 LSB

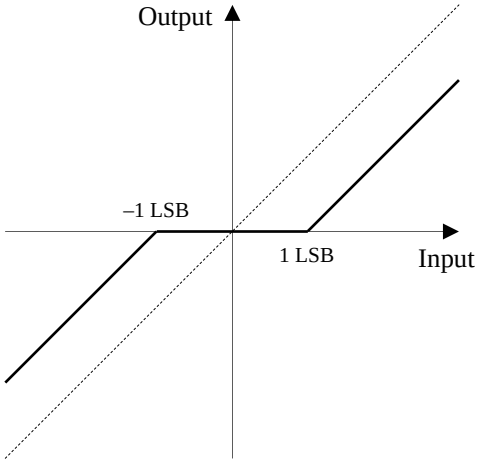
• IRIS_ROUND[3:0] (PID controller differential error cumulative prevention level)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								IRIS_ROUND[3:0]							

Noise respondence prevention level of PID controller differentiator is set. When the function is enabled, the amplitude of noise generated by differentiation in the PID controller can be decreased. However, the differential function may fall.

Setup value	Error accumulation prevention level
0	Disable
1 to 14	$\pm 1/2^{(15-n)}$ LSB
15	± 1 LSB

Figure on right shows the basic concept of above function.
When maximum value is set, input signal smaller than ± 1 LSB is ignored.



■ Detail descriptions of register (continued)

• PID_ZERO[3:0] (PID controller zero point)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				PID_ZERO[3:0]											

Zero point of PID controller is set.

• PID_POLE[3:0] (PID controller pole)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PID_POLE[3:0]															

Pole of PID controller is set.

Setup value	Zero point
0	10 Hz / 10 Hz
1	15 Hz / 15 Hz
2	20 Hz / 20 Hz
3	25 Hz / 25 Hz
4	30 Hz / 30 Hz
5	35 Hz / 30 Hz
6	35 Hz / 35 Hz
7	40 Hz / 35 Hz
8	40 Hz / 40 Hz
9	45 Hz / 45 Hz
10	50 Hz / 50 Hz
11	55 Hz / 55 Hz
12	60 Hz / 60 Hz
13	65 Hz / 65 Hz
14	70 Hz / 70 Hz
15	75 Hz / 75 Hz

Setup value	Pole
0	710 Hz
1	790 Hz
2	870 Hz
3	950 Hz
4	1 040 Hz
5	1 120 Hz
6	1 200 Hz
7	1 280 Hz
8	1 370 Hz
9	1 450 Hz
10	1 530 Hz
11	1 620 Hz
12	1 700 Hz
13	1 790 Hz
14	1 870 Hz
15	1 960 Hz

■ Detail descriptions of register (continued)

• ARW[3:0]

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												ARW[3:0]			

Number of bits in PID integrator is set. It affects the recovery time from saturation in the PID integrator.

Setup value	Number of bits in integrator
0 to 3	12-bit
4 to 14	(15 – setup value)-bit
15	1-bit

• LMT_ENB

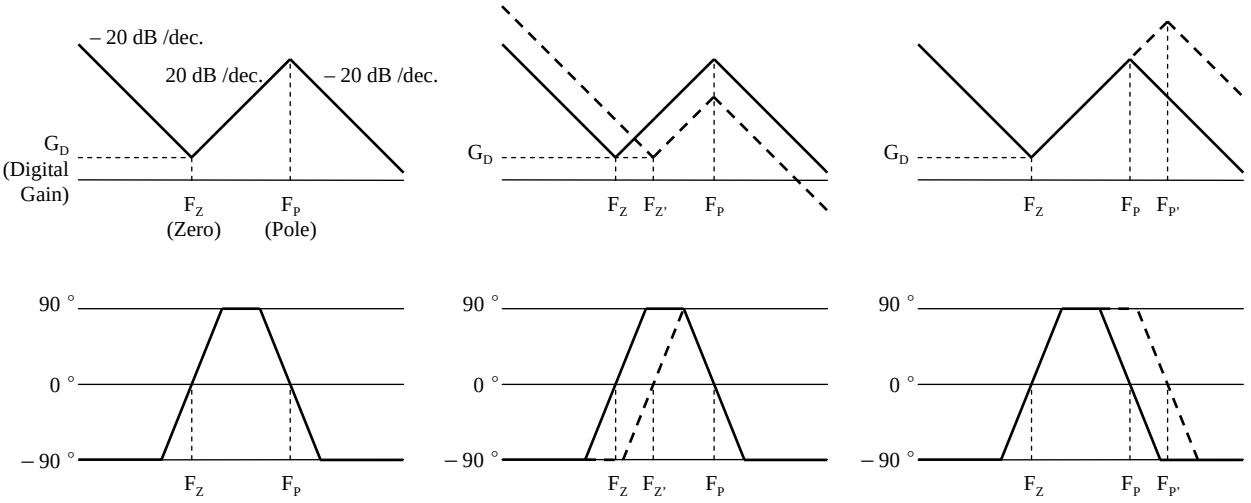
Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											LMT_ENB				

Integral stop function in PID output is enabled / disabled. It affects the recovery time from saturation in the PID output.

Setup value	Integral stop function
0	Disable
1	Enable

■ Detail descriptions of register (continued)

The characteristic of PID controller, and the effect of changing PID_ZERO[3:0] and PID_POLE[3:0] is shown below (Bode diagram).



Bode diagram of PID controller

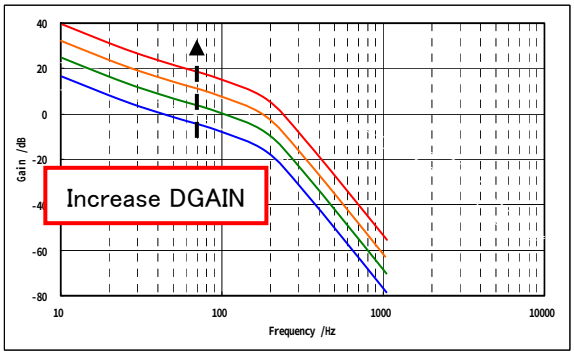
Changing zero from F_Z to $F_{Z'}$

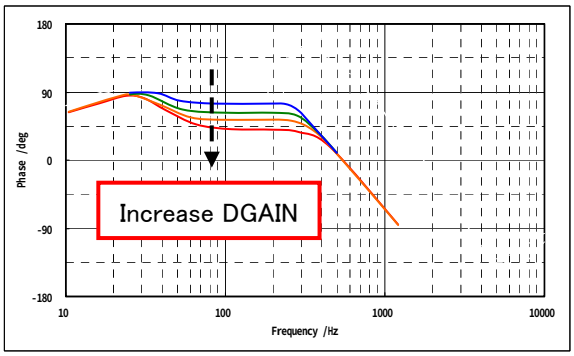
Changing pole from F_P to $F_{P'}$

G_D: DGAIN[6:0]
F_Z: PID_ZERO[3:0]
F_P: PID_POLE[3:0]

■ Detail descriptions of register (continued)

When DGAIN[6:0] is increased, phase margin around 10 to 300 Hz becomes smaller.

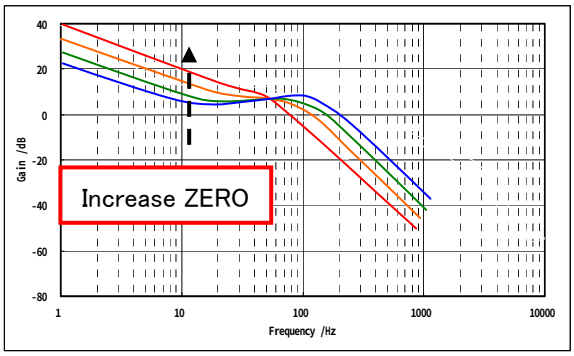


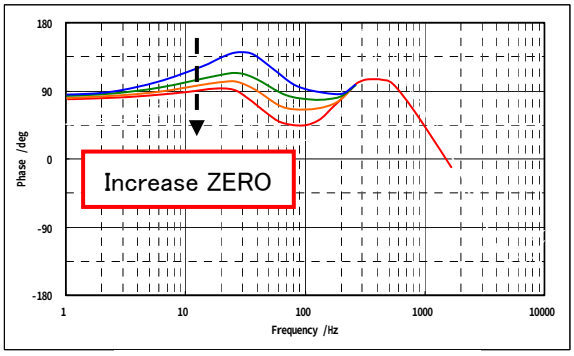


※ Above is a conceptual diagram

When ZERO[3:0] is increased, phase margin around 10 to 300 Hz becomes smaller.

To ensure phase margin by adjusting ZERO[3:0], usage of FRA (Frequency Response Analyzer) is required.





※ Above is a conceptual diagram

■ Detail descriptions of register (continued)

• PWM_FLT_OFF

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										PWM_FLT_OFF					

Whether filtering function after PID controller is enabled or disabled is set. When the function is enabled, LPF is inserted to the controller.
LPF removes noise coming out from PID controller, so basically set PWM_FLT_OFF = 0.
If phase margin in closed-loop frequency characteristic is not enough, iris may have a ringing when iris target changes. In that case, setting PWM_FLT_OFF = 1 will improve phase margin and may prevent ringing.

Setup value	Filter after PID
0	Enable
1	Disable

• PWM_LPF_FC[2:0]

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							PWM_LPF_FC[2:0]								

Cut-off frequency after PID controller is set.
Lower cut-off frequency is more effective to remove noise to PID controller.
Basically, use PWM_LPF_FC[2:0] = 0.
If phase margin in closed-loop frequency characteristic is not enough, iris may have a ringing when iris target changes. In that case, setting higher cut-off frequency will improve phase margin and may prevent ringing.

Setup value	Cut-off frequency (Hz)
0	900
1	1 300
2	1 600
3	2 000
4	2 600
5	3 200
6	4 000
7	Prohibition

■ Detail descriptions of register (continued)

• PWM_IRIS[2:0]

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				PWM_IRIS[2:0]											

PWM frequency of Iris block is set.

Setup value	PWM frequency (kHz)
0	26
1	31.25
2	62.5
3	93.75
4	125
5	150
6	187.5
7	210

• DT_ADJ_IRIS[1:0]

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		DT_ADJ_IRIS[1:0]													

Dead time correction amount of Iris block is set.

Setup value	Dead time correction amount
0	Standard correction
1	Standard correction – 1
2	Standard correction – 2
3	No correction

■ Detail descriptions of register (continued)

• TGT_LPF_FC[1:0]

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												TGT_LPF_FC[3:0]			

Cut-off frequency of input filter of instruction value for Iris is set.
Lower cut-off frequency makes iris target to change more smoothly, and cuts down acoustic noise.
Especially when cut-off frequency is lower than VD frequency, almost no step change appears. But iris target change may slightly delay.

Setup value	Cut-off frequency
0	325 Hz
1	650 Hz
2	1 300 Hz
3	2 600 Hz
4	40 Hz
5	50 Hz
6	63 Hz

Setup value	Cut-off frequency
7	80 Hz
8	100 Hz
9	125 Hz
10	160 Hz
11	200 Hz
12	250 Hz
—	—

• TGT_FLT_OFF

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											TGT_FLT_OFF				

Whether filtering-function of instruction value for Iris is enabled or disabled is set.
When the function is enabled, LPF is inserted to between instruction value input and deviation calculator.

Setup value	Iris target filter
0	Enable
1	Disable

■ Detail descriptions of register (continued)

• PID_INV

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										PID_INV					

PID control polarity is inverted.

Setup value	PID control polarity
0	Non-inverting
1	Inverting

■ Detail descriptions of register (continued)

• START1[7:0] (Pulse 1 start position)

Address			06h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						START1[9:0]									

• WIDTH1[9:0] (Pulse 1 width)

Address			07h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				WIDTH1[11:0]											

• P1EN (Pulse 1 output)

Address			07h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
P1EN															

Refer to the next page for the details of function.

■ Detail descriptions of register (continued)

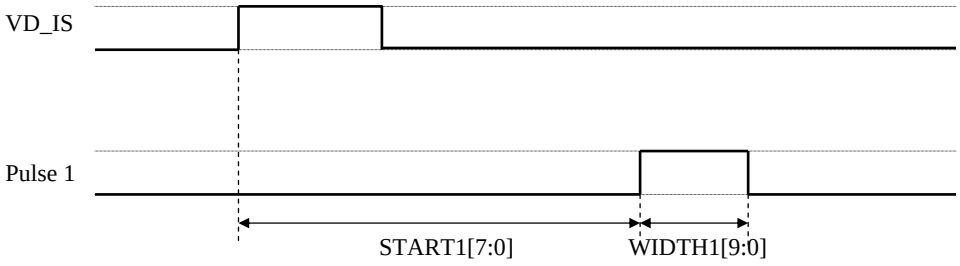
START1[7:0] , WIDTH1[9:0], and P1EN set the pulse output (pulse 1) for strobe.

START1[7:0] sets the start time of pulse 1. The count of start time starts from the rising edge of video sync signal (VD_IS), and continues until the setup time.

WIDTH1[9:0] sets the width of pulse 1. The count of pulse width starts in synchronization with the end of count of start time, and continues until the setup time.

P1EN controls the output of pulse 1.

When any of START1[7:0], WIDTH1[9:0], and P1EN is "0", pulse 1 is not output.



START1	Start time
0	0
1	20.1 µs
n	n × (68/3.375) µs
1023	20.56 ms

WIDTH1	Pulse width
0	0
1	1.19 µs
n	n × (4/3.375) µs
4095	4.87 ms

■ Detail descriptions of register (continued)

• START2[8:0] (Pulse 2 start position)

Address			08h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						START2[9:0]									

• WIDTH2[5:0] (Pulse 2 width)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										WIDTH2[5:0]					

• P2EN (Pulse 2 output)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
P2EN															

Refer to the next page for the details of functions.

■ Detail descriptions of register (continued)

START2[8:0], WIDTH2[5:0], and P2EN set the pulse output (pulse 2) for Iris full-close.

START2[8:0] sets the start time of pulse 2. The count of start time starts from the rising edge of video sync signal (VD_IS), and continues until the setup time.

WIDTH2[5:0] sets the width of pulse 2. The setup is performed at the number of times of rising after the end of count of start time. After the specified number of times of rising edge of VD_IS is counted, the output of pulse 2 ends at the falling edge of VD_IS.

P2EN controls the output of pulse 2.

When any of START2[8:0], WIDTH2[5:0], and P2EN is "0", pulse 2 is output.
Moreover, the setup value is not updated under the count of START2 or WIDTH2.

※The above pulse width is under the condition of WIDTH2[5:0]＝4

START2	Start time
0	0
1	20.1 µs
n	n × (68/3.375) µs
1023	20.56 ms

WIDTH2	Pulse width
0	0
1	VD_IS 1 count
63	VD_IS 63 count
n	VD_IS n count

■ Detail descriptions of register (continued)

- TGT_IN_TEST[9:0] (Iris output duty direct specified value)

Address			0Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						TGT_IN_TEST[9:0]									

Drive duty of Iris output block can be directly controlled. DUTY_TEST should be set to "1" in order to enable this function.
TGT_IN_TEST[9] sets the rotation direction of Iris output block. TGT_IN_TEST[8:0] sets the drive duty of Iris output block.

- Method for calculating drive duty

Drive duty depends on the setup value of PWM_IRIS[2:0].
a is calculated by a = { TGT_IN_TEST[8:1], 2'b00, TGT_IN_TEST[0] } (binary 10-bit).
b corresponding to PWM_IRIS[2:0] is selected from the following table.
The drive duty is given by calculating a/b. When a/b > 1, the drive duty is 100%.
Example) When TGT_IN_TEST[8:0] = 80h, PWM_IRIS[2:0] = 2,
a = { 40h, 2'b00, 1'b0 } = 200h
a/b = 200h / 862 = 0.59

TGT_IN_TEST[9]	Drive direction
0	Current direction OUTE2 → OUTE1
1	Current direction OUTE1 → OUTE2

TGT_IN_TEST[8:0]	Drive duty
000h	0%
1FFh	100%
n	a/b

PWM_IRIS[2:0]	b
0	2 046
1	1 726
2	862
3	574
4	430
5	350
6	286
7	254

■ Detail descriptions of register (continued)

• DUTY_TEST (Iris output duty direct specification enable)

Address			0Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				DUTY_TEST											

Whether duty direct control function in Iris output block is enabled or disabled is set.
When DUTY_TEST = 1 is set, PWM output will drive with the duty specified by TGT_IN_TEST[9:0].

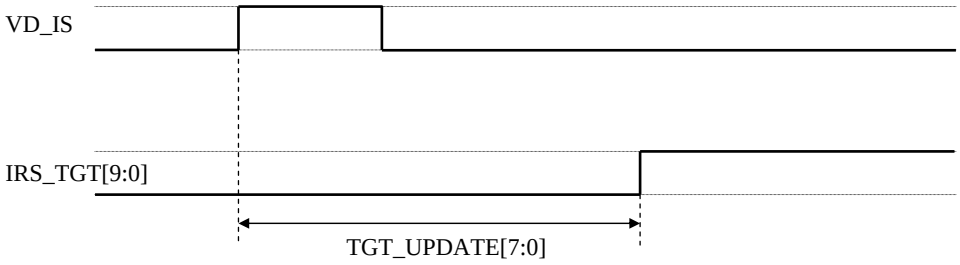
Setup value	Function
0	Disable (Normal operation)
1	Enable

■ Detail descriptions of register (continued)

• TGT_UPDATE[7:0] (IRS_TGT (iris target) update delay time)

Address			0Eh			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TGT_UPDATE[7:0]							

TGT_UPDATE[7:0] adjusts the update timing of IRS_TGT[9:0].
IRS_TGT[9:0] is updated after the delay time in the below table from rising edge of VD_IS.



Setting Value	Update delay
0	0
1	80 µs
n	n × (270/3.375) µs
255	20.4 ms

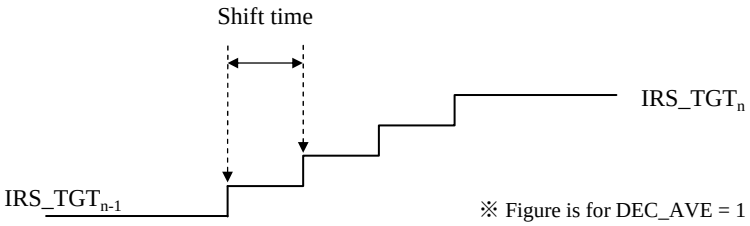
■ Detail descriptions of register (continued)

• AVE_SPEED[4:0] (Iris target moving average speed)

Address			0Eh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			AVE_SPEED[4:0]												

AVE_SPEED[4:0] sets the moving average shift time for iris target.

Setup value	Moving ave. shift time
0	2 µs
1	152 µs
n	(n × 512+1)/3.375 µs
31	4.703 ms



Example)

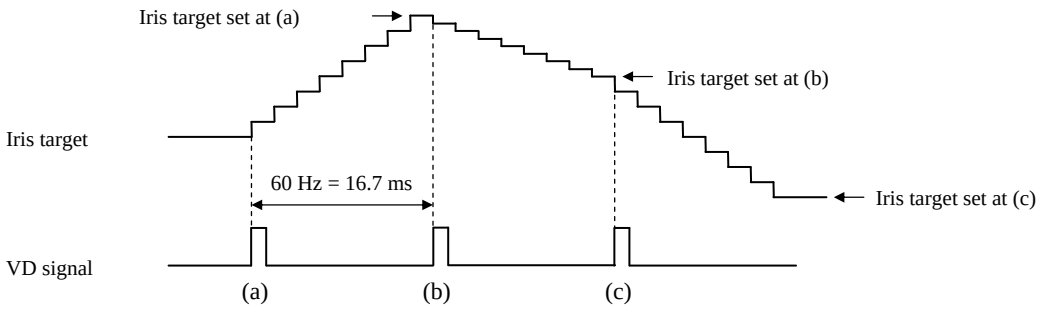
How to set AVE_SPEED[4:0] so that iris update time is exactly the same as VD period (DEC_AVE = 0, 8 times average):

If VD = 60 Hz, time required for 1 shift is

1/(60 Hz) / 8 = 2.08 ms

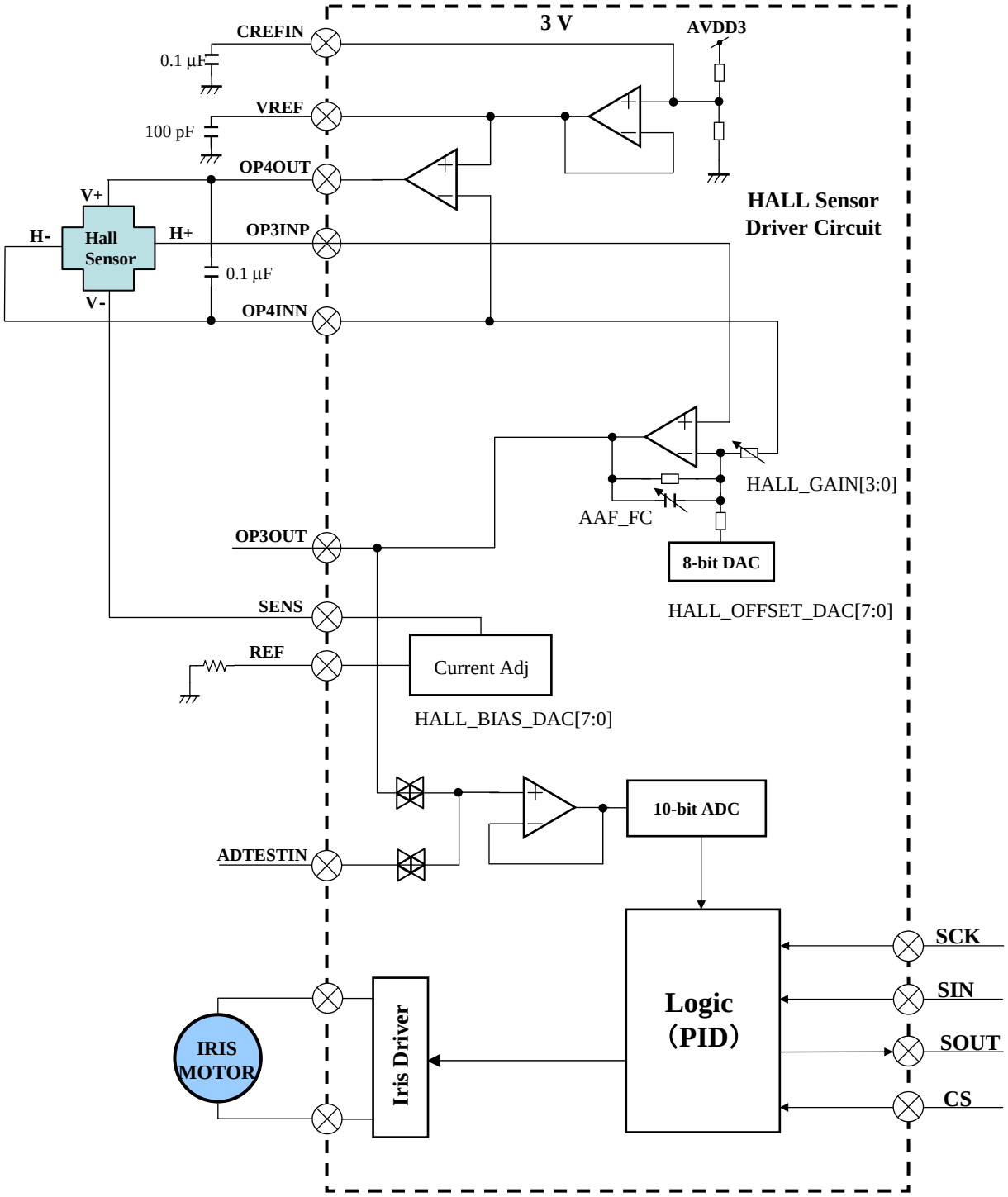
From the table, shift time will be 2.12 ms when AVE_SPEED[4:0] is set.

Since DEC_AVE = 0 (8 times average) is set, iris target change will complete in 17.0 ms.



Iris Control Hall Sensor

■ Block Diagram



■ Detail descriptions of register

- HALL_BIAS_DAC[7:0]

Address			04h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								HALL_BIAS_DAC[7:0]							

Drive current value for hall element is set. The value depends on an external resistance of REF pin.
SENS pin current is calculated by the following formula.

I_{SENS} = REF pin voltage / R_{REF} × (Setup value / 8)

Variation : ±11%, REF pin voltage = 1.26 V (Typ.)

- HALL_OFFSET_DAC[7:0]

Address			04h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HALL_OFFSET_DAC[7:0]															

Offset value for hall output Amp. is set.

Setup value	Amount of offset
0 to 255	AVDD3 / 256 × (Setup value – 128)

The methods for adjusting bias current and offset is shown as follows.

1. Bias current of hall element is set.

2. Once the amount of offset adjustment is set to zero (setup value : 80h). OP3OUT pin output (feedback to 10-bit ADC) is adjusted.
   a) Hall gain (HALL_GAIN[3:0]) is adjusted so that OP3OUT pin output range between Iris full open and full close nears the target range. (Rough-adjustment)
   Example : When the target is DVDD = 3.0 V, full open = 0.2 V, full close = 2.8 V,
   hall gain (HALL_GAIN[3:0]) is adjusted so OP3OUT pin output range nears 2.8 V – 0.2 V = 2.6 V.
   b) Bias current is adjusted so that the output range agrees with the target range. (Fine adjustment)
   c) Offset is adjusted so that OP3OUT pin output range agrees with the target range.

There is no problem even if either of b and c is performed previously.

■ Detail descriptions of register (continued)

• HALL_GAIN[3:0]

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				HALL_GAIN[3:0]											

Gain of hall output Amp. is set.

Setup value	Gain	Setup value	Gain
0	21.9	8	58.0
1	26.4	9	62.6
2	31.0	10	67.1
3	35.5	11	71.7
4	40.1	12	76.3
5	44.6	13	80.8
6	49.2	14	85.4
7	53.7	15	89.9

• AAF_FC

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			AAF_FC												

Cut-off frequency of hall output Amp. is set.

Setup value	Cut-off frequency (kHz)
0	6.85
1	20.0

(Hall amp. gain : min.)

■ Detail descriptions of register (continued)

• PDWNB

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					PDWNB										

PDWNB sets disable / enable of iris control circuit.

Setup Vale	Iris control
0	Disable
1	Enable

• ASWMODE[1:0]

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											ASWMODE[1:0]				

ASWMODE[1:0] sets test mode for iris ADC.

Setup value	Iris ADC mode
0	Normal mode
1	Normal mode
2	Iris test mode
3	—

By setting ASWMODE[1:0]=2, open loop frequency response of iris can be measured.
Refer to next page for detail.

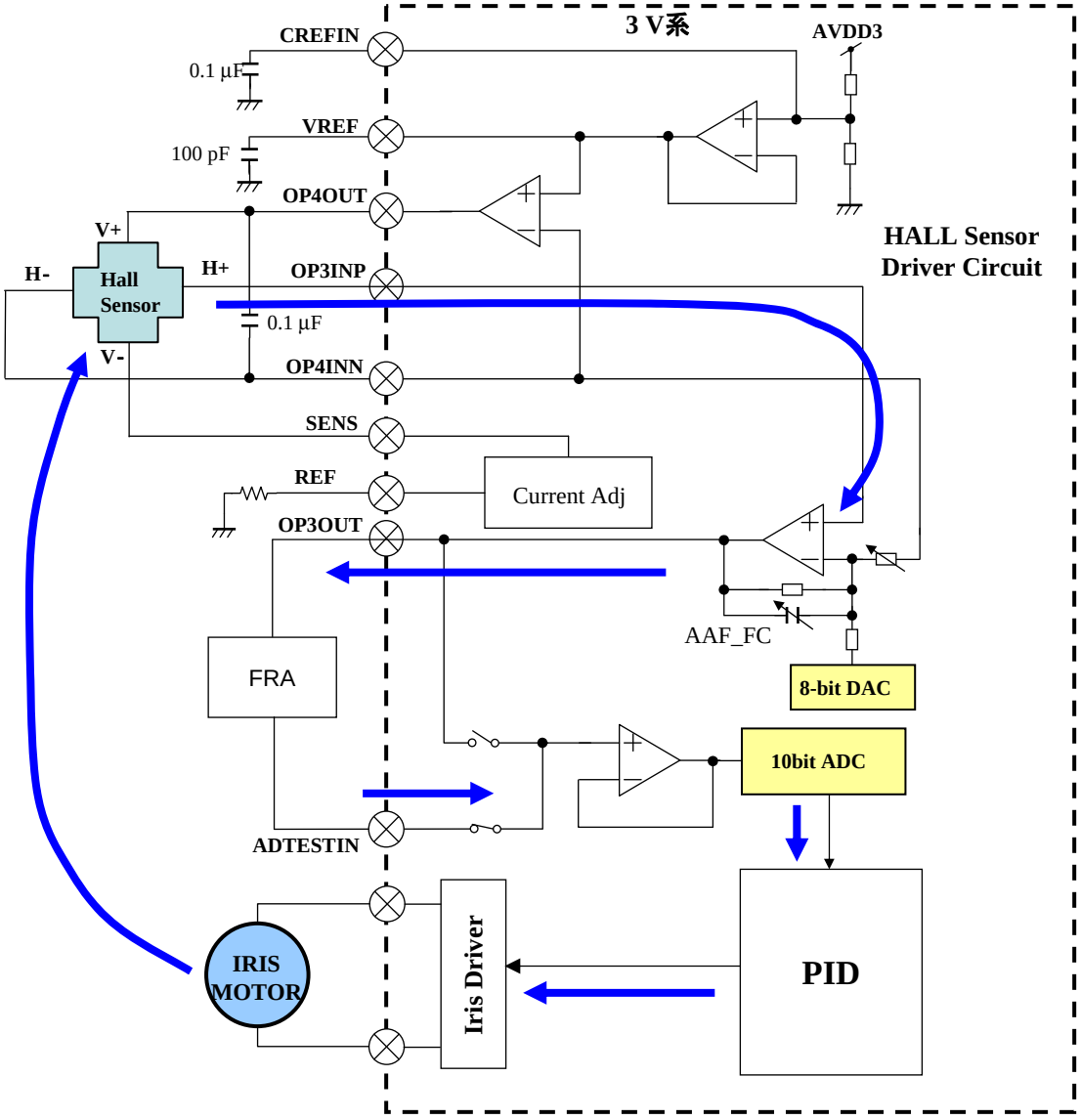
• ADC_TEST

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			ADC_TEST												

ADC_TEST is used for iris ADC functional test.
Do not set ADC_TEST = 1.

Setup value	Function
0	Normal operation
1	Iris ADC functional test

■ Method for measuring open loop frequency response



FRA : Frequency Response Analyzer

1) Set ASWMODE[1:0]=2.
2) Connect FRA (frequency response analyzer) between OP3OUT and ADTESTIN.
3) Set parameters for PID controller.
4) Open loop frequency from ADTESTIN to OP3OUT can be measured.

■ Detail descriptions of register (continued)

• PID_CLIP[3:0]

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PID_CLIP[3:0]															

PID_CLIP[3:0] sets maximum duty of iris PWM driver.

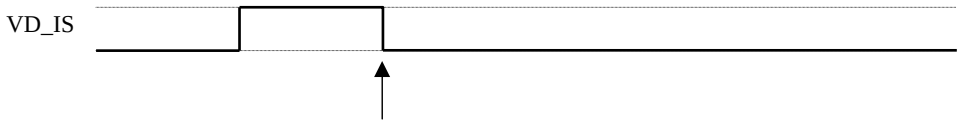
Setup value	Maximum duty
0	100%
1	93.75%
n	(100－n×6.25)%
15	6.25%

■ Detail descriptions of register (continued)

• IRSAD[9:0]

Address			0Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						IRSAD[9:0]									

IRSAD[9:0] is a read-only register to retrieve iris ADC output.
Access this register only when VD_IS is low.
(AN41908A updates the data at VD_IS = “H”. If IRSAD[9:0] is accessed during VD_IS = “H”, the read data may be incorrect.)



Iris ADC output: data is fixed at the falling edge of VD_IS.

LED Driver

■Electrical Characteristics at AVDD5, MVCCx = 4.8 V, DVDD, AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.

No.	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
LED driver							
1	Output ON resistancs	R_{onLED}	I = 20 mA, 5 V sell	—	—	15	Ω
2	H bridge leak current	$I_{leakLED}$	—	—	—	0.8	µA

■ Detail descriptions of register

LED can be controlled ON/OFF by the following registers.

- LEDA (LED A setup)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				LEDA											

- LEDB (LED B setup)

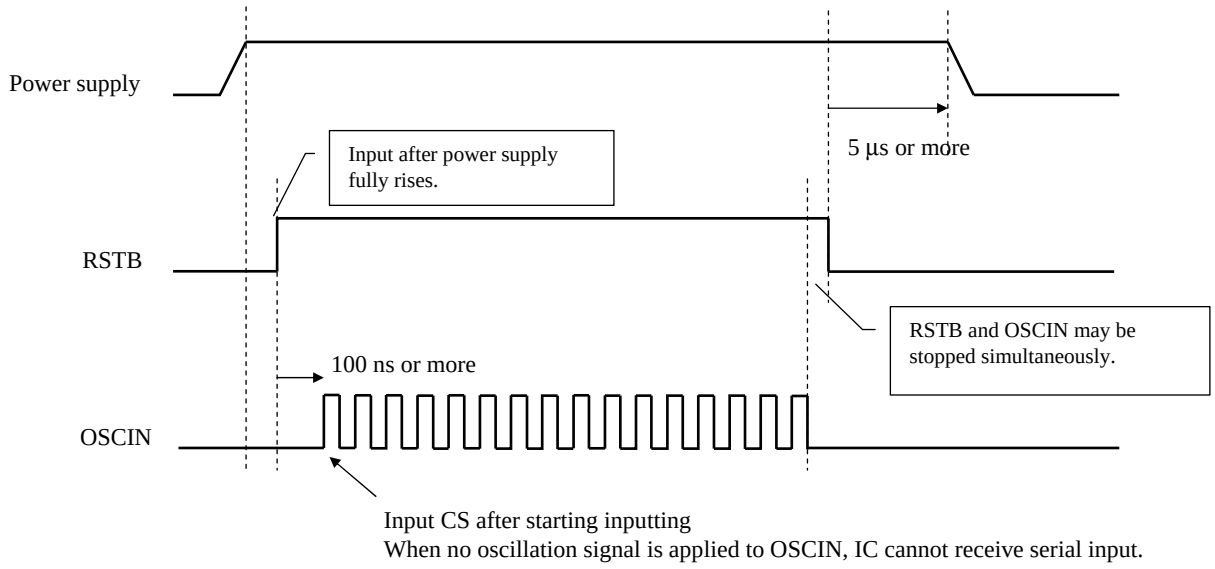
Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				LEDB											

LEDA and LEDB set the output of LED A and LED B respectively.

Setup value	LED output
0	OFF
1	ON

1. Start / Stop sequence

The Start / Stop sequence of power supply, RSTB, and OSCIN is shown as follows.



2. Input capacitance of input pin

Input capacitance of input pin is 10 pF or less.

3. Timing of OSCIN and VD signal

Since the processing which VD signal (VD_FX or VD_IS input) is synchronized with OSCIN is performed in this IC, OSCIN and VD signal do not have restrictions of input timing.

4. Power down mode

When PDWNB = 0 is set by serial, power down mode is set.
The analog circuit of Iris drive system is stopped in power down mode. (The operation of micro step driver dose not be affected.)
When only micro step driver is used, set PDWNB to "0" in order to reduce current consumption.
When using in power down mode at PDWNB = 0, the processing of pins of Iris drive system is shown as follows.

Pin	Processing
Input pin described in page 7, 8 of product standards	Connected to GND
Output pin described in page 7, 8 of product standards	Open
CREFIN (49)	Open
REF (57)	Open

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