



# SC8673030L

Asymmetric Dual Silicon N-ch Power MOSFET with Schottky Barrier Diode

For Load-switching, DC-DC Converter

■ Features

- Low Drain-source On-state Resistance : RDS(on) typ.  
FET1 : 6.7 mΩ (VGS = 4.5 V), FET2 : 1.6 mΩ (VGS = 4.5 V)
- Halogen-free / RoHS compliant  
(EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol : A3

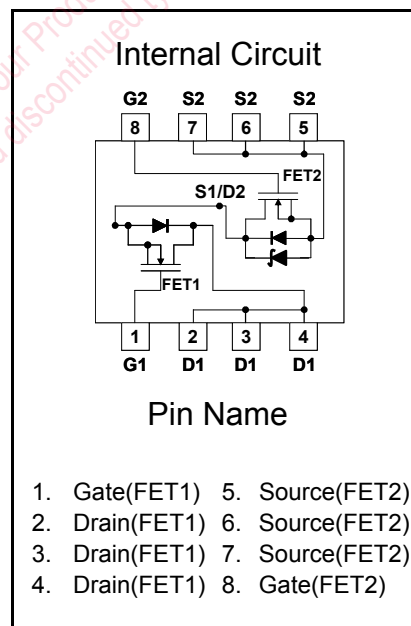
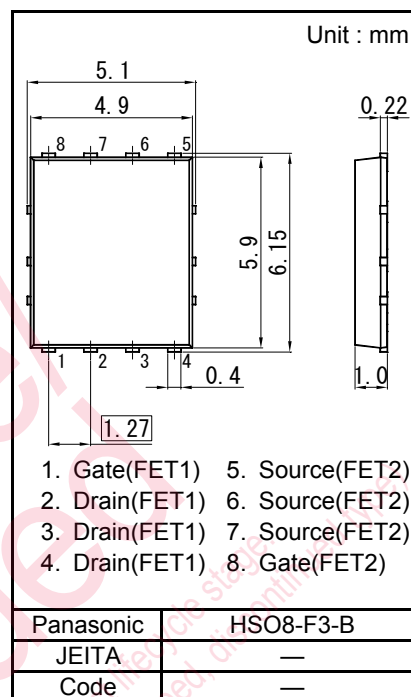
■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating		Unit
		FET1	FET2	
Drain to Source Voltage	VDS	30	30	V
Gate to Source Voltage	VGS	±20	±20	V
Drain Current	Package limited	ID1	20	A
	DC *1	ID2	12	
Drain Current (Pulsed) *1 *2	IDp	60	144	A
Total Power Dissipation	Ta = 25 °C, DC *1	PD1	1.7	W
	Ta = 25 °C, DC *3	PD2	1	
	Tc = 25 °C	PD3	19	
Thermal Resistance	Channel to Ambient *1	Rth(ch-a)1	70	°C / W
	Channel to Ambient *3	Rth(ch-a)2	125	
	Channel to Case	Rth(ch-c)	6.6	
Channel Temperature	Tch	150		°C
Storage Temperature Range	Tstg	-55 to +150		°C
Avalanche Current (Single pulse) *4	IAR	10	24	A
Avalanche Energy (Single pulse) *4	EAR	13	72	mJ

- Note \*1 Device mounted on a glass-epoxy board in Figure 1.1 and 1.2  
 \*2 Pulse test : Ensure that the channel temperature does not exceed 150 °C  
 \*3 Device mounted on a glass-epoxy board in Figure 1.3  
 \*4 VDD = 24 V, VGS = 10 to 0 V, L = 0.1 mH, Tch = 25 °C (initial)



Outline and Figures

FR4 Glass-Epoxy Board (25.4 mm × 25.4 mm × 0.8 mm)

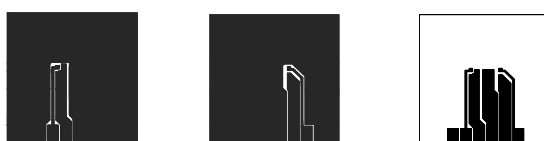
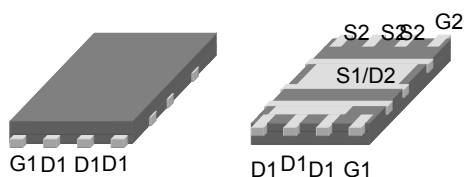


Figure 1.1 (FET1) Figure 1.2 (FET2) Figure 1.3 (FET1, FET2)



■ Electrical Characteristics Ta = 25 °C ± 3 °C

FET1

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Drain Current	IDSS	VDS = 30 V, VGS = 0 V			10	μA
Gate-source Leakage Current	IGSS	VGS = ±16 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 1.45 mA, VDS = 10 V	1.3		3	V
Drain-source On-state Resistance	RDS(on)1	ID = 10 A, VGS = 10 V		5.1	7.1	mΩ
	RDS(on)2	ID = 10 A, VGS = 4.5 V		6.7	9.8	
Input Capacitance	Ciss	VDS = 10 V, VGS = 0 V f = 1 MHz		1 200	1 680	pF
Output Capacitance	Coss			140	196	
Reverse Transfer Capacitance	Crss			100	160	
Turn-on Delay Time <sup>*1</sup>	td(on)	VDD = 15 V, VGS = 0 to 10 V		8		ns
Rise Time <sup>*1</sup>	tr	ID = 10 A		6		
Turn-off Delay Time <sup>*1</sup>	td(off)	VDD = 15 V, VGS = 10 to 0 V		39		ns
Fall Time <sup>*1</sup>	tf	ID = 10 A		6		
Total Gate Charge	Qg	VDD = 15 V, VGS = 0 to 4.5 V ID = 10 A		9.2		nC
Gate to Source Charge	Qgs			3		
Gate to Drain Charge	Qgd			3.5		
Gate resistance	rg	f = 5 MHz		1.4	3	Ω

Body Diode Characteristic

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode Forward Voltage	VSD	IS = 10 A, VGS = 0 V		0.8	1.2	V

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. \*1 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

FET2

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Drain Current	IDSS	VDS = 24 V, VGS = 0 V			1	mA
Gate-source Leakage Current	IGSS	VGS = ±16 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 5.96 mA, VDS = 10 V	1.3		3	V
Drain-source On-state Resistance	RDS(on)1	ID = 24 A, VGS = 10 V		1.3	1.9	mΩ
	RDS(on)2	ID = 24 A, VGS = 4.5 V		1.6	2.2	
Input Capacitance	Ciss	VDS = 10 V, VGS = 0 V f = 1 MHz		5 000	7 000	pF
Output Capacitance	Coss			600	840	
Reverse Transfer Capacitance	Crss			420	680	
Turn-on Delay Time <sup>*1</sup>	td(on)	VDD = 15 V, VGS = 0 to 10 V		16		ns
Rise Time <sup>*1</sup>	tr	ID = 24 A		22		
Turn-off Delay Time <sup>*1</sup>	td(off)	VDD = 15 V, VGS = 10 to 0 V		61		ns
Fall Time <sup>*1</sup>	tf	ID = 24 A		12		
Total Gate Charge	Qg	VDD = 15 V, VGS = 0 to 4.5 V ID = 24 A		38		nC
Gate to Source Charge	Qgs			13		
Gate to Drain Charge	Qgd			15		
Gate resistance	rg	f = 5 MHz		1.4	3	Ω

Body Diode Characteristic

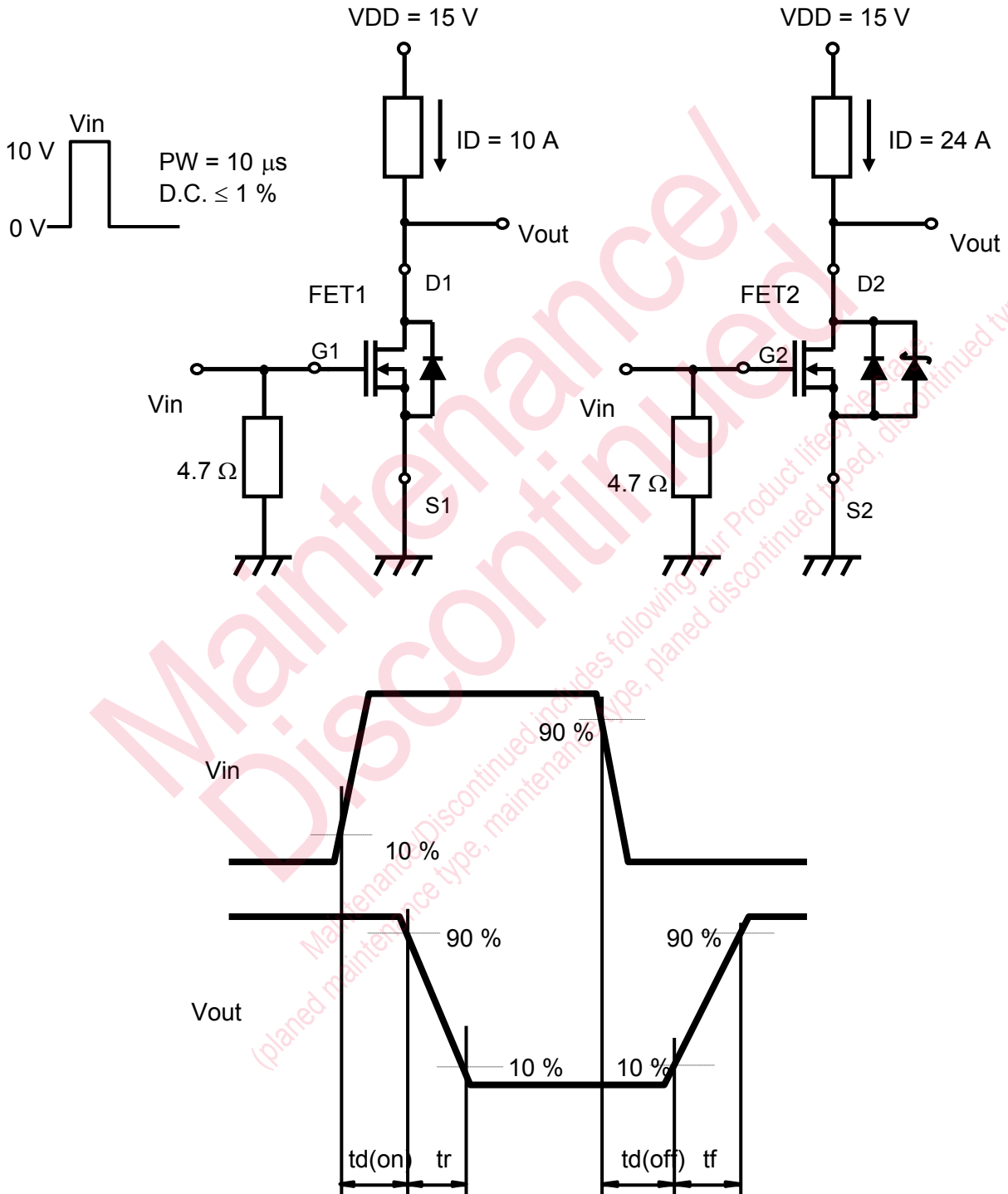
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Diode Forward Voltage	VSD1	IS = 24 A, VGS = 0 V		0.8	1.2	V
	VSD2	IS = 2 A, VGS = 0 V		0.5	1.2	

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. \*1 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



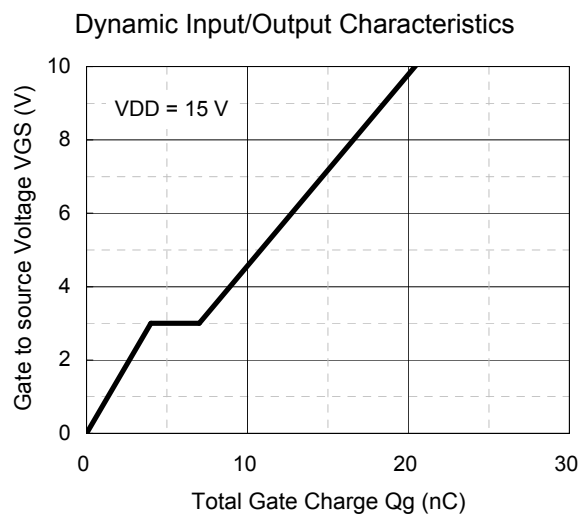
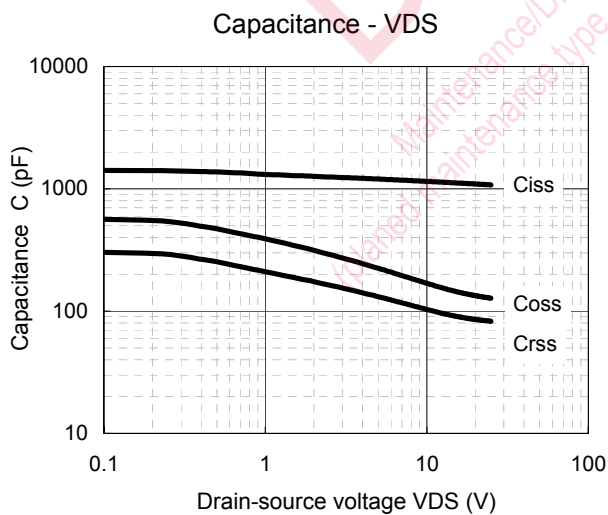
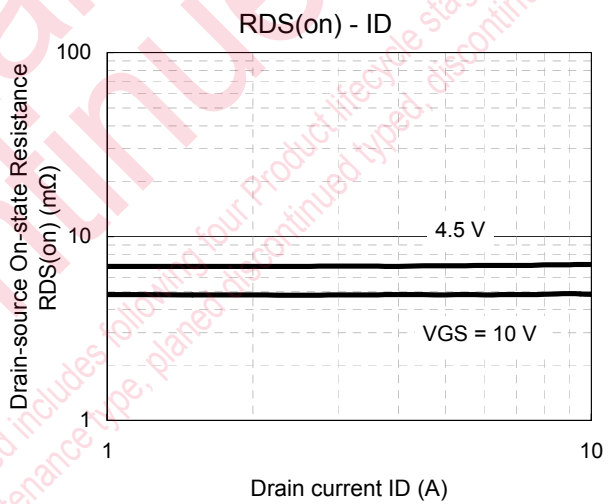
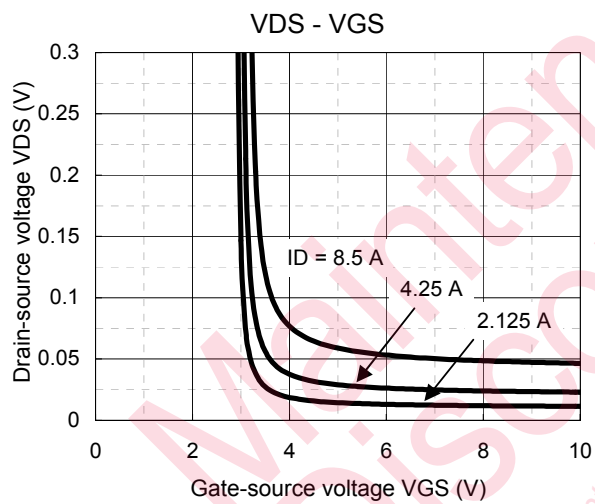
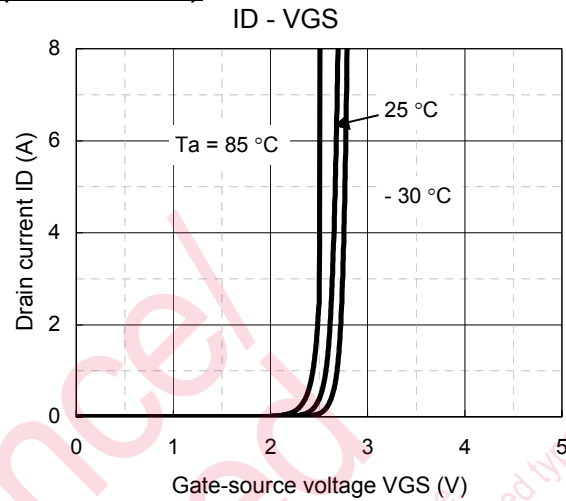
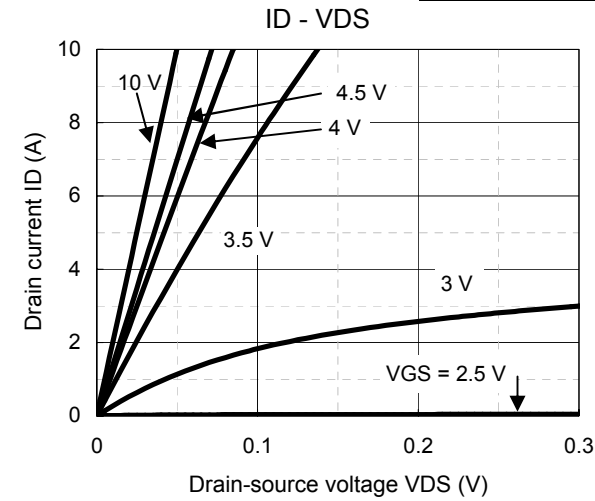
\*1 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time





FET1

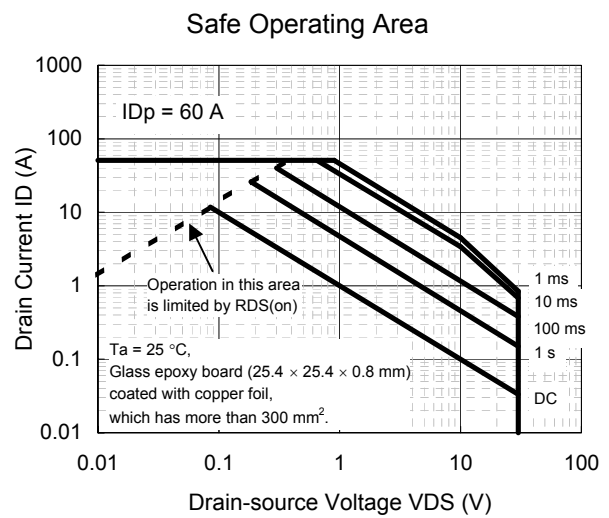
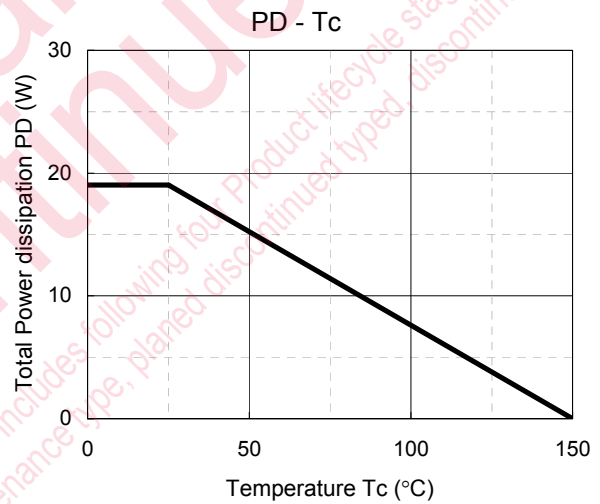
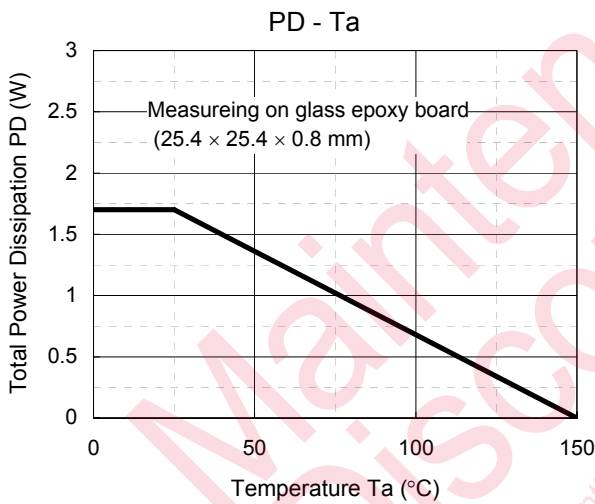
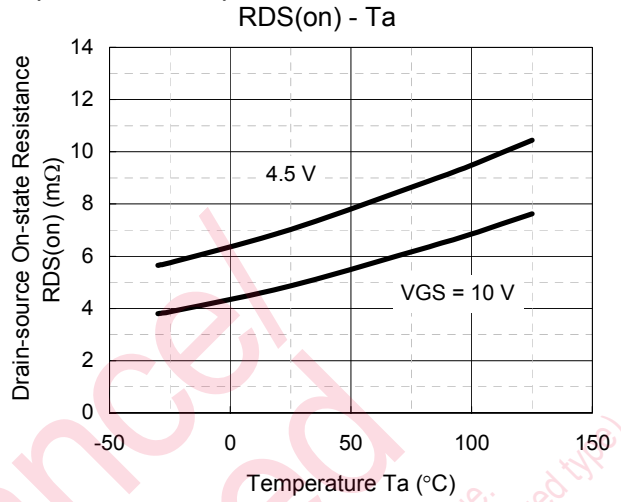
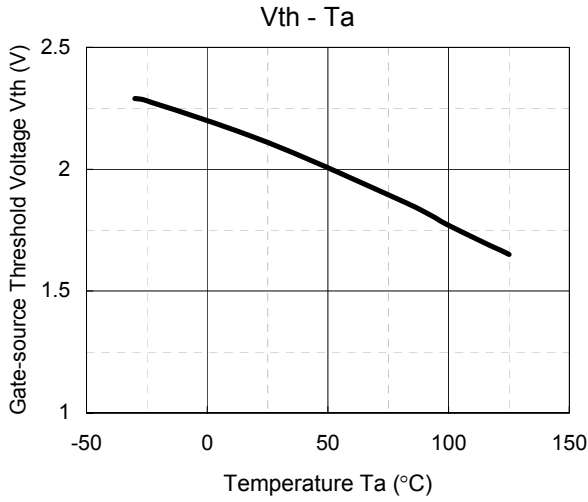
Technical Data ( reference )





FET1

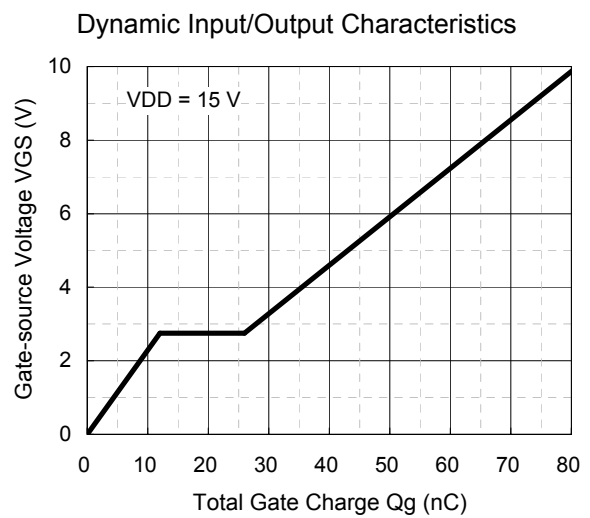
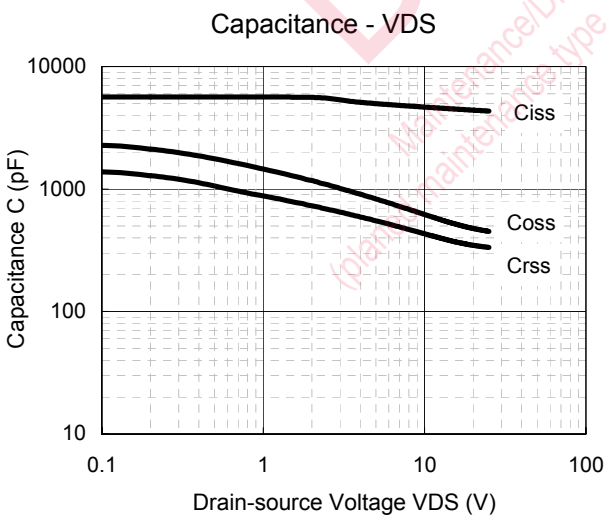
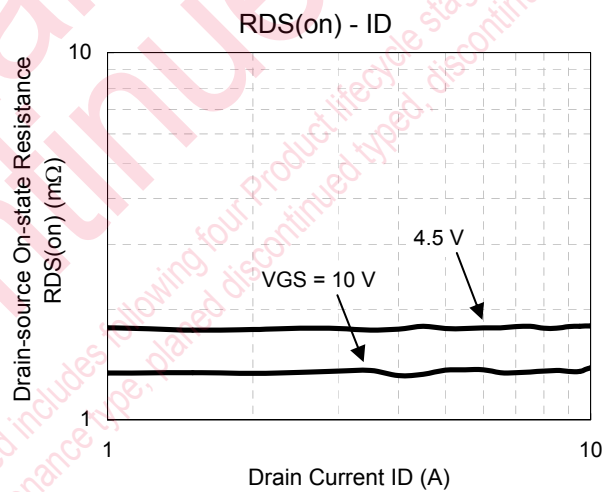
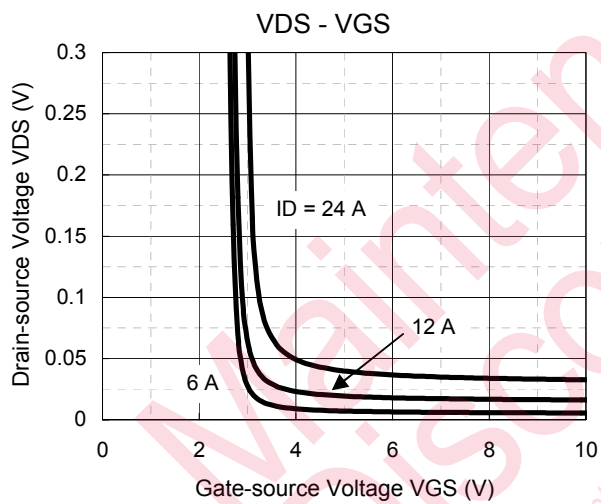
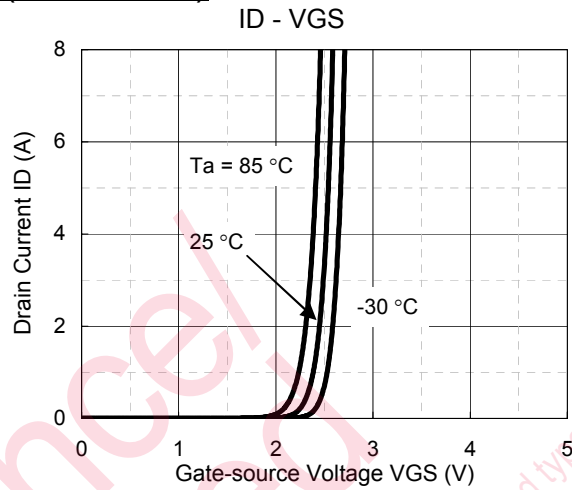
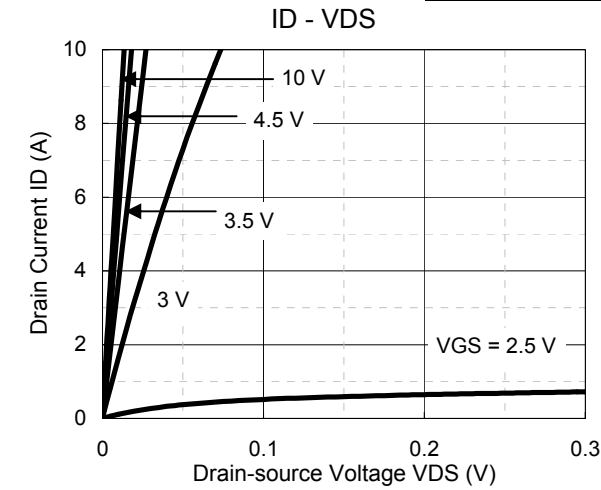
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FET2

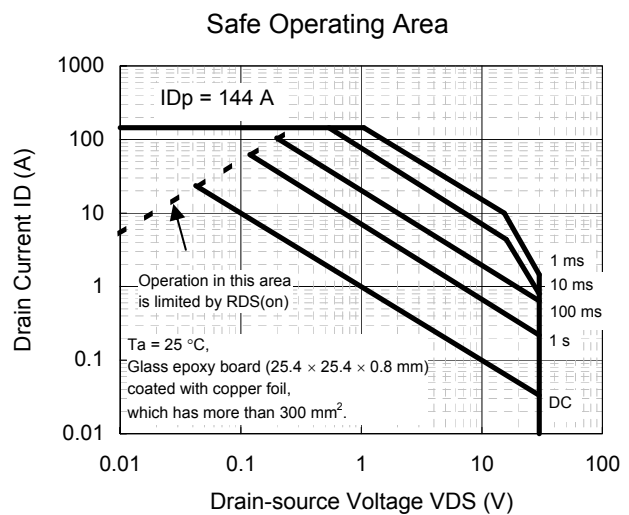
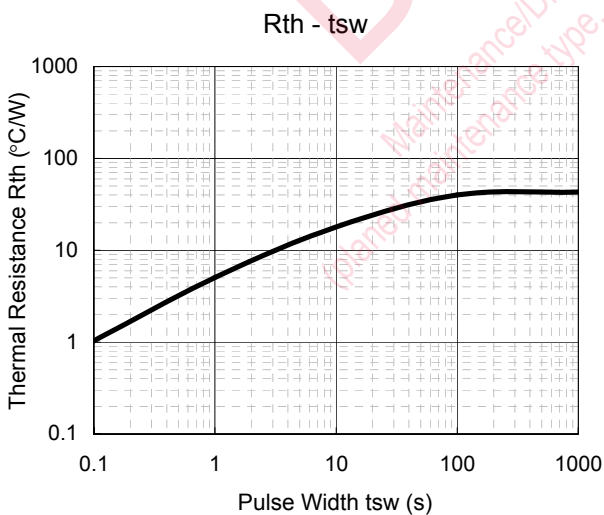
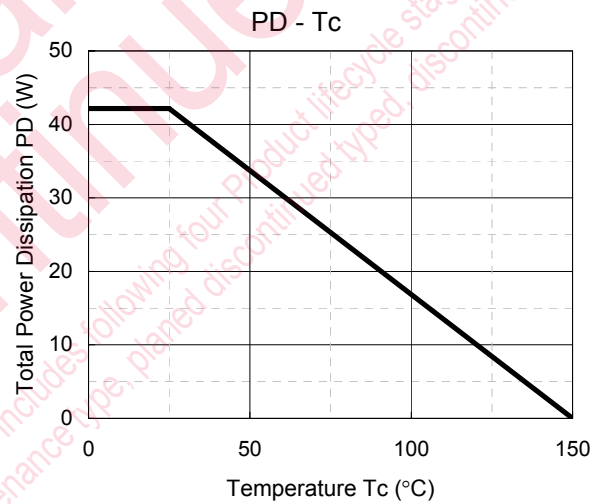
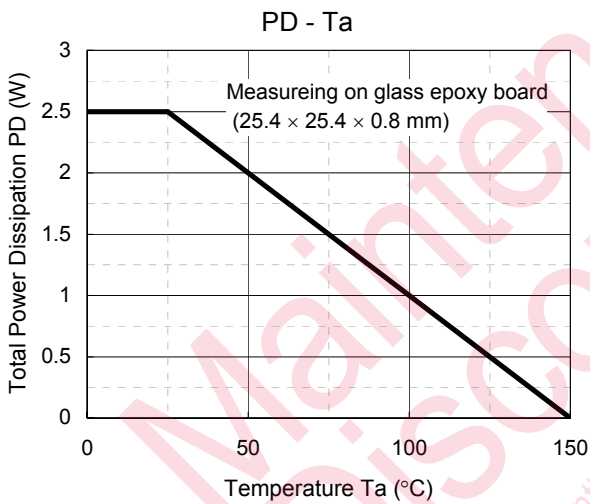
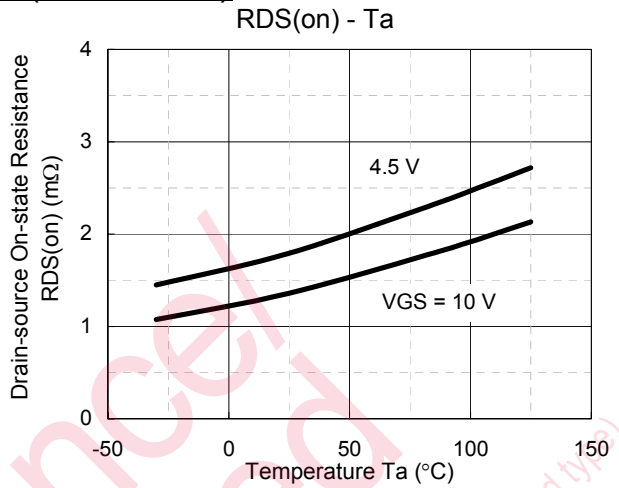
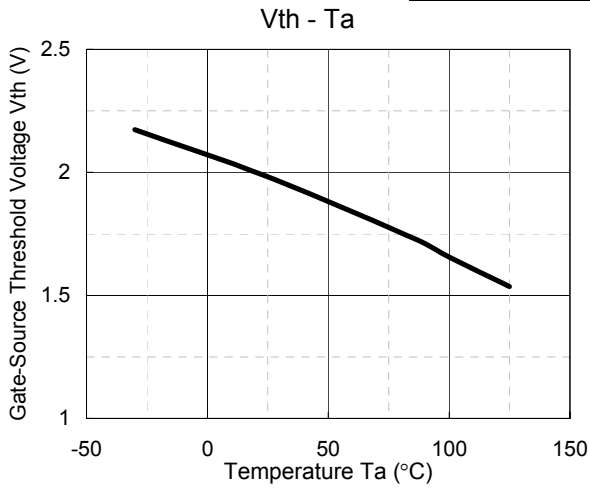
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FET2

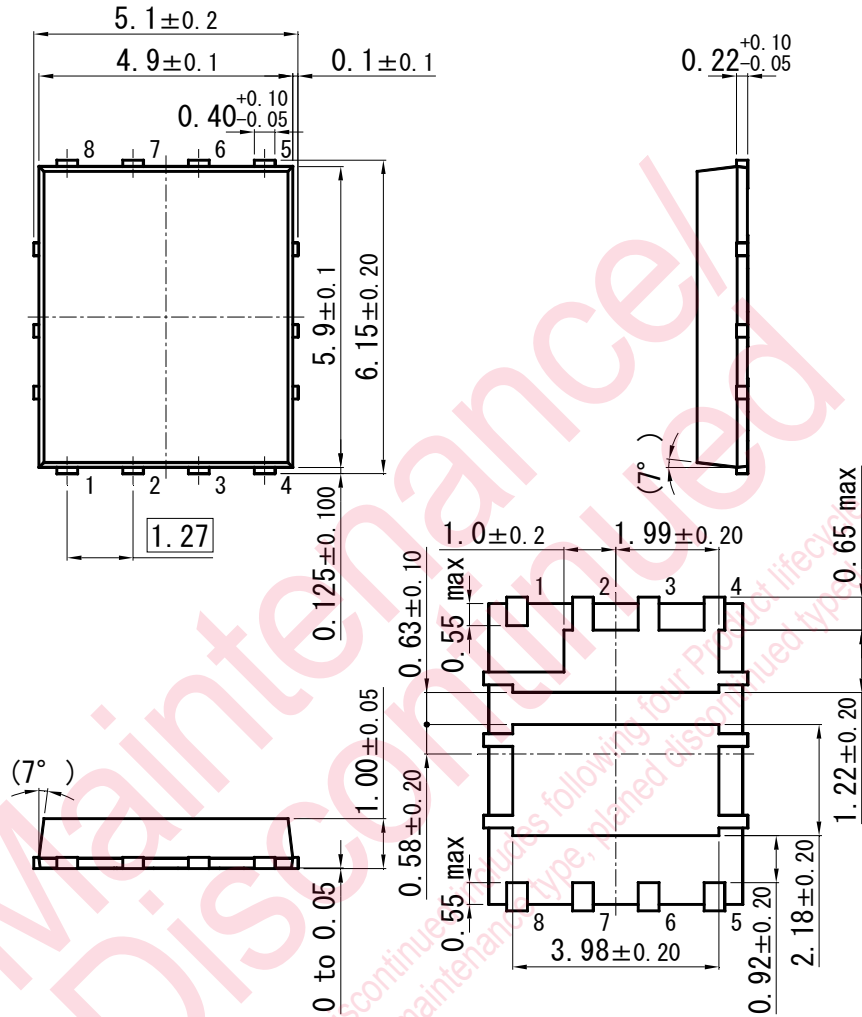
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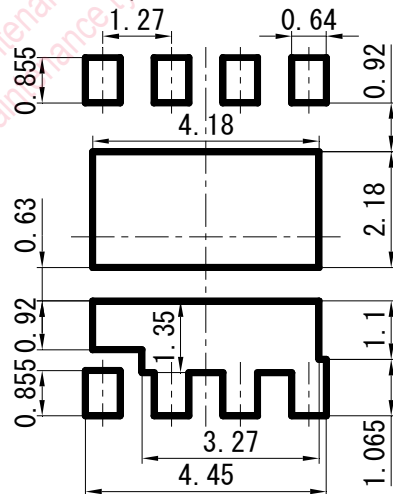


HSO8-F3-B

Unit : mm



■ Land Pattern (Reference) (Unit : mm)





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