

# MTM86727

Silicon N-channel MOS FET (FET)  
Silicon epitaxial planar type (SBD)

For DC-DC converter circuits

For switching circuits

## ■ Overview

MTM86727 is the composite MOS FET (N-channel MOS FET and schottky barrier diode) that is highly suitable for DC-DC converter and other switching circuits.

## ■ Features

- Built-in schottky barrier diode:  $V_R = 20\text{ V}$ ,  $I_F = 800\text{ mA}$
- Low ON resistance:  $R_{on} = 80\text{ m}\Omega$  ( $V_{GS} = 4.0\text{ V}$ )
- Low short-circuit input capacitance (common source):  $C_{iss} = 280\text{ pF}$
- Small package: WSSMini6-F1 (1.6 mm × 1.6 mm × 0.5 mm)
- Low drive voltage: 2.5 V drive

## ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

	Parameter	Symbol	Rating	Unit
FET	Drain-source surrender voltage	$V_{DSS}$	20	V
	Gate-source surrender voltage	$V_{GSS}$	±10	V
	Drain current	$I_D$	2.2	A
	Peak drain current	$I_{DP}$	8.0	A
	Channel temperature	$T_{ch}$	150	°C
	Storage temperature	$T_{stg}$	-55 to +150	°C
SBD	Reverse voltage	$V_R$	20	V
	Forward current (Average)	$I_{F(AV)}$	800	mA
	Non-repetitive peak reverse surge voltage *1	$I_{FSM}$	3	A
	Junction temperature	$T_j$	125	°C
	Storage temperature	$T_{stg}$	-55 to +125	°C
Overall	Total power dissipation *2	$P_D$	540	mW

Note) \*1: 50 Hz sine wave 1 cycle (Non-repetitive peak current)

\*2: Measuring on ceramic substrate at 40 mm × 38 mm × 0.2 mm

$P_D$  absolute maximum rating without a heat sink: 150 mW

## ■ Package

### • Code

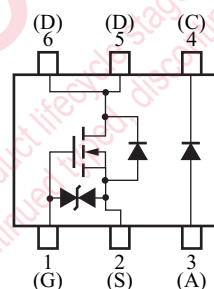
WSSMini6-F1

### • Pin Name

- |           |            |
|-----------|------------|
| 1. Gate   | 4. Cathode |
| 2. Source | 5. Drain   |
| 3. Anode  | 6. Drain   |

## ■ Marking Symbol: JE

## ■ Internal Connection



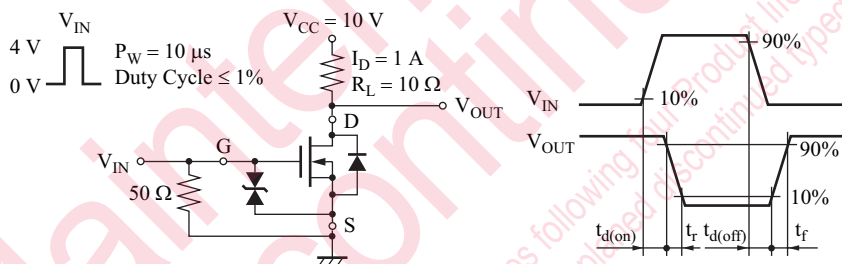
■ Electrical Characteristics  $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

• FET

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	$V_{DSS}$	$I_D = 1 \text{ mA}, V_{GS} = 0$	20			V
Drain-source cutoff current	$I_{DSS}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0$			1.0	$\mu\text{A}$
Gate-source cutoff current	$I_{GSS}$	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0$			$\pm 10$	$\mu\text{A}$
Gate threshold voltage	$V_{TH}$	$I_D = 1.0 \text{ mA}, V_{DS} = 10 \text{ V}$	0.4	0.85	1.3	V
Drain-source ON resistance 1	$R_{DS(on)1}$	$I_D = 1 \text{ A}, V_{GS} = 4.0 \text{ V}$		80	105	$\text{m}\Omega$
Drain-source ON resistance 2	$R_{DS(on)2}$	$I_D = 0.5 \text{ A}, V_{GS} = 2.5 \text{ V}$		100	150	$\text{m}\Omega$
Forward transfer admittance	$ Y_{fs} $	$I_D = 1.0 \text{ A}, V_{DS} = 10 \text{ V}$	3.0			S
Short-circuit input capacitance (Common source)	$C_{iss}$	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		280		pF
Short-circuit output capacitance (Common source)	$C_{oss}$			18		pF
Reverse transfer capacitance (Common source)	$C_{rss}$			17		pF
Turn-on delay time *	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, V_{GS} = 0 \text{ V to } 4 \text{ V}, I_D = 1 \text{ A}$		5		ns
Rise time *	$t_r$			8		ns
Turn-off delay time *	$t_{d(off)}$	$V_{DD} = 6 \text{ V}, V_{GS} = 4 \text{ V to } 0 \text{ V}, I_D = 1 \text{ A}$		20		ns
Fall time *	$t_f$			18		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*: Test circuit



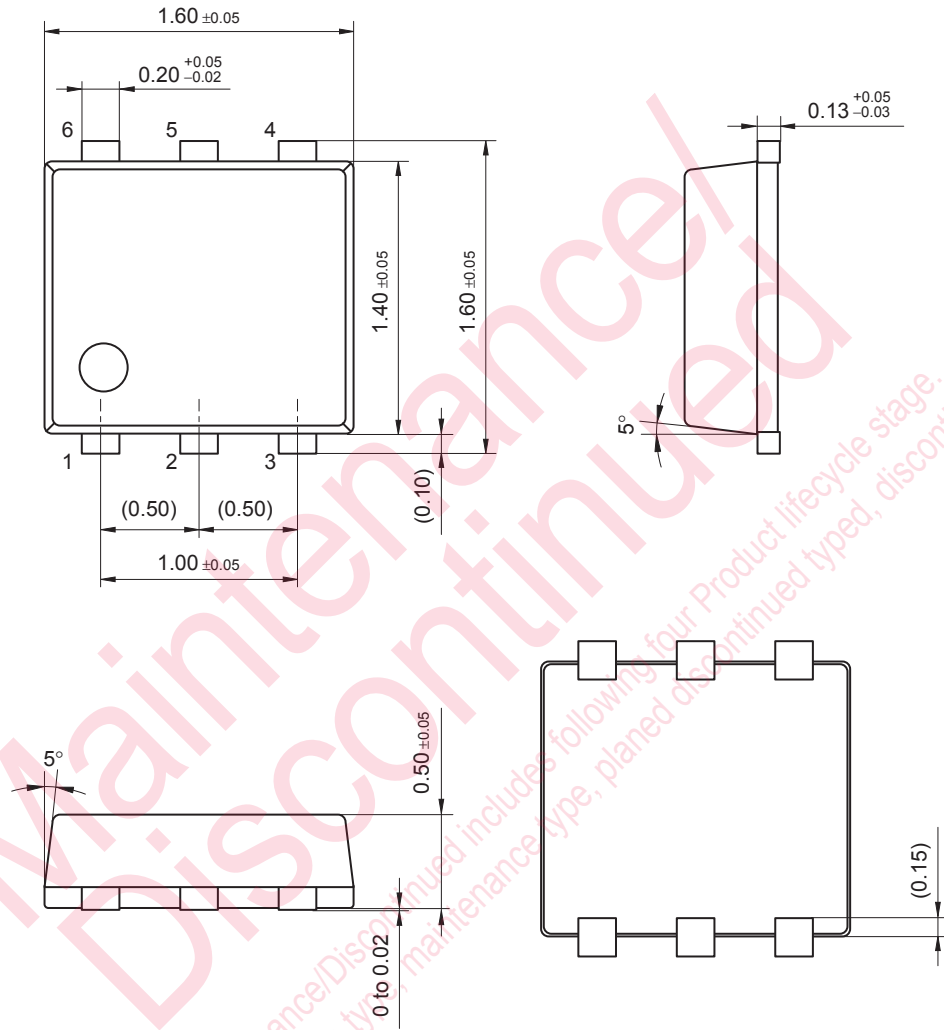
• SBD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Forward voltage	$V_F$	$I_F = 800 \text{ mA}$			0.47	V
Reverse current	$I_R$	$V_R = 20 \text{ V}$			80	$\mu\text{A}$

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7031 measuring methods for diodes.

WSSMini6-F1

Unit: mm



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