Overview
The MN3662 is a high responsivity CCD linear image sensor having floating photodiodes in the photodetector region, CCD analog shift registers for read out. It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

Features
- 3648 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- High blue responsivity of a maximum responsivity ratio of 40% (typ.) at 400nm, and smooth spectral response over the entire visible region.
- Large signal output of 1500mV (typ.) at saturation, and hold type combined odd/even output that makes signal processing easy.
- 24 Black dummy bits and low optical response (typ. 1%) at the areas other than the photodetector region.
- Operation with a single +12V positive power supply.

Pin Assignments

Application
- Reading out drawings, characters and numerals in image scanners, OCRs, etc.
- Measurement of position and dimensions of objects.

Block Diagram

B1 to B24 : Black dummy pixels
### Absolute Maximum Ratings (Ta=25°C, VSS=0V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>VDD</td>
<td>–0.3 to +17</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input pin voltage</td>
<td>VI</td>
<td>–0.3 to +17</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output pin voltage</td>
<td>VO</td>
<td>–0.3 to +17</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>Topr</td>
<td>–20 to +60</td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>Tstr</td>
<td>–40 to +100</td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

### Operating Conditions

#### Voltage conditions (Ta=–25 to +60°C, VSS=0V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>VDD</td>
<td>11.2</td>
<td>12.0</td>
<td>12.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IS test pin voltage</td>
<td>VIO</td>
<td>11.2</td>
<td>12.0</td>
<td>12.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Photo storage gate voltage</td>
<td>VPG</td>
<td>4.2</td>
<td>4.5</td>
<td>4.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output gate voltage</td>
<td>VOG</td>
<td>4.2</td>
<td>4.5</td>
<td>4.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CCD shift register clock High level</td>
<td>VZH</td>
<td>9.0</td>
<td>10.0</td>
<td>12.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CCD shift register clock Low level</td>
<td>VZL</td>
<td></td>
<td>0</td>
<td>0.5</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Reset gate clock High level</td>
<td>VRH</td>
<td>9.0</td>
<td>10.0</td>
<td>12.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Reset gate clock Low level</td>
<td>VRH</td>
<td></td>
<td>0</td>
<td>0.5</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Shift gate clock High level</td>
<td>VSH</td>
<td>9.0</td>
<td>10.0</td>
<td>12.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Shift gate clock Low level</td>
<td>VSL</td>
<td></td>
<td>0</td>
<td>0.5</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

#### Timing conditions (Ta=–25 to +60°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shift register clock frequency</td>
<td>fC</td>
<td>fC =1/2T</td>
<td>0.1</td>
<td></td>
<td>1.0</td>
<td>MHz</td>
</tr>
<tr>
<td>Reset clock frequency</td>
<td>fR</td>
<td>fR =1/T</td>
<td>0.2</td>
<td></td>
<td>2.0</td>
<td>MHz</td>
</tr>
<tr>
<td>Shift clock rise time</td>
<td>tSR</td>
<td></td>
<td>0</td>
<td>15</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>Shift clock set up time</td>
<td>tSS</td>
<td></td>
<td>0</td>
<td>0.03</td>
<td>10.0</td>
<td>ns</td>
</tr>
<tr>
<td>Shift clock pulse width</td>
<td>tSW</td>
<td></td>
<td>10</td>
<td>12</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>Shift clock hold time</td>
<td>tSH</td>
<td></td>
<td>0</td>
<td>0.5</td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>Shift register clock rise time</td>
<td>tCR</td>
<td></td>
<td>0</td>
<td>20</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>Shift register clock fall time</td>
<td>tCF</td>
<td></td>
<td>0</td>
<td>20</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>Reset clock rise time</td>
<td>tRR</td>
<td></td>
<td>0</td>
<td>15</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>Reset clock fall time</td>
<td>tRF</td>
<td></td>
<td>0</td>
<td>15</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>Reset clock pulse width</td>
<td>tRW</td>
<td></td>
<td>30</td>
<td>60</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>Reset clock set up time</td>
<td>tRS</td>
<td></td>
<td>200</td>
<td>400</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Reset clock hold time</td>
<td>tRH</td>
<td></td>
<td>0</td>
<td>5</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>Output signal set up time</td>
<td>tOS</td>
<td></td>
<td>120</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

* OS output level=300mV

### Electrical Characteristics

#### DC characteristics (Ta=0 to +60°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply current</td>
<td>IDD</td>
<td>VSS=+12V</td>
<td></td>
<td>10</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td>Photostorage gate pin leak current</td>
<td>IPG</td>
<td>VSS=+5V</td>
<td></td>
<td></td>
<td>50</td>
<td>µA</td>
</tr>
<tr>
<td>Output gate pin leak current</td>
<td>IOG</td>
<td>VSS=+5V</td>
<td></td>
<td></td>
<td>50</td>
<td>µA</td>
</tr>
</tbody>
</table>

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**Discontinued**

Discontinued includes following four Product lifecycle stage
(planed maintenance type, maintenance type, planed discontinued typed, discontinued type)
- Clock input capacitance (Ta=−20 to +60°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shift register clock input capacitance</td>
<td>C1, C2</td>
<td>VDD=12V</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Reset clock input capacitance</td>
<td>C_R</td>
<td>f=1MHz</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Shift clock input capacitance</td>
<td>C_s</td>
<td></td>
<td>150</td>
<td>—</td>
<td>—</td>
<td>pF</td>
</tr>
</tbody>
</table>

- Optical Characteristics (Ta=25°C, Normal operating condition, f=1MHz, T_acc (accumulation time)=10ms)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation output voltage</td>
<td>V_SAT</td>
<td>(Note 1)</td>
<td>1000</td>
<td>1500</td>
<td>—</td>
<td>mV</td>
</tr>
<tr>
<td>Saturation exposure</td>
<td>SE</td>
<td>(Note 1)</td>
<td>1.30</td>
<td>1.95</td>
<td>—</td>
<td>lx·s</td>
</tr>
<tr>
<td>Minimum saturation exposure output voltage</td>
<td>V_SATmin</td>
<td>(Note 2)</td>
<td>1000</td>
<td>—</td>
<td>1400</td>
<td>mV</td>
</tr>
<tr>
<td>Photoresponse non-uniformity</td>
<td>PRNU</td>
<td>(Note 3)</td>
<td>exposure: 1.3lx·s</td>
<td>—</td>
<td>—</td>
<td>20%</td>
</tr>
<tr>
<td>Bit non-uniformity</td>
<td>BNU</td>
<td>(Note 4)</td>
<td>exposure: 1.3lx·s</td>
<td>—</td>
<td>—</td>
<td>±10%</td>
</tr>
<tr>
<td>Odd/even bit non-uniformity</td>
<td>O/E</td>
<td>(Note 5)</td>
<td>exposure: 1.3lx·s</td>
<td>1</td>
<td>5</td>
<td>%</td>
</tr>
<tr>
<td>Dark signal output voltage</td>
<td>V_d</td>
<td>(Note 6)</td>
<td>Dark condition</td>
<td>—</td>
<td>—</td>
<td>10 mV</td>
</tr>
<tr>
<td>Shift register total transfer efficiency</td>
<td>STTE</td>
<td>(Note 7)</td>
<td>exposure: 1.3lx·s</td>
<td>92</td>
<td>99</td>
<td>%</td>
</tr>
<tr>
<td>Modulation transfer function</td>
<td>MTF</td>
<td>(Note 8)</td>
<td></td>
<td>76</td>
<td>—</td>
<td>%</td>
</tr>
</tbody>
</table>

- Optical system: Light source = G-54 green fluorescent lamp (peak wavelength=543nm), using a slit of size 40mm × 40mm.
  Distance between slit and sensor = 200mm (equivalent to F=5)
- Inspected by the output from a unity gain differential amplifier to which the OS and DS are input (input impedance=100kΩ or more)
- These specifications apply to the 3648 valid pixels excluding the dummy pixels D1 to D4.

Note 1) Saturation output voltage: This is the output voltage at the point beyond which it is not possible to maintain the linearity of the photoelectric conversion characteristics as the exposure is increased. (The exposure at this point is called the saturation exposure.)

Note 2) Minimum saturation exposure output voltage: This is the output voltage at the minimum specified value (1.3lx·s) of the saturation exposure. It is possible to calculate the responsivity from this parameter. That is,
  Responsivity (minimum value) = 1.0V/1.3lx·s = 0.77V/lx·s
  Responsivity (maximum value) = 1.4V/1.3lx·s = 1.08V/lx·s

The responsivity when a daylight type fluorescent lamp is used will be about 1.5 times the responsivity when the G-54 green fluorescent lamp is used.

Note 3) Photoresponse non-uniformity (PRNU): This is defined by the following equation where the difference between the maximum and minimum values in the output of all the 3648 active pixels is denoted by Δx when the photodetector region is illuminated by a light of uniform illumination intensity distribution, and the average value of the output voltage from all the 3648 pixels is denoted by Xave. The responsivity when a daylight type fluorescent lamp is used will be about 1.5 times the responsivity when the G-54 green fluorescent lamp is used.

Note 4) Bit non-uniformity: This is defined by the following equation where the average output voltage of each pixel among the 3648 pixels is denoted by X_i (i = 1 to 3648) when the photodetector region is illuminated by a light of uniform illumination intensity distribution, and the average output voltage of the pixels near the ith pixel is denoted by Xlocal-ave. (a total of 20 pixels with 10 pixels before and 10 pixels after that pixel). Here, the max. operation consists of comparing with the absolute value and assigning the sign of the numerator.

Note 5) Odd-even bit non-uniformity: This is defined by the following equation where the average output voltage of the 1824 even numbered pixel photodiodes is denoted by X_ave, the average output voltage of the 1824 odd numbered pixel photodiodes is denoted by X_ave, and the average output voltage of all the 3648 pixels is denoted by Xave. when the photodetector region is illuminated by a light of uniform illumination intensity distribution.

Note 6) Dark signal output voltage: This is the maximum value of the outputs from the 3648 valid pixels in the dark condition with Ta=25°C and Tacc=10ms. The dark signal output voltage normally gets doubled with an increase of about 8 to 10°C in Ta, and is proportional to Tacc.

Note 7) Shift register total transfer efficiency: This is given by the following equation where the average output voltage of all the 3648 pixels is denoted by Xave. and the larger of the output voltages of the 2 dummy pixels following the dummy pixel D4 is denoted by X when the photodetector region is illuminated by a light of uniform illumination intensity distribution.

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Note 8) Modulation transfer function: This is defined by the following equation where the average output voltages from the pixels with the white pattern and the pixels with the black pattern are respectively denoted by $V_w$ and $V_b$ when a black and white stripe pattern (in which the black and white patterns alternate at every pixel) is projected on the photodetector region in phase (equivalent to the Nyquist spatial frequency).

$$MTF_R = \frac{V_w - V_b}{V_w + V_b} \times 100\%$$

This value is a measure of resolution of the sensor. This parameter is not a guaranteed value but is merely a reference value.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Pin name</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OS</td>
<td>Signal output</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>(\phi_R)</td>
<td>Reset clock</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>(\phi_{1A})</td>
<td>CCD shift register clock</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>(\phi_{2A})</td>
<td>CCD shift register clock</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>PG</td>
<td>Photo storage gate</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>(\phi_{3G})</td>
<td>Shift gate clock</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>IS</td>
<td>Test pin</td>
<td>Connect externally to (V_{DD}).</td>
</tr>
<tr>
<td>14</td>
<td>(\phi_{2B})</td>
<td>CCD shift register clock</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>(\phi_{1B})</td>
<td>CCD shift register clock</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>(V_{SS})</td>
<td>Ground</td>
<td>Connected to the substrate.</td>
</tr>
<tr>
<td>17</td>
<td>OG</td>
<td>Output gate</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>(V_{DD})</td>
<td>Power supply</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>NC</td>
<td>Non connection</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>DS</td>
<td>Compensatin output</td>
<td></td>
</tr>
</tbody>
</table>

Note) Connect all NC pins externally to Ground.

### Construction of the Image Sensor

The MN3662 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region
- The photoelectric conversion device consists of a 5µm floating photodiode and a 3µm channel stopper for each pixel, and 3648 of these devices are linearly arranged side by side at a pitch of 8µm.
- The photo detector's windows are 8µm × 8µm squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 24 optically shielded pixels which serve as the black reference.

b) CCD Transfer region (shift register)
- The optical output after photoelectric conversion is transferred respectively to the odd and even CCD transfer region at the timing of the shift gate electrode \(\phi_{3G}\), the photoelectric converted output transferred to this analog shift register is transferred successively to the output region.
- A buried type CCD that can be driven by a 2-phase clock is used as the analog shift register.

c) Output region
- The signal transferred to this region is sent to the detector region and is output after impedance conversion by a two stage source follower amplifier.

**Evaluation board**

The placement of the each component is very important in order to get a good output signal. The evaluation board BS801 is available for evaluating the MN3662.
Timing Diagram

(1) I/O timing

Integration Time (Tint.)

\(\phi_{SO}\)

\(\phi_1\)

\(\phi_2\)

\(\phi_R\)

DS

OS

(2) Drive timing

(3) Timing condition measuring circuit

Drive circuit

\(C_1 = C_2 = C_{12} = 880\text{pF}\)

\(C_3 = 150\text{pF}\)

\(C_4 = 10\text{pF}\)

Graphs and Characteristics

- Photoelectric Conversion Characteristics
- Spectral Response Characteristics

Characteristics under standard operating condition
Light source: Green fluorescent lamp

Relative responsivity

Under standard operating condition

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