Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

1.1 Overview

1.1.1 Overview

The MN103S is a 32-bit microcontroller combining ease of use intended for programs development in the C language with a simple, high-performance architecture made possible through pursuit of cost performance.

Built around a compact 32-bit CPU with a basic instruction word length of 1 byte, this LSI includes internal memory for instructions and data, DMA controller, a clock generator, bus controller, interrupt controller, watchdog timer, standard peripheral circuitry such as timers and serial interfaces, PWM circuit best suited to controlling 3-phase motors and A/D converters for motor position control. The MN103S Series' high-speed CPU coupled with abundance of peripheral features provides an easy means of developing low-cost, high-performance and multi-functional system on LSI for motor and power control applications requiring fast response - a feature previously unavailable with conventional microcontrollers.

1.1.2 Product Summary

This manual describes the following models.

Table:1.1.1 Product Summary

Model	ROM Size	RAM Size	Pins	Timer (8bit/16bit)	PWM	Serial I/F	A/D	VGA
MN103SFJ7A	32KB	2KB	TQFP 48 pin	8/1	1	2	2	-
MN103SFN0D	64KB	4KB	QFP 44 pin TQFP 48 pin	8/2	1	2	2	-
MN103SFN0X		8KB						
MN103SFN0G	128KB	6KB						
MN103SFN0Y		8KB						
MN103SFN1D	64KB	4KB	TQFP 64 pin LQFP 64 pin	12/3	2	3	2	-
MN103SFN1X		8KB						
MN103SFN1G	128KB	6KB						
MN103SFN1Y		8KB						
MN103SFN2D	64KB	4KB	TQFP 80 pin	12/5	2	3	2	-
MN103SFN2X		8KB						
MN103SFN2G	128KB	6KB						
MN103SFN2Y		8KB						
MN103SFN4D	64KB	4KB	QFP 44 pin TQFP 48 pin	8/2	1	2	2	1
MN103SFN4X		8KB						
MN103SFN4G	128KB	6KB						
MN103SFN4Y		8KB						
MN103SFN5D	64KB	4KB	TQFP 64 pin LQFP 64 pin	12/3	2	3	2	2
MN103SFN5X		8KB						
MN103SFN5G	128KB	6KB						
MN103SFN5Y		8KB						
MN103SFN6D	64KB	4KB	TQFP 80 pin	12/5	2	3	2	2
MN103SFN6X		8KB						
MN103SFN6G	128KB	6KB						
MN103SFN6Y		8KB						

1.2 Hardware Functions

CPU Core
MN103S core
4 GB of address space (for instructions / data)
LOAD/STORE architecture with 5-stage pipeline
46 basic instructions + 8 extension instructions
6 addressing modes
Instruction set of 1 byte in word length
Extension arithmetic unit incorporated
(high-speed multiply instruction, high-speed division instruction etc.)
Machine cycle: 16.7 ns (oscillation frequency: 10 MHz, 6 multiplying)
Operation mode: NORMAL mode, SELLP mode, HALT mode, STOP mode

Oscillation Circuit
External oscillation (crystal/ ceramic)

Clock multiply circuit
Oscillation clock can be multiplied by from 3 to 12

Internal Memory
ROM 32 K/64 K/128 Kbytes RAM 2 K/4 K/6 K/8 Kbytes
The ROM/RAM size is different in each product.
Please refer to [2.6.2 Memory Map] for details.

DMA Controller*
Numbr of channels : 1 channel
Startup sources : 15 sources (MN103SFN0/N4 series)
20 sources (MN103SFN1/N5 series)
22 sources (MN103SFN2/N6 series)
(External interrupts : Max 12 sources,
Serial Interface : Max 9 sources,
Software start : 1 sources)
Transfer modes : 3 modes (One word transfer, Burst transfer, Intermittent transfer)
* There is not the function in the MN103SFJ7A.

Interrupts
Non-maskable interrupts
Watchdog timer overflow interrupts
System error interrupts
Fail safe function interrupts
Internal interrupts (Level interrupt)
MN103SFJ7A : 23 interrupts
MN103SFN0/N4 series: 29 interrupts
MN103SFN1/N5 series: 42 interrupts
MN103SFN2/N6 series: 48 interrupts

<Timer Interrupts>
Timer 0 underflow interrupt
Timer 1 underflow interrupt
Timer 2 underflow interrupt
Timer 3 underflow interrupt
Timer 4 underflow interrupt
Timer 5 underflow interrupt
Timer 6 underflow interrupt
Timer 7 underflow interrupt
Timer 8 underflow interrupt
Timer 9 underflow interrupt
Timer 10 underflow interrupt
Timer 11 underflow interrupt
Timer 16 overflow/underflow interrupt

Timer 16 compare/capture A interrupt
Timer 16 compare/capture B interrupt
Timer 17 overflow/underflow interrupt
Timer 17 compare/capture A interrupt
Timer 17 compare/capture B interrupt
Timer 18 overflow/underflow interrupt
Timer 18 compare/capture A interrupt
Timer 18 compare/capture B interrupt
Timer 19 overflow/underflow interrupt
Timer 19 compare/capture A interrupt
Timer 19 compare/capture B interrupt
Timer 20 overflow/underflow interrupt
Timer 20 compare/capture A interrupt
Timer 20 compare/capture B interrupt

<Serial Interface>
Serial 0 reception end interrupts
Serial 0 communication/transmission end interrupts
Serial 1 reception end interrupts
Serial 1 communication/transmission end interrupts
Serial 2 reception end interrupts
Serial 2 communication/transmission end interrupts

<PWM>
PWM0 overflow interrupts
PWM0 underflow interrupts
PWM0 synchronous A/D start A
PWM0 synchronous A/D start B
PWM1 overflow interrupts
PWM1 underflow interrupts
PWM1 synchronous A/D start A
PWM1 synchronous A/D start B

<A/D>
A /D 0 conversion end interrupt
A /D 0 conversion end B interrupt
A /D 1 conversion end interrupt
A /D 1 conversion end B interrupt

<DMA>
DMA transfer end interrupt
DMA request after DMA transfer end interrupt
DMA transfer request overflow interrupt

External interrupts(Level interrupt)
MN103SFJ7A : 4 interrupts
MN103SFN0/N4 series : 8 interrupts
MN103SFN1/N5 series : 10 interrupts
MN103SFN2/N6 series : 12 interrupts

External interrupt pins : From IRQ00 to IRQ11
Interrupt detection condition : Each edge, both edges, high-level and low-level detection
Each interrupt detection condition is able to filtering with the noise filter

Timer Counter	8-bit timer	8 sets (MN103SFJ7A, MN103SFN0/N4 series) 12 sets (MN103SFN1/N5, MN103SFN2/N6 series)
	16-bit timer	1 sets (MN103SFJ7A) 2 sets (MN103SFN0/N4 series) 3 sets (MN103SFN1/N5 series) 5 sets (MN103SFN2/N6 series)

Timer 0 (8-bit timer)
- Interval timer, Timer pulse output, Event count, Baud rate timer
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM0IO pin input,
  Timer 1 underflow, Timer 2 underflow

Timer 1 (8-bit timer)
- Interval timer, Timer pulse output, Event count, Baud rate timer,
  Cascade connection (connected to Timer 0)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM1IO pin input,
  Timer 0 underflow, Timer 2 underflow

Timer 2 (8-bit timer)
- Interval timer, Timer pulse output [*1], Event count [*1], Baud rate timer,
  Cascade connection (connected to Timer 1)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM2IO pin input [*1],
  Timer 0 underflow, Timer 1 underflow

Timer 3 (8-bit timer)
- Interval timer, Timer pulse output [*1], Event count [*1], Baud rate timer,
  Cascade connection (connected to Timer 2)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM3IO pin input [*1],
  Timer 0 underflow, Timer 1 underflow, Timer 2 underflow

Timer 4 (8-bit timer)
- Interval timer, Timer pulse output, Event count
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM4IO pin input,
  Timer 5 underflow, Timer 6 underflow

Timer 5 (8-bit timer)
- Interval timer, Timer pulse output, Event count
  Cascade connection (connected to Timer 4)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM5IO pin input,
  Timer 4 underflow, Timer 6 underflow

Timer 6 (8-bit timer)
- Interval timer, Timer pulse output, Event count
  Cascade connection (connected to Timer 5)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM6IO pin input,
  Timer 4 underflow, Timer 5 underflow

Timer 7 (8-bit timer)
- Interval timer, Timer pulse output, Event count
  Cascade connection (connected to Timer 6)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM7IO pin input,
  Timer 4 underflow, Timer 5 underflow, Timer 6 underflow

Timer 8 (8-bit Timer) *2
- Interval timer, Timer pulse output *3, Event count *3
- Count clock source
IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM8IO pin input *3
  Timer 9 underflow, Timer 10 underflow

Timer 9 (8-bit timer) *2
- Interval timer, Timer pulse output *3, Event count *3,
  Cascade connection (Connected to Timer 8)
-Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM9IO pin input *3
Timer 8 underflow, Timer 10 underflow

Timer 10 (8-bit timer) *2
- Interval timer, Timer pulse output, Event count, Cascade connection (Connected to Timer 9)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM10IO pin input
  Timer 8 underflow, Timer 9 underflow

Timer 11 (8-bit timer) *2
- Interval timer, Timer pulse output, Event count, Cascade connection (Connected to Timer 10)
- Count clock source
  IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM11IO pin input
  Timer 8 underflow, Timer 9 underflow, Timer 10 underflow

Timer 16 (16-bit timer)
- Interval timer, Event count, Up/down count, Timer output,
  PWM output, Input capture, one-shot output, External trigger start
  Start by PWMn overflow interrupt, PMWn underflow interrupt,
  A/D conversion start trigger generation
- Count clock source
  IOCLK, IOCLK/8, Timer 6 underflow, Timer 7 underflow, TM16BIO pin input

Timer 17 (16-bit timer) *2 *4
- Interval timer, Event count, Up/down count, Timer output,
  PWM output, Input capture, one-shot output, External trigger start
- Count clock source
  IOCLK, IOCLK/8, IOCLK/64, Timer 11 underflow, TM17BIO pin input

Timer 18 (16-bit timer) *5
- Interval timer, Event count, Up/down count, Timer output,
  PWM output (output to 6 ports all at once is possible), Input capture, one-shot output,
  External trigger start
- Count clock source
  IOCLK, IOCLK/8, IOCLK/64, Timer 7 underflow,
  TM18BIO pin input

Timer 19 (16-bit timer) *2
- Interval timer, Event count, Up/down count, Timer output,
  PWM output, Input capture, one-shot output, External trigger start
  Start by PWMn overflow interrupt, PWMn underflow interrupt,
  A/D conversion start trigger generation
- Count clock source
  IOCLK, IOCLK/8, Timer 10 underflow, Timer 11 underflow,
  TM19BIO pin input

Timer 20 (16-bit timer) *2 *4
- Interval timer, Event count, Up/down count, Timer output,
  PWM output, Input capture, one-shot output, External trigger start,
- Count clock source
  IOCLK, IOCLK/8, Timer 6 underflow,
  Timer 7 underflow, TM20BIO pin input

*1 The function using the TMnIO pin (n=2, 3) cannot be used by the MN103SFN0/N4 series.
*2 There is not the function in the MN103SFN0/N4 series.
*3 The function using the TMnIO pin (n=8, 9) cannot be used by the MN103SFN1/N5 series.
*4 There is not the function in the MN103SFN1/N5 series.
*5 There is not the function in the MN103SFJ7A.

Watchdog Timer
Detection time 6.55 ms to 1677.72 ms (oscillation frequency 10 MHz)
Generates non-maskable interrupt at detection
Generates hard-reset at second consective overflow

A /D Converter
A/D0
- Resolution 10 bits
- Minimum conversion time 0.5 µs
- Analog input 5 channels (AD0IN00 to AD1IN04)
- A/D conversion start trigger is in synchronization with complementary 3-phase PWM cycle and 16-bit timer

A/D1
- Resolution 10 bits
- Minimum conversion time 0.5 µs
- Analog input 5 channels (AD0IN00 to AD1IN04)
  MN103SFJ7A : 3 channels (AD1IN00 to AD1IN02)
  MN103SFN0/N4 series: 3 channels (AD1IN00 to AD1IN02)
  MN103SFN1/N5 series: 7 channels (AD1IN00 to AD1IN06)
  MN103SFN2/N6 series: 11 channels (AD1IN00 to AD1IN10)
- A/D conversion start trigger is in synchronization with complementary 3-phase PWM cycle and 16-bit timer

Complementary 3-phase PWM output
- Min. resolution: 16.7 ns
- Triangular and saw-tooth waves output
- Incorporates a dead time insertion circuit
- Can overwrite registers by double buffer during PWM operation
- PWM output protection circuit supporting external interrupts and non-maskable interrupt
- Output timing varying function
  A/D conversion start trigger, 16-bit timer start trigger

VGA
- VGA
  MN103SFN4 series 1 sets
  MN103SFN5/N6 series 2 sets
- The gain of eight stages can be set (2.05, 3.03, 4.00, 4.98, 5.96, 7.90, 9.83, and 19.40times)
- Offset voltage cancel cansel function(short-circuit or switching)

Serial Interface 3 channels

Serial 0 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface
-Overrun error detection
-Transfer clock source
1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 3 underflow,
IOCLK/2, IOCLK/4,
SBT0 pin
-Can be selected as the first bit to be transferred,
Any transfer size from 2 to 8 bits can be selected.
-Can be continuously transmitted, received or transmitted and received.
-Maximum transfer rate: 5.0 Mbps

Full duplex UART
- Parity check, Overrun and flaming error detection
- Transfer clock source
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 0 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 1 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 2 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 3 underflow,
IOCLK/16, IOCLK/32, IOCLK/64
- Can be selected as the first bit to be transferred,
Any transfer size from 7 to 8 bits can be selected.
- Continuous transmission, reception, and transmission/reception
- Maximum transfer rate: 300 kbps

Serial 1 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface
- Overrun error detection
- Transfer clock source
1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 3 underflow,
IOCLK/2, IOCLK/4,
SBT1 pin
- Can be selected as the first bit to be transferred,
Any transfer size from 2 to 8 bits can be selected.
- Continuous transmission, reception, and transmission/reception
- Maximum transfer rate: 5.0 Mbps

Full duplex UART
- Parity check, Overrun and flaming error detection
- Transfer clock source
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 0 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 1 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 2 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 3 underflow,
IOCLK/16, IOCLK/32, IOCLK/64
- Can be selected as the first bit to be transferred,
Any transfer size from 7 to 8 bits can be selected.
- Continuous transmission, reception, and transmission/reception
- Maximum transfer rate: 300 kbps

Serial 2 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
-Overrun error detection
-Transfer clock source
1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 3 underflow,
IOCLK/2, IOCLK/4,
SBT2 pin
- Can be selected as the first bit to be transferred,
Any transfer size from 2 to 8 bits can be selected.
- Continuous transmission, reception and transmission / reception
- Maximum transfer rate: 5.0 Mbps
- Corresponding to the 4 channel system communication and the SPI communication

Full duplex UART
- Parity check, Overrun and flaming error detection
- Transfer clock source
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 0 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 1 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 2 underflow,
1/16, 1/32, 1/64, 1/128, 1/256, 1/512 and 1/1024 of timer 3 underflow,
IOCLK/16, IOCLK/32, IOCLK/64
- Can be selected as the first bit to be transferred,
Any transfer size from 7 to 8 bits can be selected.
- Continuous transmission, reception and transmission / reception
- Maximum transfer rate: 300 kbps

Regulator incorporates regulator, and use of 5 V power supply is possible

Power Supply Detection
Detection level 3.6 V to 4.3 V
When power supply voltage is under detection level, reset is generated.

MN103SFJ7A

Port / pins	
I/O ports	28 pins
Motor control output	6 pins
External interrupt	4 pins
A/D input	6 pins
Input ports	
A/D input	2 pins
Special pins	14 pins
Reset input pin	1 pin
Oscillation pin	2 pins
Mode pin	2 pins
Debug pin	2 pins
Power pin	7 pins
Package	TQFP048 (7 mm square, 0.5 mm pitch)

MN103SFN0/N4 series

Port / pins	
I/O ports	28 pins
Motor control output	6 pins
External interrupt	8 pins
A/D input	6 pins
Input ports	
VGA, A/D input	2 pins
Special pins	14 pins
Reset input pin	1 pin
Oscillation pin	2 pins
Mode pin	2 pins
Debug pin	2 pins
Power pin	7 pins
Package	QFP044 (10 mm square, 0.8 mm pitch)
	TQFP048 (7 mm square, 0.5 mm pitch)

MN103SFN1/N5 series

Port / pins	
I/O ports	46 pins
Motor control output	12 pins
External interrupt	10 pins
A/D input	8 pins
Input ports	
VGA, A/D input	4 pins
Special pins1	4 pins
Reset input pin	1 pin
Oscillation pin	2 pins
Mode pin	2 pins
Debug pin	2 pins
Power pin	7 pins
Package	TQFP064 (10 mm square, 0.5 mm pitch)
	LQFP064 (14 mm square, 0.8 mm pitch)

MN103SFN2/N6 series

Port / pins	
I/O ports	60 pins
Motor control output	12 pins
External interrupt	12 pins
A/D input	12 pins
Input ports	
VGA, A/D input	4 pins
Special pins1	6 pins
Reset input pin	1 pin
Oscillation pin	2 pins
Mode pin	2 pins
Debug pin	2 pins
Power pin	9 pins
Package	TQFP080 (12 mm square, 0.5 mm pitch)

1.3 Pin Description

1.3.1 Pin Configuration

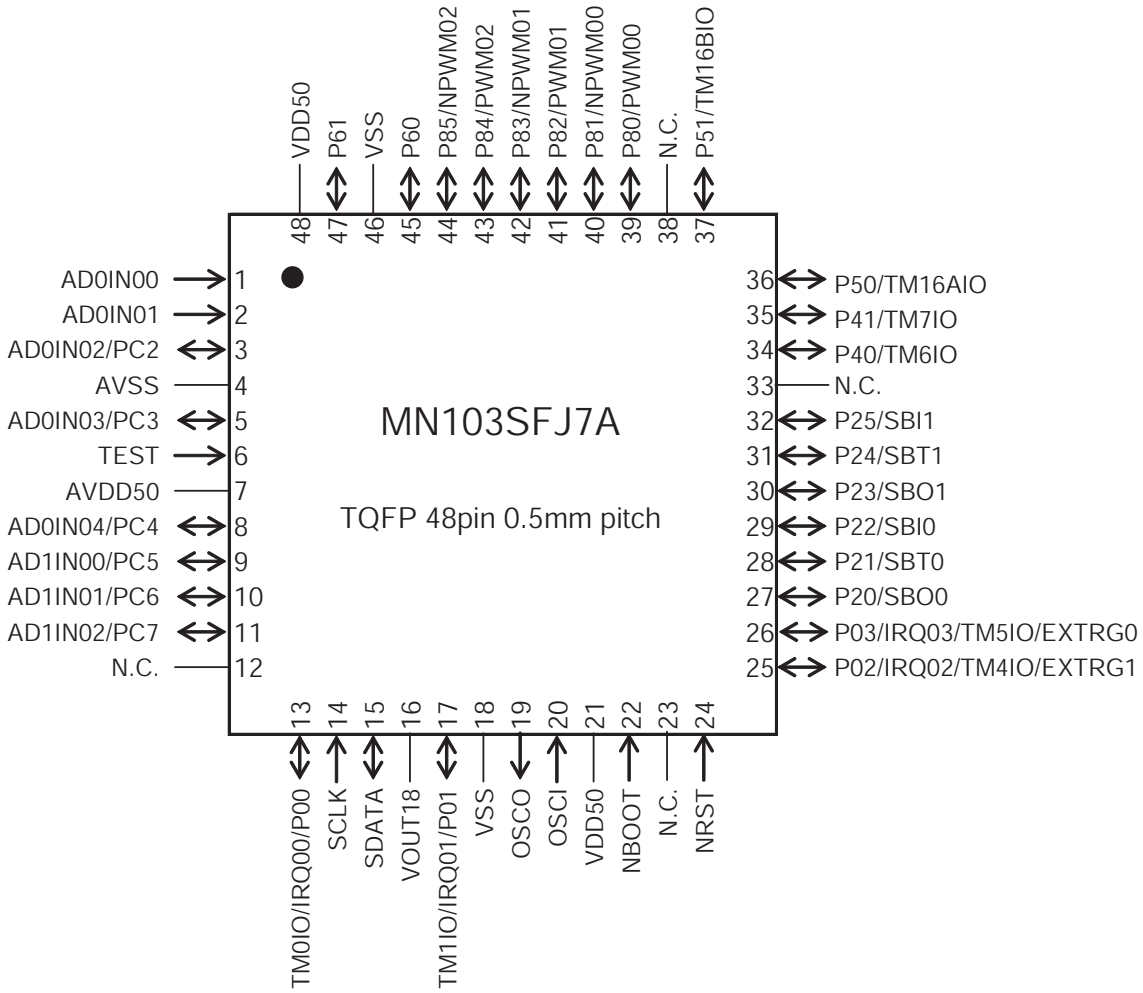
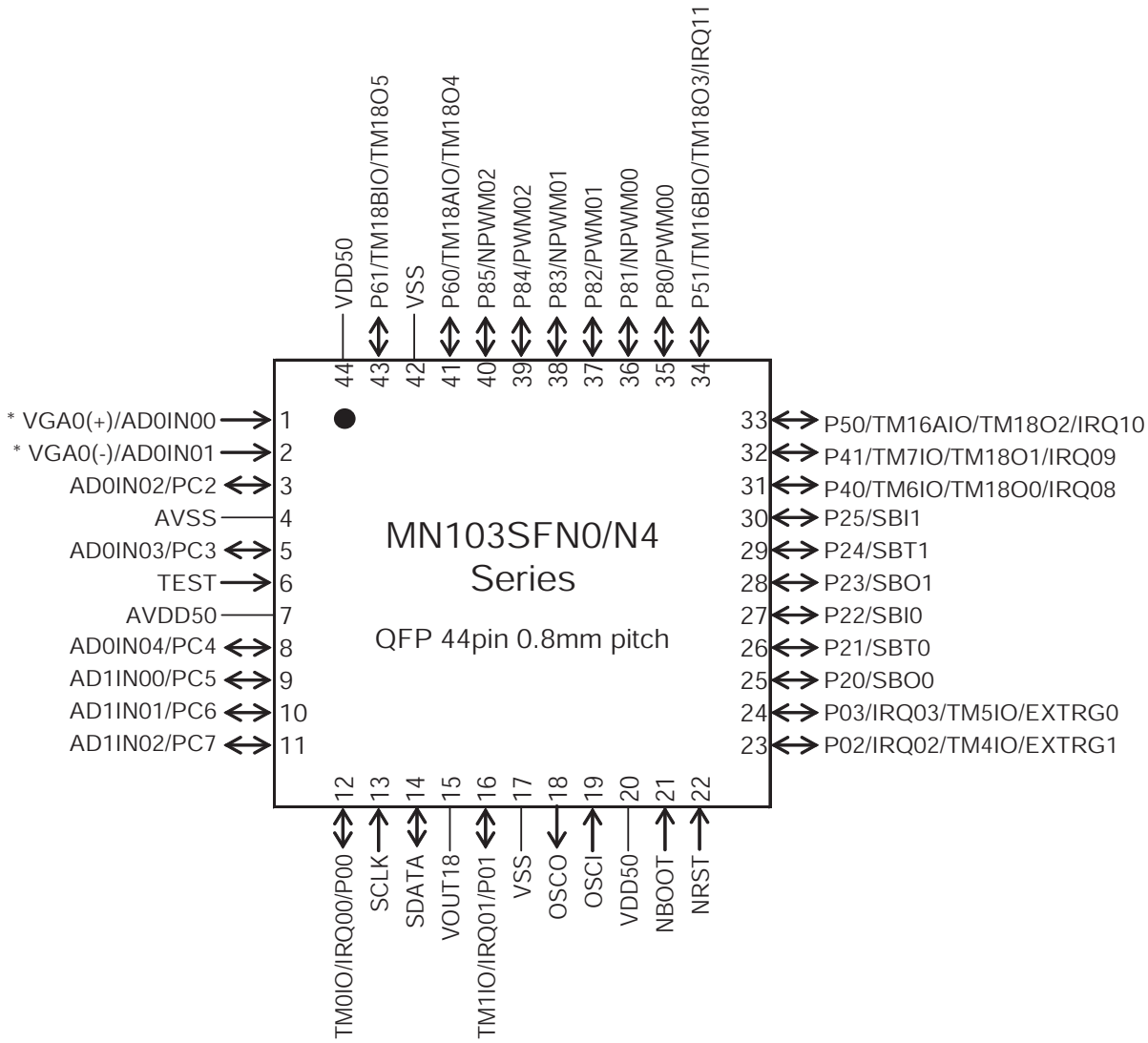
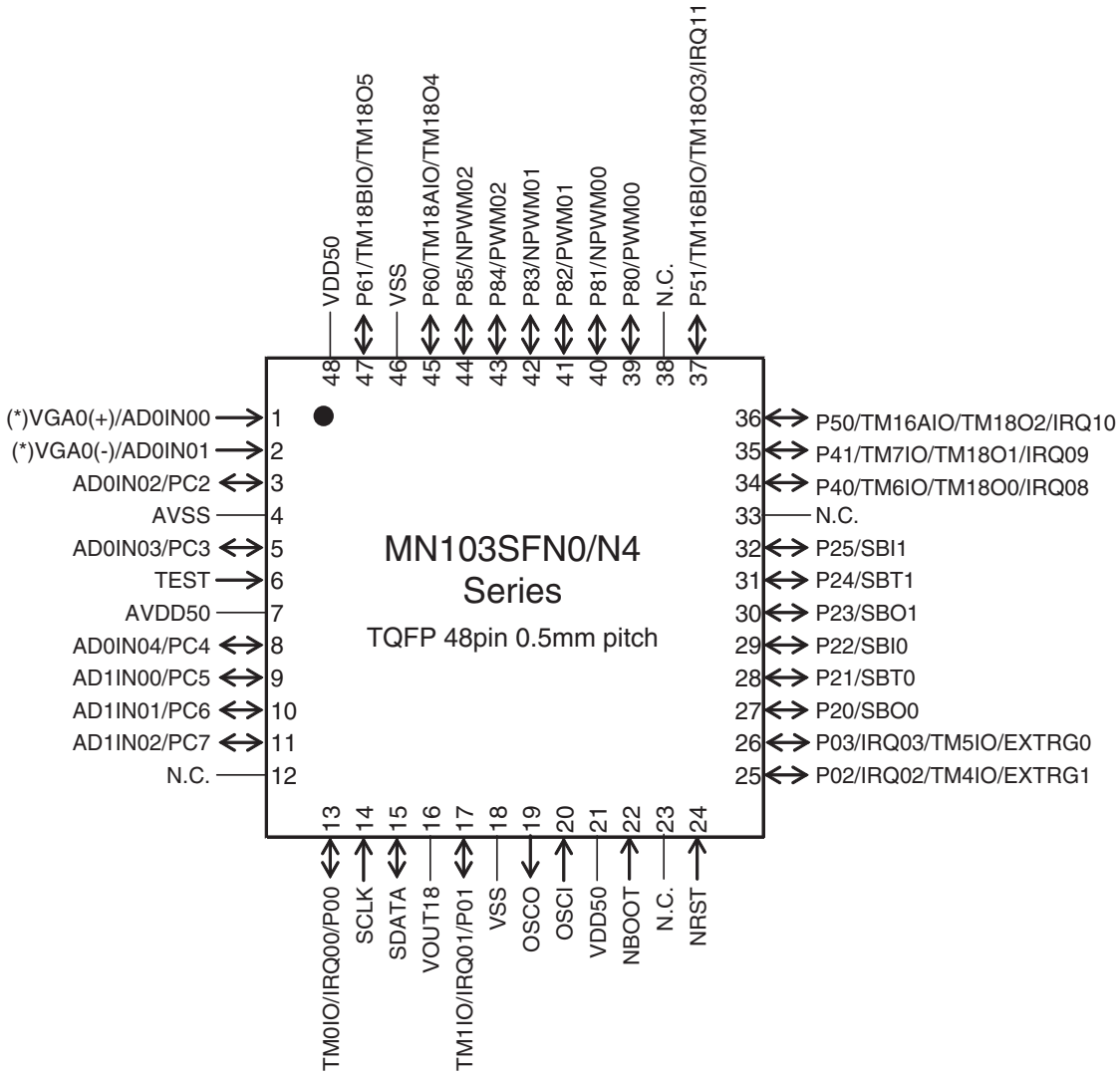


Figure:1.3.1 Pin Configuration (MN103SFJ7A)



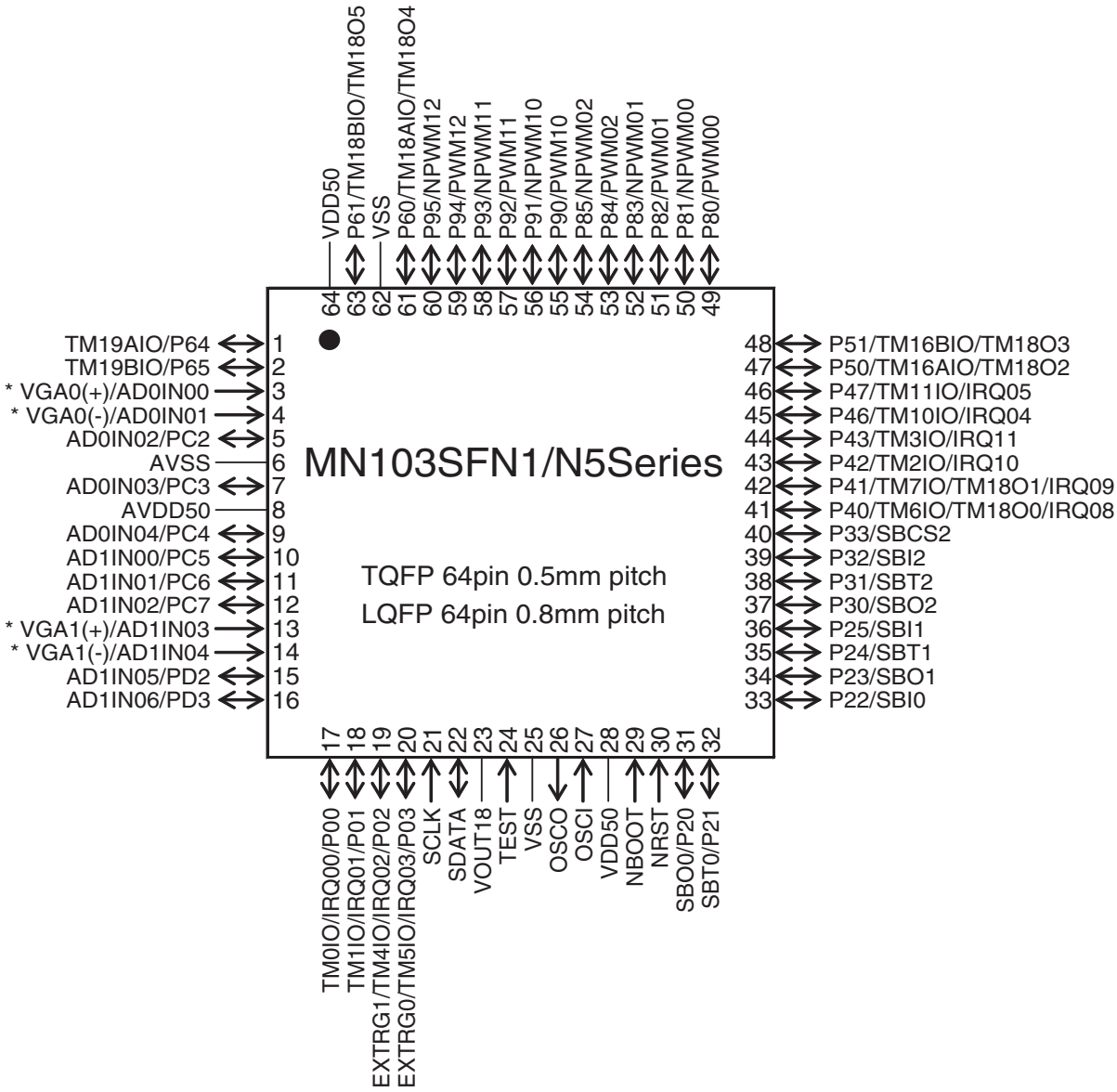
* VGA is not in the MN103SFN0 series.
1,2 pin of MN103SFN0 series are the dedicated input pin for A/D converter.

Figure:1.3.2 Pin Configuration (MN103SFN0/N4 series QFP 44 pin)



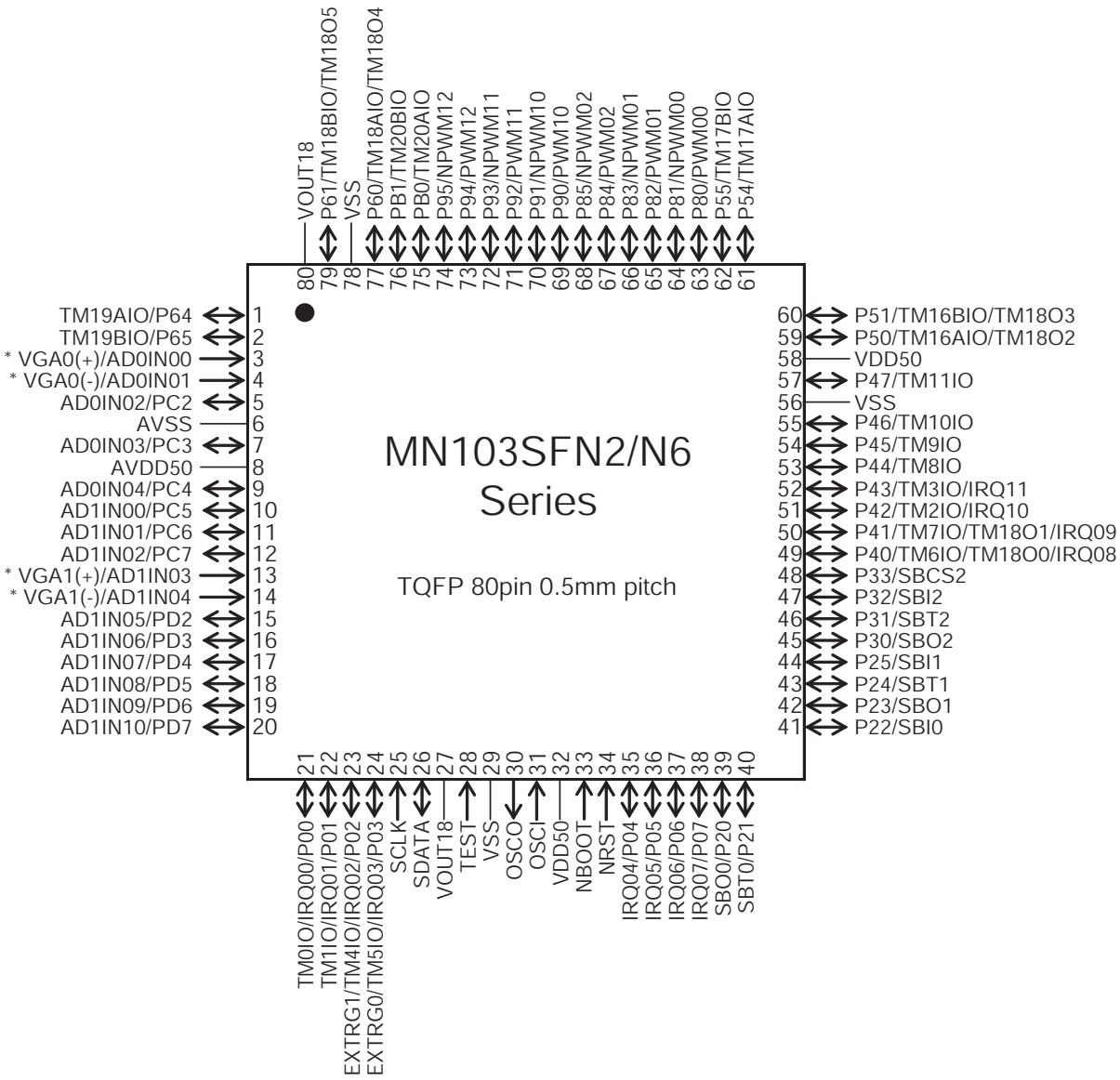
* VGA is not in the MN103SFN0 series.
1,2 pin of MN103SFN0 series are the dedicated input pin for A/D converter.

Figure:1.3.3 Pin Configuration (MN103SFN0/N4 series TQFP 48 pin)



* VGA is not in the MN103SFN1 series.
3,4,13,14 pin of MN103SFN1 series are the dedicated input pin for A/D converter.

Figure:1.3.4 Pin Configuration (MN103SFN1/N5 series)



* VGA is not in the MN103SFN2 series.
3,4,13,14 pin of MN103SFN2 series are the dedicated input pin for A/D converter.

Figure:1.3.5 Pin Configuration (MN103SFN2/N6 series)

1.3.2 Pin Specification

Table:1.3.1 Pin Specification

PIN	Special function	MN103SFJ7A	MN103SFN0/N4 series	MN103SFN1/N5 series	MN103SFN2/N6 series	I/O	Direction control	Pull-up control	Functions
NRST	-	O	O	O	O	in	-	-	
P00	IRQ00	O	O	O	O	in/out	P0DIR0	P0PLU0	External interrupt input 0
	TM0IO	O	O	O	O				Timer 0 I/O
P01	IRQ01	O	O	O	O	in/out	P0DIR1	P0PLU1	External interrupt input 1
	TM1IO	O	O	O	O				Timer 1 I/O
P02	IRQ02	O	O	O	O	in/out	P0DIR2	P0PLU2	External interrupt input 2
	TM4IO	O	O	O	O				Timer 4 I/O
	EXTRG1	O	O	O	O				External trigger input 1 for debugger
P03	IRQ03	O	O	O	O	in/out	P0DIR3	P0PLU3	External interrupt input 3
	TM5IO	O	O	O	O				Timer 5 I/O
	EXTRG0	O	O	O	O				External trigger input 0 for debugger
P04	IRQ04	-	-	-	O	in/out	P0DIR4	P0PLU4	External interrupt input 4
P05	IRQ05	-	-	-	O	in/out	P0DIR5	P0PLU5	External interrupt input 5
P06	IRQ06	-	-	-	O	in/out	P0DIR6	P0PLU6	External interrupt input 6
P07	IRQ07	-	-	-	O	in/out	P0DIR7	P0PLU7	External interrupt input 7
P20	SBO0	O	O	O	O	in/out	P2DIR0	P2PLU0	Serial 0 transmission data output
P21	SBT0	O	O	O	O	in/out	P2DIR1	P2PLU1	Serial 0 clock I/O
P22	SBI0	O	O	O	O	in/out	P2DIR2	P2PLU2	Serial 0 reception data input
P23	SBO1	O	O	O	O	in/out	P2DIR3	P2PLU3	Serial 1 transmission data output
P24	SBT1	O	O	O	O	in/out	P2DIR4	P2PLU4	Serial 1 clock I/O
P25	SBI1	O	O	O	O	in/out	P2DIR5	P2PLU5	Serial 1 reception data input
P30	SBO2	-	-	O	O	in/out	P3DIR0	P3PLU0	Serial 2 transmission data output
P31	SBT2	-	-	O	O	in/out	P3DIR1	P3PLU1	Serial 2 clock I/O
P32	SBI2	-	-	O	O	in/out	P3DIR2	P3PLU2	Serial 2 reception data input
P33	SBCS2	-	-	O	O	in/out	P3DIR3	P3PLU3	Serial 2 chip select I/O
P40	IRQ08	-	O	O	O	in/out	P4DIR0	P4PLU0	External interrupt input 8
	TM6IO	O	O	O	O				Timer 6 I/O
	TM18O0	-	O	O	O				Timer 18 output 0
P41	IRQ09	-	O	O	O	in/out	P4DIR1	P4PLU1	External interrupt input 9
	TM7IO	O	O	O	O				Timer 7 I/O
	TM18O1	-	O	O	O				Timer 18 output 1
P42	IRQ10	-	-	O	O	in/out	P4DIR2	P4PLU2	External interrupt input 10
	TM2IO	-	-	O	O				Timer 2 I/O
P43	IRQ11	-	-	O	O	in/out	P4DIR3	P4PLU3	External interrupt input 11
	TM3IO	-	-	O	O				Timer 3 I/O
P44	TM8IO	-	-	-	O	in/out	P4DIR4	P4PLU4	Timer 8 I/O
P45	TM9IO	-	-	-	O	in/out	P4DIR5	P4PLU5	Timer 9 I/O
P46	TM10IO	-	-	O	O	in/out	P4DIR6	P4PLU6	Timer 10 I/O
	IRQ04	-	-	O	-				External interrupt input 4
P47	TM11IO	-	-	O	O	in/out	P4DIR7	P4PLU7	Timer 11 I/O
	IRQ05	-	-	O	-				External interrupt input 5
P50	TM16AIO	O	O	O	O	in/out	P5DIR0	P5PLU0	Timer 16 A I/O
	TM18O2	-	O	O	O				Timer 18 output 0
	IRQ10	-	O	-	-				External interrupt input 10

PIN	Special function	MN103SFJ7A	MN103SFN0/N4 series	MN103SFN1/N5 series	MN103SFN2/N6 series	I/O	Direction control	Pull-up control	Functions
P51	TM16BIO	O	O	O	O	in/out	P5DIR1	P5PLU1	Timer 16 B I/O
	TM18O3	-	O	O	O				Timer 18 output 1
	IRQ11	-	O	-	-				External interrupt input 11
P54	TM17AIO	-	-	-	O	in/out	P5DIR4	P5PLU4	Timer 17 A I/O
P55	TM17BIO	-	-	-	O	in/out	P5DIR5	P5PLU5	Timer 17 B I/O
P60	-	O	-	-	-	in/out	P6DIR0	P6PLU0	No function
	TM18AIO	-	O	O	O				Timer 18 A I/O
	TM18O4	-	O	O	O				Timer 18 output 4
P61	-	O	-	-	-	in/out	P6DIR1	P6PLU1	No function
	TM18BIO	-	O	O	O				Timer 18 B I/O
	TM18O5	-	O	O	O				Timer 18 output 5
P64	TM19AIO	-	-	O	O	in/out	P6DIR4	P6PLU4	Timer 19 A I/O
P65	TM19BIO	-	-	O	O	in/out	P6DIR5	P6PLU5	Timer 19 B I/O
P80	PWM00	O	O	O	O	in/out	P8DIR0	P8PLU0	3-phase PWM0 signal output 0
P81	NPWM00	O	O	O	O	in/out	P8DIR1	P8PLU1	3-phase PWM0 signal inversion output 0
P82	PWM01	O	O	O	O	in/out	P8DIR2	P8PLU2	3-phase PWM0 signal output 1
P83	NPWM01	O	O	O	O	in/out	P8DIR3	P8PLU3	3-phase PWM0 signal inversion output 1
P84	PWM02	O	O	O	O	in/out	P8DIR4	P8PLU4	3-phase PWM0 signal output 2
P85	NPWM02	O	O	O	O	in/out	P8DIR5	P8PLU5	3-phase PWM0 signal inversion output 2
P90	PWM10	-	-	O	O	in/out	P9DIR0	P9PLU0	3-phase PWM1 signal output 0
P91	NPWM10	-	-	O	O	in/out	P9DIR1	P9PLU1	3-phase PWM1 signal inversion output 0
P92	PWM11	-	-	O	O	in/out	P9DIR2	P9PLU2	3-phase PWM1 signal output 1
P93	NPWM11	-	-	O	O	in/out	P9DIR3	P9PLU3	3-phase PWM1 signal inversion output 1
P94	PWM12	-	-	O	O	in/out	P9DIR4	P9PLU4	3-phase PWM1 signal output 2
P95	NPWM12	-	-	O	O	in/out	P9DIR5	P9PLU5	3-phase PWM1 signal inversion output 2
PB0	TM20AIO	-	-	-	O	in/out	PBDIR0	PBPLU0	Timer 20 A I/O
PB1	TM20BIO	-	-	-	O	in/out	PBDIR1	PBPLU1	Timer 20 B I/O
-	AD0IN00	O	O	O	O	in	-	-	A/D converter analog input 0
	VGA0(+)*	-	O	O	O				VGA analog input 0(+)
-	AD0IN01	O	O	O	O	in	-	-	A/D converter analog input 1
	VGA0(-)*	-	O	O	O				VGA analog input 0(-)
PC2	AD0IN02	O	O	O	O	in/out	PCDIR2	PCPLU2	A/D converter analog input 2
PC3	AD0IN03	O	O	O	O	in/out	PCDIR3	PCPLU3	A/D converter analog input 3
PC4	AD0IN04	O	O	O	O	in/out	PCDIR4	PCPLU4	A/D converter analog input 4
PC5	AD1IN00	O	O	O	O	in/out	PCDIR5	PCPLU5	A/D converter analog input 5
PC6	AD1IN01	O	O	O	O	in/out	PCDIR6	PCPLU6	A/D converter analog input 6
PC7	AD1IN02	O	O	O	O	in/out	PCDIR7	PCPLU7	A/D converter analog input 7
-	AD1IN03	-	-	O	O	in	-	-	A/D converter analog input 8
	VGA1(+)*	-	-	O	O				VGA analog input 1(+)
-	AD1IN04	-	-	O	O	in	-	-	A/D converter analog input 9
	VGA1(-)*	-	-	O	O				VGA analog input 1(-)
PD2	AD1IN05	-	-	O	O	in/out	PDDIR2	PDPLU2	A/D converter analog input 10
PD3	AD1IN06	-	-	O	O	in/out	PDDIR3	PDPLU3	A/D converter analog input 11
PD4	AD1IN07	-	-	-	O	in/out	PDDIR4	PDPLU4	A/D converter analog input 12
PD5	AD1IN08	-	-	-	O	in/out	PDDIR5	PDPLU5	A/D converter analog input 13
PD6	AD1IN09	-	-	-	O	in/out	PDDIR6	PDPLU6	A/D converter analog input 14
PD7	AD1IN10	-	-	-	O	in/out	PDDIR7	PDPLU7	A/D converter analog input 15

* The VGA analog input pin is not in MN103SFJ7A and MN103SFN0/N1/N2 series.

1.3.3 Pin Functions (MN103SFJ7A)

Table:1.3.2 Pin Functions (MN103SFJ7A)

Name	Pin No.	I/O	Other Function	Function	Description
VDD50 VDD50	21 48	-	-	Power supply pin	Power pin for 5 V, digital IO Supply 5 V to all of pins and connect 1 μF capacitor or more between all of the VDD50 and VSS pins. (Put the capacitor near the pins.)
VOUT18	16	-	-	Power output pin	Power pin for 1.8 V, digital IO Connect 1 μF capacitor between all of the VOUT18 and VSS pins. (Put the capacitor near the pins.)
VSS VSS	18 46	-	-	Power supply pin	GND for digital
AVDD50	7	-	-	Power supply pin for A/D	Power for A/D. Supply 5 V to AVDD50 pin and connect 1 μF capacitor or more between AVDD50 and AVSS pins. (Put the capacitor near the pins.)
AVSS	4	-	-	Power supply pin for A/D	GND for A/D
NBOOT	22	Input	-	Start area change pin	Use this pin when the start-up area of ROM is changed. Please add the pull-up resistor of 2 kΩ usually.
OSCI OSCO	20 19	Input Output	-	Clock input pin Clock output pin	Oscillator pins for connecting with ceramic oscillator or crystal oscillator. When inputting clock externally, input from OSCI and open OSCO.
NRST	24	Input	-	Reset pins (negative logic)	Pin for power-on reset. Internal pull-up resistors are contained. When this pin is at “L” level, internal state of LSI is initialized. After that, when the input is set to “H” level, reset is cancelled. After oscillation stabilization time by hardware, reset proccessing is executed. Connect 0.1 μF capacitor or more between NRST and VSS pins.
P00 P01 P02 P03	13 17 25 26	I/O	IRQ00/TM0IO IRQ01/TM1IO IRQ02/TM4IO/EXTRG1 IRQ03/TM5IO/EXTRG0	I/O port 0	4-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode (P00 to P03) is selected, and pull-up resistor is disable.
P20 P21 P22 P23 P24 P25	27 28 29 30 31 32	I/O	SBO0 SBT0 SBI0 SBO1 SBT1 SBI1	I/O port 2	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode (P20 to P25) is selected, and pull-up resistor is disable.
P40 P41	34 35	I/O	TM6IO TM7IO	I/O port 4	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up resistor for each bit can be selected individually by the P4PLU register. At reset, the input mode (P40, P41) is selected and pull-up resistor is disable.
P50 P51	36 37	I/O	TM16AIO TM16BIO	I/O port 5	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, the input mode (P50, P51) is selected and pull-up resistor is disable.

Name	Pin No.	I/O	Other Function	Function	Description
P60 P61	45 47	I/O	-	I/O port 6	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode (P60, P61) is selected and pull-up resistor is disable.
P80 P81 P82 P83 P84 P85	39 40 41 42 43 44	I/O	PWM00 NPWM00 PWM01 NPWM01 PWM02 NPWM02	I/O port 8	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode (P80 to P85) is selected and pull-up resistor is disable.
PC2 PC3 PC4 PC5 PC6 PC7	3 5 8 9 10 11	I/O	AD0IN02 AD0IN03 AD0IN04 AD1IN00 AD1IN01 AD1IN02	I/O port C	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the PCDIR register. A pull-up resistor for each bit can be selected individually by the PCPLU register. At reset, the input mode (PC2 to PC7) is selected and pull-up resistor is disable.
SBO0 SBO1	27 30	Output	P20 P23	Serial interface transmission output pin	Transmission data output pins for serial interface 0 and 1. Select output mode by the P2DIR register and serial pin function by the P2MD register. These can be used as normal I/O pins when the serial interface is not used.
SBI0 SBI1	29 32	Input	P22 P25	Serial interface reception data input pin	Reception data input pins for serial interface 0 and 1. Pull-up resistor can be selected by the P2PLU register. Select input mode by the P2DIR register and serial pin function by the P2MD register. These can be used as normal I/O pins when the serial interface is not used.
SBT0 SBT1	28 31	I/O	P21 P24	Serial interface clock I/O pin	Clock I/O pins for serial interface 0 and 1. Pull-up resistor can be selected by the P2PLU register. Select I/O mode by the P2DIR register and serial pin function by the P2MD register. These can be used as normal I/O pins when the serial interface is not used.
TM0IO TM1IO TM4IO TM5IO TM6IO TM7IO	13 17 25 26 34 35	I/O	P00 P01 P02 P03 P40 P41	Timer I/O pin	Event counter input and timer pulse output pin for 8-bit timer 0, 1, 4, 5, 6 and 7. To use this pin as event counter input, select timer input pin by P0MD, P4MD1 register and select input mode by the P0DIR and P4DIR registers. In input mode, pull-up resistor can be selected by the P0PLU and P4PLU registers. To use this pin as timer pulse output, select timer output pin by the P0MD and P4MD1 registers and set to output mode by the P0DIR and P4DIR registers. These can be used as normal I/O pins when these are not used as timer I/O pins.
TM16AIO TM16BIO	36 37	I/O	P50 P51	Timer I/O pin	Event counter input, timer output, and PWM output pin for 16-bit timer 16. To use this pin as event counter input, select input mode by the P5MD1 register, and set to input mode by the P5DIR register. In input mode, pull-up resistor can be selected by the P5PLU register. To use this as timer output and PWM output, select timer output pin by the P5MD1 register, and set to output mode by the P5DIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.

Name	Pin No.	I/O	Other Function	Function	Description
AD0IN00 AD0IN01 AD0IN02 AD0IN03 AD0IN04 AD1IN00 AD1IN01 AD1IN02	1 2 3 5 8 9 10 11	Input	 PC2 PC3 PC4 PC5 PC6 PC7	Analog input pin	Analog input pins for 1-type 8-channel, 10-bit A/D converters. These can be used as normal I/O pins when these are not used as analog input. However, AD0IN00 and AD0IN01 are excluded.
IRQ00 IRQ01 IRQ02 IRQ03	13 17 25 26	Input	P00 P01 P02 P03	External interrupt pin	External interrupt input pins. The valid edge can be selected. Set whether both edges are detected or not by IRQEDGESEL register. When it is set not to detect both edges, select rising edge, falling edge, High-level, or Low-level by EXTMD0 registers. When it is set to detect both edges, select rising edge by the external interrupt condition setting register.
PWM00 PWM01 PWM02	39 41 43	Output	P80 P82 P84	Motor control PWM signal output pin	Motor control 3-phase PWM signal output pin Select PWM signal output pin by the P8MD register and enable PWM output by the PWMOFF0A register. These can be used as normal I/O pins when these pins are not used as PWM signal output pin.
NPWM00 NPWM01 NPWM02	40 42 44	Output	P81 P83 P85	Motor control PWM signal reverse output pin	Motor control 3-phase PWM signal inversion output pin. Select PWM signal output pin by the P8MD register and enable PWM output by the PWMOFF0A register. These can be used as normal I/O pins when these is not used as PWM signal output pin.
EXTRG0 EXTRG1	26 25	Output	P03/IRQ03/TM5IO P02/IRQ02/TM4IO	External trigger output pins for debugger	External trigger pins for debugger. Please connect it with the trigger pin of the debugger when you use the trigger function.
TEST	6	Input	-	Teset signal input pin	Input pin for test signal input. Connect pull-up resistor of 2 kΩ or more. (Put the resistor near the pins.)
SCLK SDATA	14 15	Input I/O	-	On-chip debugger I/O pins	Clock input and data I/O pins for on-chip debugger. Connect pull-up resistor of 2 kΩ or more.

1.3.4 Pin Functions (MN103SFN0/N4 series)

Table:1.3.3 Pin Functions (MN103SFN0/N4 series)

Name	Pin No.		I/O	Other Function	Function	Description
	QFP 44	TQFP 48				
VDD50 VDD50	20 44	21 48	-	-	Power supply pin	Power pin for 5 V, digital IO Supply 5 V to all of pins and connect 1 μF capacitor or more between all of the VDD50 and VSS pins. (Put the capacitor near the pins.)
VOUT18	15	16	-	-	Power output pin	Power pin for 1.8 V, digital IO Connect 1 μF capacitor between all of the VOUT18 and VSS pins. (Put the capacitor near the pins.)
VSS VSS	17 42	18 46	-	-	Power supply pin	GND for digital
AVDD50	7	7	-	-	Power supply pin for A/D	Power for A/D. Supply 5 V to AVDD50 pin and connect 1 μF capacitor or more between AVDD50 and AVSS pins. (Put the capacitor near the pins.)
AVSS	4	4	-	-	Power supply pin for A/D	GND for A/D
NBOOT	21	22	Input	-	Start area change pin	Use this pin when the start-up area of ROM is changed. Please add the pull-up resistor of 2 kΩ usually.
OSCI OSCO	19 18	20 19	Input Output	-	Clock input pin Clock output pin	Oscillator pins for connecting with ceramic oscillator or crystal oscillator. When inputting clock externally, input from OSCI and open OSCO.
NRST	22	24	Input	-	Reset pins (negative logic)	Pin for power-on reset. Internal pull-up resistors are contained. When this pin is at “L” level, internal state of LSI is initialized. After that, when the input is set to “H” level, reset is cancelled. After oscillation stabilization time by hardware, reset proccessing is executed. Connect 0.1 μF capacitor or more between NRST and VSS pins.
P00 P01 P02 P03	12 16 23 24	13 17 25 26	I/O	IRQ00/TM0IO IRQ01/TM1IO IRQ02/TM4IO/EXTRG1 IRQ03/TM5IO/EXTRG0	I/O port 0	4-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode (P00 to P03) is selected, and pull-up resistor is disable.
P20 P21 P22 P23 P24 P25	25 26 27 28 29 30	27 28 29 30 31 32	I/O	SBO0 SBT0 SBI0 SBO1 SBT1 SBI1	I/O port 2	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode (P20 to P25) is selected, and pull-up resistor is disable.
P40 P41	31 32	34 35	I/O	IRQ08/TM6IO/TM18O0 IRQ09/TM7IO/TM18O1	I/O port 4	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up resistor for each bit can be selected individually by the P4PLU register. At reset, the input mode (P40, P41) is selected and pull-up resistor is disable.
P50 P51	33 34	36 37	I/O	IRQ10/TM16AIO/ TM18O2 IRQ11/TM16BIO/ TM18O3	I/O port 5	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, the input mode (P50, P51) is selected and pull-up resistor is disable.

Name	Pin No.		I/O	Other Function	Function	Description
	QFP 44	TQFP 48				
P60 P61	41 43	45 47	I/O	TM18AIO/TM18O4 TM18BIO/TM18O5	I/O port 6	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode (P60, P61) is selected and pull-up resistor is disable.
P80 P81 P82 P83 P84 P85	35 36 37 38 39 40	39 40 41 42 43 44	I/O	PWM00 NPWM00 PWM01 NPWM01 PWM02 NPWM02	I/O port 8	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode (P80 to P85) is selected and pull-up resistor is disable.
PC2 PC3 PC4 PC5 PC6 PC7	3 5 8 9 10 11	3 5 8 9 10 11	I/O	AD0IN02 AD0IN03 AD0IN04 AD1IN00 AD1IN01 AD1IN02	I/O port C	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the PCDIR register. A pull-up resistor for each bit can be selected individually by the PCPLU register. At reset, the input mode (PC2 to PC7) is selected and pull-up resistor is disable.
SBO0 SBO1	25 28	27 30	Output	P20 P23	Serial interface transmission output pin	Transmission data output pins for serial interface 0 and 1. Select output mode by the P2DIR register and serial pin function by the P2MD register. These can be used as normal I/O pins when the serial interface is not used.
SBI0 SBI1	27 30	29 32	Input	P22 P25	Serial interface reception data input pin	Reception data input pins for serial interface 0 and 1. Pull-up resistor can be selected by the P2PLU register. Select input mode by the P2DIR register and serial pin function by the P2MD register. These can be used as normal I/O pins when the serial interface is not used.
SBT0 SBT1	26 29	28 31	I/O	P21 P24	Serial interface clock I/O pin	Clock I/O pins for serial interface 0 and 1. Pull-up resistor can be selected by the P2PLU register. Select I/O mode by the P2DIR register and serial pin function by the P2MD register. These can be used as normal I/O pins when the serial interface is not used.
TM0IO TM1IO TM4IO TM5IO TM6IO TM7IO	12 16 23 24 31 32	13 17 25 26 34 35	I/O	P00 P01 P02 P03 P40 P41	Timer I/O pin	Event counter input and timer pulse output pin for 8-bit timer 0, 1, 4, 5, 6 and 7. To use this pin as event counter input, select timer input pin by the P0MD and P4MD1 registers and set to input mode by the P0DIR and P4DIR registers. In input mode, pull-up resistor can be selected by the P0PLU and P4PLU registers. To use this pin as timer pulse output, select timer output pin by the P0MD, P4MD1 and P4MD2 registers and set to output mode by the P0DIR and P4DIR registers. These can be used as normal I/O pins when these are not used as timer I/O pins.

Name	Pin No. QFP 44	Pin No. TQFP 48	I/O	Other Function	Function	Description
TM16AIO TM16BIO TM18AIO TM18BIO	33 34 41 43	36 37 45 47	I/O	P50 P51 P60 P61	Timer I/O pin	Event counter input, timer output, and PWM output pin for 16-bit timer 16 and 18. To use this pin as event counter input, select timer input pin by the P5MD1 and P6MD1 registers, and set to input mode by the P5DIR and P6DIR registers. In input mode, pull-up resistor can be selected by the P5PLU and P6PLU register. To use this as timer output and PWM output, select timer output pin by the P5MD1, P5MD2, P6MD1 and P6MD2 registers, and set to output mode by the P5DIR and P6DIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.
TM18O0 TM18O1 TM18O2 TM18O3 TM18O4 TM18O5	31 32 33 34 41 43	34 35 36 37 45 47	Output	P40 P41 P50 P51 P60 P61	PWM output pin	Motor control PWM signal output pin for 16-bit timer 18. PWM signal for 16-bit timer 18 is output to 6 pins simultaneously. To use this pin as PWM output, select timer output pin by the P4MD1, P4MD2, P5MD1, P5MD2, P6MD1 and P6MD2 register and set to output mode by the P4DIR, P5DIR, and P6DIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.
AD0IN00 AD0IN01 AD0IN02 AD0IN03 AD0IN04 AD1IN00 AD1IN01 AD1IN02	1 2 3 5 8 9 10 11	1 2 3 5 8 9 10 11	Input	VGA0(+) VGA0(-) PC2 PC3 PC4 PC5 PC6 PC7	Analog input pin	Analog input pins for 1-type 8-channel, 10-bit A/D converters. These can be used as normal I/O pins when these are not used as analog input. However, AD0IN00 and AD0IN01 are excluded.
IRQ00 IRQ01 IRQ02 IRQ03 IRQ08 IRQ09 IRQ10 IRQ11	12 16 23 24 31 32 33 34	13 17 25 26 34 35 36 37	Input	P00 P01 P02 P03 P40 P41 P50 P51	External interrupt pin	External interrupt input pins. The valid edge can be selected. Set whether both edges are detected or not by IRQEDGESEL register. When it is set not to detect both edges, select rising edge, falling edge, H level, or L level by EXTMD0 and EXTMD1registers. When it is set to detect both edges, select rising edge by the external interrupt condition setting register.
PWM00 PWM01 PWM02	35 37 39	39 41 43	Output	P80 P82 P84	Motor control PWM signal output pin	Motor control 3-phase PWM signal output pin Select PWM signal output pin by the P8MD register and enable PWM output by the PWMOFF0A register. These can be used as normal I/O pins when these pins are not used as PWM signal output pin.
NPWM00 NPWM01 NPWM02	36 38 40	40 42 44	Output	P81 P83 P85	Motor control PWM signal reverse output pin	Motor control 3-phase PWM signal inversion output pin. Select PWM signal output pin by the P8MD register and enable PWM output by the PWMOFF0A register. These can be used as normal I/O pins when these is not used as PWM signal output pin.
VGA0(+)* VGA0(-) *	1 2	1 2	Input	AD0IN00 AD0IN01	Analog input pins	Analog input pins for VGA0. It can be used only as an analog input.
EXTRG0 EXTRG1	24 23	26 25	Output	P03/IRQ03/TM5IO P02/IRQ02/TM4IO	External trigger output pins for debugger	External trigger pins for debugger. Please connect it with the trigger pin of the debugger when you use the trigger function.
TEST	6	6	Input	-	Teset signal input pin	Input pin for test signal input. Connect pull-up resistor of 2 kΩ or more. (Put the resistor near the pins.)
SCLK SDATA	13 14	14 15	Input I/O	-	On-chip debugger I/O pins	Clock input and data I/O pins for on-chip debugger. Connect pull-up resistor of 2 kΩ or more.

* The VGA analog input pin is not in MN103SFN0 series. 1,2 pin of MN103SFN0 series are the dedicated input pin for A/D converter.

1.3.5 Pin Functions (MN103SFN1/N5 series)

Table:1.3.4 Pin Functions (MN103SFN1/N5 series)

Name	Pin No.	I/O	Other Function	Function	Description
VDD50 VDD50	28 64	-	-	Power supply pin	Power pin for 5 V, digital IO Supply 5 V to all of pins and connect 1 μF capacitor or more between all of the VDD50 and VSS pins. (Put the capacitor near the pins.)
VOUT18	23	-	-	Power output pin	Power pin for 1.8 V, digital IO Connect 1 μF capacitor between all of the VOUT18 and VSS pins. (Put the capacitor near the pins.)
VSS VSS	25 62	-	-	Power supply pin	GND for digital
AVDD50	8	-	-	Power supply pin for A/D	Power for A/D. Supply 5 V to AVDD50 pin and connect 1 μF capacitor or more between AVDD50 and AVSS pins. (Put the capacitor near the pins.)
AVSS	6	-	-	Power supply pin for A/D	GND for A/D
NBOOT	29	Input	-	Start area change pin	Use this pin when the start-up area of ROM is changed. Please add the pull-up resistor of 2 kΩ usually.
OSCI OSCO	27 26	Input Output	-	Clock input pin Clock output pin	Oscillator pins for connecting with ceramic oscillator or crystal oscillator. When inputting clock externally, input from OSCI and open OSCO.
NRST	30	Input	-	Reset pins (negative logic)	Pin for power-on reset. Internal pull-up resistors are contained. When this pin is at “L” level, internal state of LSI is initialized. After that, when the input is set to “H” level, reset is cancelled. After oscillation stabilization time by hardware, reset proccessing is executed. Connect 0.1 μF capacitor or more between NRST and VSS pins.
P00 P01 P02 P03	17 18 19 20	I/O	IRQ00/TM0IO IRQ01/TM1IO IRQ02/TM4IO/EXTRG1 IRQ03/TM5IO/EXTRG0	I/O port 0	4-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode (P00 to P03) is selected, and pull-up resistor is disable.
P20 P21 P22 P23 P24 P25	31 32 33 34 35 36	I/O	SBO0 SBT0 SBI0 SBO1 SBT1 SBI1	I/O port 2	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode (P20 to P25) is selected, and pull-up resistor is disable.
P30 P31 P32 P33	37 38 39 40	I/O	SBO2 SBT2 SBI2 SBCS2	I/O port 3	4-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for ech bit can be selected individually by the P3PLU register. At reset, the input mode (P30 to P33) is selected, pull-up resistor is disable.
P40 P41 P42 P43 P46 P47	41 42 43 44 45 46	I/O	IRQ08/TM6IO/TM18O0 IRQ09/TM7IO/TM18O1 IRQ10/TM2IO IRQ11/TM3IO TM10IO/IRQ04 TM11IO/IRQ05	I/O port 4	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up resistor for each bit can be selected individually by the P4PLU register. At reset, the input mode (P40 to P43, P46 to P47) is selected and pull-up resistor is disable.

Name	Pin No.	I/O	Other Function	Function	Description
P50 P51	47 48	I/O	TM16AIO/TM18O2 TM16BIO/TM18O3	I/O port 5	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, the input mode (P50 to P51) is selected and pull-up resistor is disable.
P60 P61 P64 P65	61 63 1 2	I/O	TM18AIO/TM18O4 TM18BIO/TM18O5 TM19AIO TM19BIO	I/O port 6	4-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode (P60 to P61, P64 to P65) is selected and pull-up resistor is disable.
P80 P81 P82 P83 P84 P85	49 50 51 52 53 54	I/O	PWM00 NPWM00 PWM01 NPWM01 PWM02 NPWM02	I/O port 8	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode (P80 to P85) is selected and pull-up resistor is disable.
P90 P91 P92 P93 P94 P95	55 56 57 58 59 60	I/O	PWM10 NPWM10 PWM11 NPWM11 PWM12 NPWM12	I/O port 9	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode (P90 to P95) is selected and pull-up resistor is disable.
PC2 PC3 PC4 PC5 PC6 PC7	5 7 9 10 11 12	I/O	AD0IN02 AD0IN03 AD0IN04 AD1IN00 AD1IN01 AD1IN02	I/O port C	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the PCDIR register. A pull-up resistor for each bit can be selected individually by the PCPLU register. At reset, the input mode (PC2 to PC7) is selected and pull-up resistor is disable.
PD2 PD3	15 16	I/O	AD1IN05 AD1IN06	I/O port D	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the PDDIR register. A pull-up resistor for each bit can be selected individually by the PDPLU register. At reset, the input mode (PD2 to PD3) is selected and pull-up resistor is disable.
SBO0 SBO1 SBO2	31 34 37	Output	P20 P23 P30	Serial interface transmission output pin	Transmission data output pins for serial interface 0 to 2. Select output mode by the P2DIR and P3DIR registers and serial pin function by the P2MD and P3MD registers. These can be used as normal I/O pins when the serial interface is not used.
SBI0 SBI1 SBI2	33 36 39	Input	P22 P25 P32	Serial interface reception data input pin	Reception data input pins for serial interface 0 to 2. Pull-up resistor can be selected by the P2PLU and P3PLU registers. Select input mode by the P2DIR and P3DIR registers. These can be used as normal I/O pins when the serial interface is not used.
SBT0 SBT1 SBT2	32 35 38	I/O	P21 P24 P31	Serial interface clock I/O pin	Clock I/O pins for serial interface 0 to 2. Pull-up resistor can be selected by the P2PLU and P3PLU register. Select I/O mode by the P2DIR and P3DIR register and serial pin function by the P2MD and P3MD register. These can be used as normal I/O pins when the serial interface is not used.

Name	Pin No.	I/O	Other Function	Function	Description
SBCS2	40	I/O	P33	Serial interface chip select I/O pin	Chip select pin for serial interface 2. Pull-up resistor can be selected by the P3PLU register. Select I/O mode by the P3DIR register and serial pin function by the P3MD register. This can be used as normal I/O pins when the serial interface is not used.
TM0IO TM1IO TM2IO TM3IO TM4IO TM5IO TM6IO TM7IO TM10IO TM11IO	17 18 43 44 19 20 41 42 45 46	I/O	P00 P01 P42 P43 P02 P03 P40 P41 P46 P47	Timer I/O pin	Event counter input and timer pulse output pin for 8-bit timer 0 to 7, 10 and 11. To use this pin as event counter input, select input mode by the P0DIR and P4DIR registers. In input mode, pull-up resistor can be selected by the P0PLU and P4PLU registers. To use this pin as timer pulse output, select timer output pin by the P0MD, P4MD1 and P4MD2 registers and set to output mode by the P0DIR and P4DIR registers. These can be used as normal I/O pins when these are not used as timer I/O pins.
TM16AIO TM16BIO TM18AIO TM18BIO TM19AIO TM19BIO	47 48 61 63 1 2	I/O	P50 P51 P60 P61 P64 P65	Timer I/O pin	Event counter input, timer output, and PWM output pin for 16-bit timer 16, 18 and 19. To use this pin as event counter input, select input mode by the P5DIR and P6DIR registers. In input mode, pull-up resistor can be selected by the P5PLU and P6PLU register. To use this as timer output and PWM output, select timer output pin by the P5MD1, P5MD2, P6MD1 and P6MD2 registers, and set to output mode by the P5DIR and P6DIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.
TM18O0 TM18O1 TM18O2 TM18O3 TM18O4 TM18O5	41 42 47 48 61 63	Output	P40 P41 P50 P51 P60 P61	PWM output pin	Motor control PWM signal output pin for 16-bit timer 18. PWM signal for 16-bit timer 18 is output to 6 pins simultaneously. To use this pin as PWM output, select timer output pin by the P4MD1, P4MD2, P5MD1, P5MD2, P6MD1 and P6MD2 register and set to output mode by the P4DIR, P5DIR, and P6DIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.
AD0IN00 AD0IN01 AD0IN02 AD0IN03 AD0IN04 AD1IN00 AD1IN01 AD1IN02 AD1IN03 AD1IN04 AD1IN05 AD1IN06	3 4 5 7 9 10 11 12 13 14 15 16	Input	VGA0(+) VGA0(-) PC2 PC3 PC4 PC5 PC6 PC7 VGA1(+) VGA1(-) PD2 PD3	Analog input pin	Analog input pins for 2-type 12-channel, 10-bit A/D converters. These can be used as normal I/O pins when these are not used as analog input. However, AD0IN00, AD0IN01, AD1IN03 and AD1IN04 are excluded.
IRQ00 IRQ01 IRQ02 IRQ03 IRQ04 IRQ05 IRQ08 IRQ09 IRQ10 IRQ11	17 18 19 20 45 46 41 42 43 44	Input	P00 P01 P02 P03 P04 P05 P40 P41 P42 P43	External interrupt pin	External interrupt input pins. The valid edge can be selected. Set whether both edges are detected or not by IRQEDGESEL register. When it is set not to detect both edges, select rising edge, falling edge, High-level, or Low-level by EXTMD0 and EXTMD1 register. When it is set to detect both edges, select rising edge by the external interrupt condition setting register.

Name	Pin No.	I/O	Other Function	Function	Description
PWM00 PWM01 PWM02 PWM10 PWM11 PWM12	49 51 53 55 57 59	Output	P80 P82 P84 P90 P92 P94	Motor control PWM signal output pin	Motor control 3-phase PWM signal output pin Select PWM signal output pin by the P8MD, P9MD registers and enable PWM output by the PWMOFF0, 1 registers. These can be used as normal I/O pins when these pins are not used as PWM signal output pin.
NPWM00 NPWM01 NPWM02 NPWM10 NPWM11 NPWM12	50 52 54 56 58 60	Output	P81 P83 P85 P91 P93 P95	Motor control PWM signal reverse output pin	Motor control 3-phase PWM signal inversion output pin. Select PWM signal output pin by the P8MD, P9MD registers and enable PWM output by the PWMOFF0, 1 registers. These can be used as normal I/O pins when these is not used as PWM signal output pin.
VGA0(+)* VGA0(-) * VGA1(+)* VGA1(-) *	1 2 13 14	Input	AD0IN00 AD0IN01 AD1IN03 AD1IN04	Analog input pins	Analog input pins for VGA0 and VGA1. It can be used only as an analog input.
EXTRG0 EXTRG1	20 19	Output	P03/IRQ03/TM5IO P02/IRQ02/TM4IO	External trigger output pins for debugger	External trigger pins for debugger. Please connect it with the trigger pin of the debugger when you use the trigger function.
TEST	24	Input	-	Teset signal input pin	Input pin for test signal input. Connect pull-up resistor of 2 kΩ or more. (Put the resistor near the pins.)
SCLK SDATA	21 22	Input I/O	-	On-chip debugger I/O pins	Clock input and data I/O pins for on-chip debugger. Connect pull-up resistor of 2 kΩ or more.

* The VGA analog input pin is not in MN103SFN1 series.
3,4,13,14 pin of MN103SFN1 series are the dedicated input pin for A/D converter.

1.3.6 Pin Functions (MN103SFN2/N6 series)

Table:1.3.5 Pin Functions (MN103SFN2/N6 series)

Name	Pin No.	I/O	Other Function	Function	Description
VDD50 VDD50	32 58	-	-	Power supply pin	Power pin for 5 V, digital IO Supply 5 V to all of pins and connect 1 μF capacitor or more between all of the VDD50 and VSS pins. (Put the capacitor near the pins.)
VOUT18 VOUT18	27 80	-	-	Power output pin	Power pin for 1.8 V, digital IO Connect 1 μF capacitor between all of the VOUT18 and VSS pins. (Put the capacitor near the pins.)
VSS VSS VSS	29 56 78	-	-	Power supply pin	GND for digital
AVDD50	7	-	-	Power supply pin for A/D	Power for A/D. Supply 5 V to AVDD50 pin and connect 1 μF capacitor or more between AVDD50 and AVSS pins. (Put the capacitor near the pins.)
AVSS	4	-	-	Power supply pin for A/D	GND for A/D
NBOOT	33	Input	-	Start area change pin	Use this pin when the start-up area of ROM is changed. Please add the pull-up resistor of 2 kΩ usually.
OSCI OSCO	31 30	Input Output	-	Clock input pin Clock output pin	Oscillator pins for connecting with ceramic oscillator or crystal oscillator. When inputting clock externally, input from OSCI and open OSCO.
NRST	34	Input	-	Reset pins (negative logic)	Pin for power-on reset. Internal pull-up resistors are contained. When this pin is at “L” level, internal state of LSI is initialized. After that, when the input is set to “H” level, reset is cancelled. After oscillation stabilization time by hardware, reset proccessing is executed. Connect 0.1 μF capacitor or more between NRST and VSS pins.
P00 P01 P02 P03 P04 P05 P06 P07	21 22 23 24 35 36 37 38	I/O	IRQ00/TM0IO IRQ01/TM1IO IRQ02/TM4IO/EXTRG1 IRQ03/TM5IO/EXTRG0 IRQ04 IRQ05 IRQ06 IRQ07	I/O port 0	8-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode (P00 to P07) is selected, and pull-up resistor is disable.
P20 P21 P22 P23 P24 P25	39 40 41 42 43 44	I/O	SBO0 SBT0 SBI0 SBO1 SBT1 SBI1	I/O port 2	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode (P20 to P25) is selected, and pull-up resistor is disable.
P30 P31 P32 P33	45 46 47 48	I/O	SBO2 SBT2 SBI2 SBCS2	I/O port 3	4-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for ech bit can be selected individually by the P3PLU register. At reset, the input mode (P30 to P33) is selected, pull-up resistor is disable.
P40 P41 P42 P43 P44 P45 P46 P47	49 50 51 52 53 54 55 57	I/O	IRQ08/TM6IO/TM18O0 IRQ09/TM7IO/TM18O1 IRQ10/TM2IO IRQ11/TM3IO TM8IO TM9IO TM10IO TM11IO	I/O port 4	8-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up resistor for each bit can be selected individually by the P4PLU register. At reset, the input mode (P40 to P47) is selected and pull-up resistor is disable.

Name	Pin No.	I/O	Other Function	Function	Description
P50 P51 P54 P55	59 60 61 62	I/O	TM16AIO/TM18O2 TM16BIO/TM18O3 TM17AIO TM17BIO	I/O port 5	4-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, the input mode (P50 to P51, P54 to P55) is selected and pull-up resistor is disable.
P60 P61 P64 P65	77 79 1 2	I/O	TM18AIO/TM18O4 TM18BIO/TM18O5 TM19AIO TM19BIO	I/O port 6	4-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode (P60 to P61, P64 to P65) is selected and pull-up resistor is disable.
P80 P81 P82 P83 P84 P85	63 64 65 66 67 68	I/O	PWM00 NPWM00 PWM01 NPWM01 PWM02 NPWM02	I/O port 8	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode (P80 to P85) is selected and pull-up resistor is disable.
P90 P91 P92 P93 P94 P95	69 70 71 72 73 74	I/O	PWM10 NPWM10 PWM11 NPWM11 PWM12 NPWM12	I/O port 9	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode (P90 to P95) is selected and pull-up resistor is disable.
PB0 PB1	75 76	I/O	TM20AIO TM20BIO	I/O port B	2-bit CMOS I/O port. Each bit can be set individually as either an input or output by the PBDIR register. A pull-up resistor for each bit can be selected individually by the PBPLU register. At reset, the input mode (PB0 to PB1) is selected and pull-up resistor is disable.
PC2 PC3 PC4 PC5 PC6 PC7	5 7 9 10 11 12	I/O	AD0IN02 AD0IN03 AD0IN04 AD1IN00 AD1IN01 AD1IN02	I/O port C	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the PCDIR register. A pull-up resistor for each bit can be selected individually by the PCPLU register. At reset, the input mode (PC2 to PC7) is selected and pull-up resistor is disable.
PD2 PD3 PD4 PD5 PD6 PD7	15 16 17 18 19 20	I/O	AD1IN05 AD1IN06 AD1IN07 AD1IN08 AD1IN09 AD1IN10	I/O port D	6-bit CMOS I/O port. Each bit can be set individually as either an input or output by the PDDIR register. A pull-up resistor for each bit can be selected individually by the PDPLU register. At reset, the input mode (PD2 to PD7) is selected and pull-up resistor is disable.
SBO0 SBO1 SBO2	39 42 45	Output	P20 P23 P30	Serial interface transmission output pin	Transmission data output pins for serial interface 0 to 2. Select output mode by the P2DIR and P3DIR registers and serial pin function by the P2MD and P3MD registers. These can be used as normal I/O pins when the serial interface is not used.
SBI0 SBI1 SBI2	41 44 47	Input	P22 P25 P32	Serial interface reception data input pin	Reception data input pins for serial interface 0 to 2. Pull-up resistor can be selected by the P2PLU and P3PLU register. Select input mode by the P2DIR and P3DIR register. These can be used as normal I/O pins when the serial interface is not used.

Name	Pin No.	I/O	Other Function	Function	Description
SBT0 SBT1 SBT2	40 43 46	I/O	P21 P24 P31	Serial interface clock I/O pin	Clock I/O pins for serial interface 0 to 2. Pull-up resistor can be selected by the P2PLU and P3PLU register. Select I/O mode by the P2DIR and P3DIR register and serial pin function by the P2MD and P3MD register. These can be used as normal I/O pins when the serial interface is not used.
SBCS2	48	I/O	P33	Serial interface chip select I/O pin	Chip select pin for serial interface 2. Pull-up resistor can be selected by the P3PLU register. Select I/O mode by the P3DIR register and serial pin function by the P3MD register. This can be used as normal I/O pins when the serial interface is not used.
TM0IO TM1IO TM2IO TM3IO TM4IO TM5IO TM6IO TM7IO TM8IO TM9IO TM10IO TM11IO	21 22 51 52 23 24 49 50 53 54 55 57	I/O	P00 P01 P42 P43 P02 P03 P40 P41 P44 P45 P46 P47	Timer I/O pin	Event counter input and timer pulse output pin for 8-bit timer 0 to 11. To use this pin as event counter input, select input mode by the P0DIR and P4DIR registers. In input mode, pull-up resistor can be selected by the P0PLU and P4PLU registers. To use this pin as timer pulse output, select timer output pin by the P0MD, P4MD1 and P4MD2 registers and set to output mode by the P0DIR and P4DIR registers. These can be used as normal I/O pins when these are not used as timer I/O pins.
TM16AIO TM16BIO TM17AIO TM17BIO TM18AIO TM18BIO TM19AIO TM19BIO TM20AIO TM20BIO	59 60 61 62 77 79 1 2 75 76	I/O	P50 P51 P54 P55 P60 P61 P64 P65 PB0 PB1	Timer I/O pin	Event counter input, timer output, and PWM output pin for 16-bit timer 16 to 20. To use this pin as event counter input, select input mode by the P5DIR, P6DIR, and PBDIR registers. In input mode, pull-up resistor can be selected by the P5PLU, P6PLU, and PBPLU register. To use this as timer output and PWM output, select timer output pin by the P5MD1, P5MD2, P6MD1, P6MD2, and PBMD2 registers, and set to output mode by the P5DIR, P6DIR, and PBDIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.
TM18O0 TM18O1 TM18O2 TM18O3 TM18O4 TM18O5	49 50 59 60 77 79	Output	P40 P41 P50 P51 P60 P61	PWM output pin	Motor control PWM signal output pin for 16-bit timer 18. PWM signal for 16-bit timer 18 is output to 6 pins simultaneously. To use this pin as PWM output, select timer output pin by the P4MD1, P4MD2, P5MD1, P5MD2, P6MD1, P6MD2 registers, and set to output mode by the P4DIR, P5DIR, and P6DIR register. These can be used as normal I/O pins when these are not used as timer I/O pins.
AD0IN00 AD0IN01 AD0IN02 AD0IN03 AD0IN04 AD1IN00 AD1IN01 AD1IN02 AD1IN03 AD1IN04 AD1IN05 AD1IN06 AD1IN07 AD1IN08 AD1IN09 AD1IN10	3 4 5 7 9 10 11 12 13 14 15 16 17 18 19 20	Input	VGA0(+) VGA0(-) PC2 PC3 PC4 PC5 PC6 PC7 VGA1(+) VGA1(-) PD2 PD3 PD4 PD5 PD6 PD7	Analog input pin	Analog input pins for 2-type 16-channel, 10-bit A/D converters. These can be used as normal I/O pins when these are not used as analog input. However, AD0IN00, AD0IN01, AD1IN03 and AD1IN04 are excluded.

Name	Pin No.	I/O	Other Function	Function	Description
IRQ00 IRQ01 IRQ02 IRQ03 IRQ04 IRQ05 IRQ06 IRQ07 IRQ08 IRQ09 IRQ10 IRQ11	21 22 23 24 35 36 37 38 49 50 51 52	Input	P00 P01 P02 P03 P04 P05 P06 P07 P40 P41 P42 P43	External interrupt pin	External interrupt input pins. The valid edge can be selected. Set whether both edges are detected or not by IRQEDGESEL register. When it is set not to detect both edges, select rising edge, falling edge, H level, or L level by EXTMD0 and EXTMD1 register. When it is set to detect both edges, select rising edge by the external interrupt condition setting register.
PWM00 PWM01 PWM02 PWM10 PWM11 PWM12	63 65 67 69 71 73	Output	P80 P82 P84 P90 P92 P94	Motor control PWM signal output pin	Motor control 3-phase PWM signal output pin Select PWM signal output pin by the P8MD, P9MD registers and enable PWM output by the PWMOFF0, 1 registers. These can be used as normal I/O pins when these pins are not used as PWM signal output pin.
NPWM00 NPWM01 NPWM02 NPWM10 NPWM11 NPWM12	64 66 68 70 72 74	Output	P81 P83 P85 P91 P93 P95	Motor control PWM signal reverse output pin	Motor control 3-phase PWM signal inversion output pin. Select PWM signal output pin by the P8MD, P9MD registers and enable PWM output by the PWMOFF0, 1 registers. These can be used as normal I/O pins when these is not used as PWM signal output pin.
VGA0(+)* VGA0(-) * VGA1(+)* VGA1(-) *	3 4 13 14	Input	AD0IN00 AD0IN01 AD1IN03 AD1IN04	Analog input pins	Analog input pins for VGA0 and VGA1. It can be used only as an analog input.
EXTRG0 EXTRG1	24 23	Output	P03/IRQ03/TM5IO P02/IRQ02/TM4IO	External trigger output pins for debugger	External trigger pins for debugger. Please connect it with the trigger pin of the debugger when you use the trigger function.
TEST	28	Input	-	Teset signal input pin	Input pin for test signal input. Connect pull-up resistor of 2 kΩ or more. (Put the resistor near the pins.)
SCLK SDATA	25 26	Input I/O	-	On-chip debugger I/O pins	Clock input and data I/O pins for on-chip debugger. Connect pull-up resistor of 2 kΩ or more.

*The VGA analog input pin is not in MN103SFN2 series.
3,4,13,14 pin of MN103SFN2 series are the dedicated input pin for A/D converter.

1.4 Block Diagram

1.4.1 Block Diagram (MN103SFJ7A)

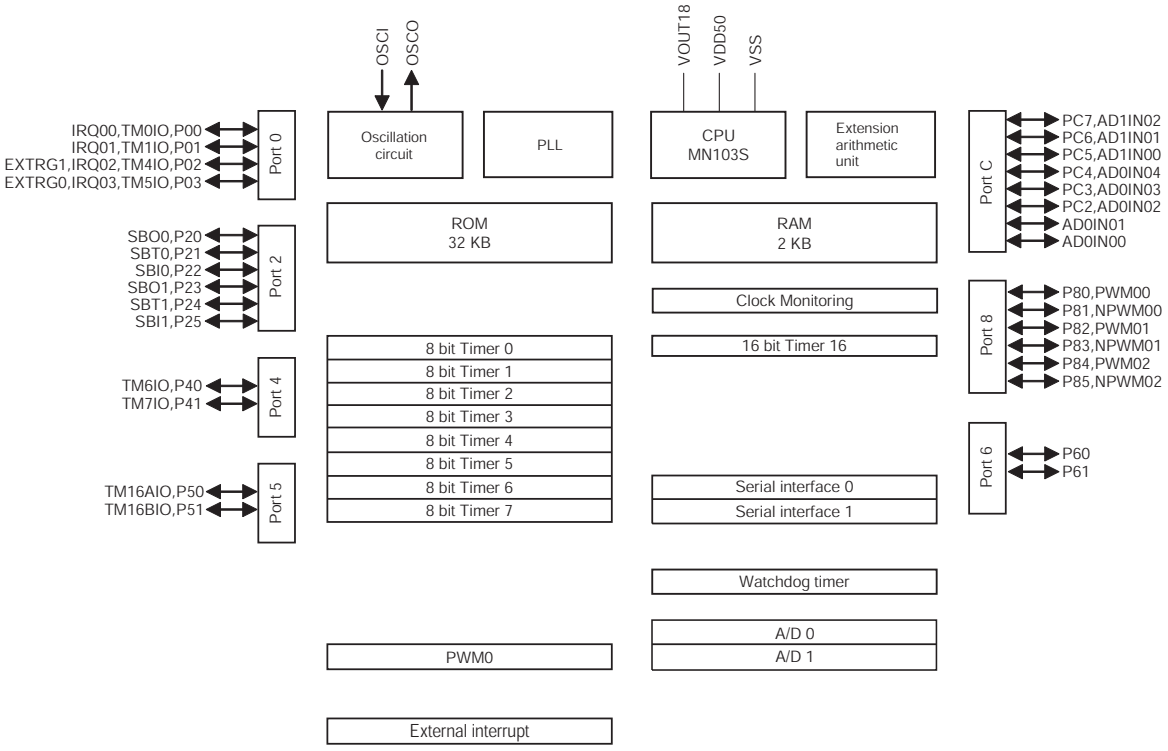


Figure:1.4.1 Block Diagram (MN103SFJ7A series)

1.4.2 Block Diagram (MN103SFN0/N4 series)

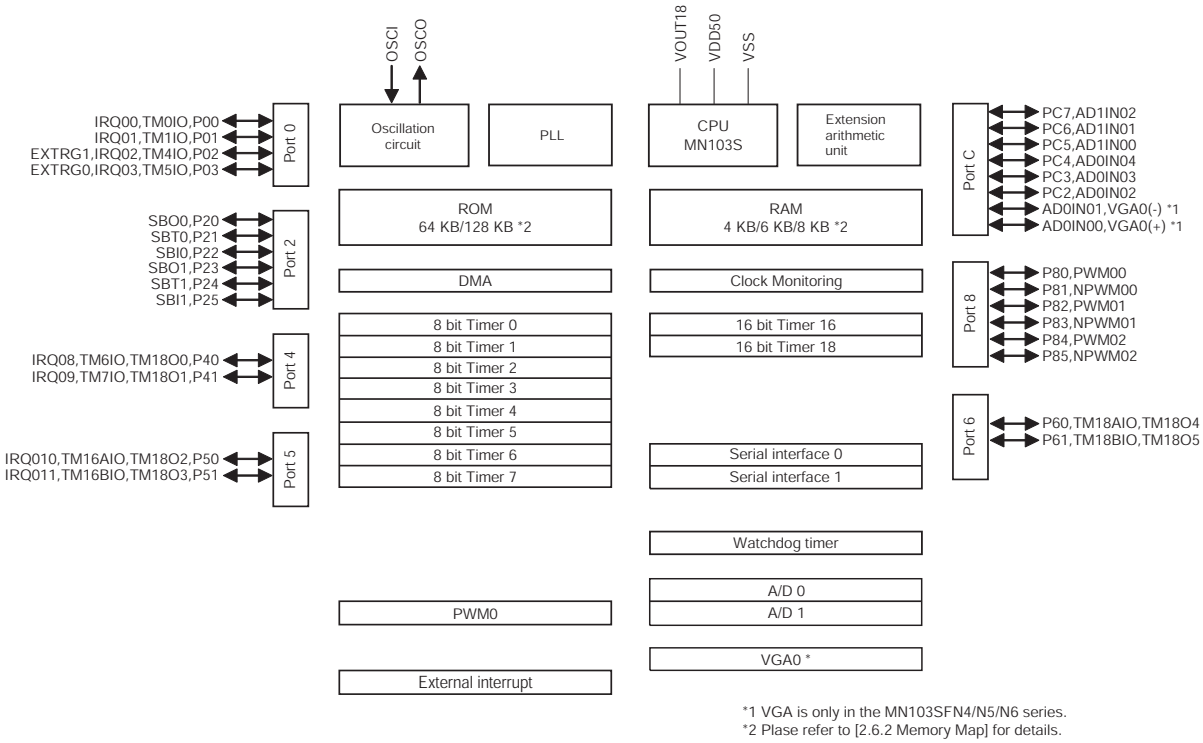


Figure:1.4.2 Block Diagram (MN103SFN0/N4 series)

1.4.3 Block Diagram (MN103SFN1/N5 series)

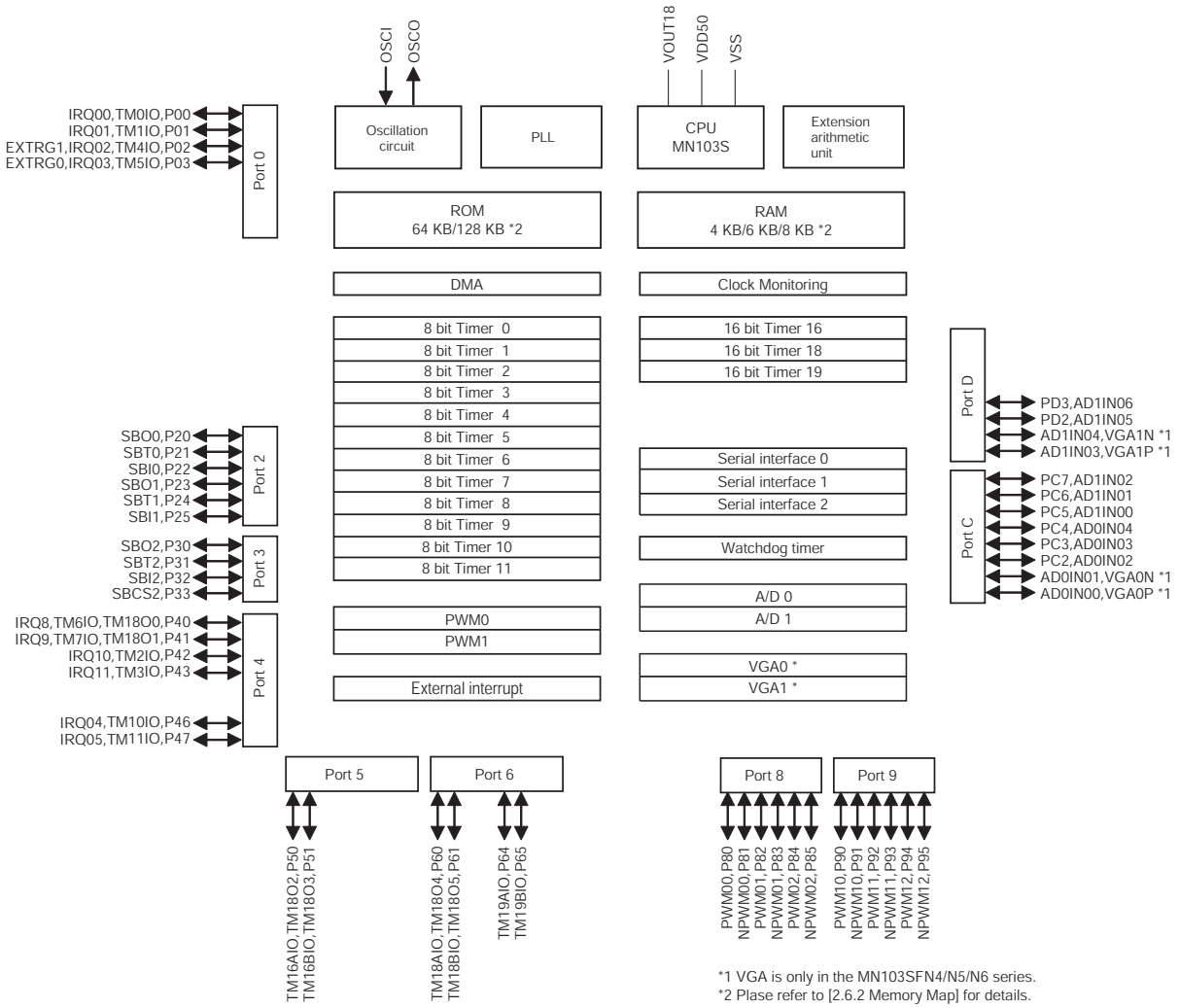


Figure:1.4.3 Block Diagram (MN103SFN1/N5 series)

1.4.4 Block Diagram (MN103SFN2/N6 series)

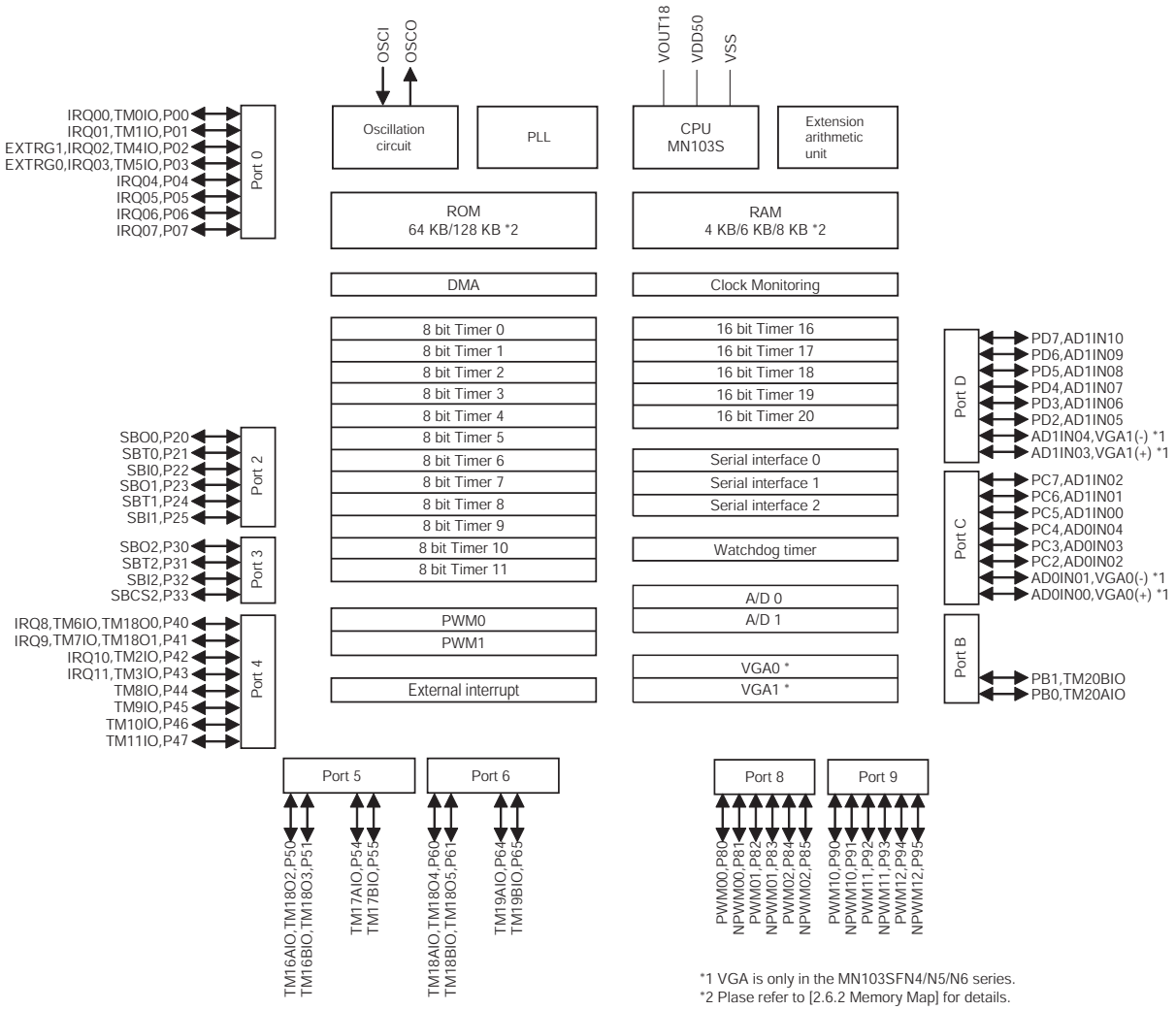


Figure:1.4.4 Block Diagram (MN103SFN2/N6 series)

1.5 Electrical Characteristics

This LSI manual describes the standard specification.

Electrical characteristics given in this section are preliminary and subject to change without notice. When using LSI, contact our sales office for product specifications.

Model	CMOS LSI
Application	General-purpose
Function	CMOS 32-bit microcontroller

1.5.1 Absolute Maximum Ratings

V_{SS} = 0.0 V

Parameter		Symbol		Rating	Unit
A1	External supply voltage 1	V_{DD50}		-0.3 to +7.0	V
A2	External supply voltage 2	AV_{DD50}		-0.3 to +7.0	V
A3	Internal supply voltage	V_{OUT18}		-0.3 to +2.5	V
A4	Input pin voltage	V_I		-0.3 to V_{DD50} +0.3 (upper limit: 7.0)	V
A5	Analog Input pin voltage for A/D *1	V_{AIN}		-0.3 to AV_{DD50} +0.3 (upper limit: 7.0)	V
A6	Input pin voltage for VGA *2	V_{VGA}		-1.5 to AV_{DD50} +0.3 (upper limit: 7.0)	V
A7	I/O pin voltage (Other than those above)	V_{IO}		-0.3 to V_{DD50} +0.3 (upper limit: 7.0)	V
A8	Peak output current	I_{OPEAK}		±15	mA
A9	Average output current	I_{OAVG1}		±7.5	mA
A10	Operating ambient temperature	T_{OPR}		-40 to 85	°C
A11	Storage temperature	T_{STG}		-40 to 125	°C
A12	Power dissipation	P_D	QFP 44 pin	370	mW
			TQFP 48 pin	320	
			TQFP 64 pin	480	
			LQFP 64 pin	480	
			TQFP 80 pin	480	

Note: Each of the absolute maximum ratings refers to a limit or values that will not damage the LSI even if the LSI is subject to that rating. The average output current rating is applicable to any given 100-ms period. Insert at least one 1 µF or higher bypass capacitor between each power supply pins (V_{DD50} pins) and ground. Insert at least one 1 µF or higher bypass capacitor between AVDD50 pin and AVSS pin. Additionally, insert at least one 1 µF bypass capacitor between each internal power supply pins (V_{OUT18} pins) and ground.

*1 MN103SFJ7A and MN103SFN0/N1/N2 series only
*2 MN103SFN4/N5/N6 series only

1.5.2 Operating Conditions

V_{SS} = 0.0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
B1	External supply voltage	V_{DD50}	-	V_{RST}	5.0	5.5	V
B2	External supply voltage	AV_{DD50}	-	V_{RST}	5.0	5.5	V

Note) Refer to “Power Detection Circuit Characteristics” on page I-44 for the supply voltage detection level V_{RST}.

Oscillation input

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
V_I = V_{DD50} or V_{SS}
V_{SS} = 0.0 V Ta = -40 °C to 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
B3	Input frequency	F_{OSC}	-	5.0	-	15.0	MHz

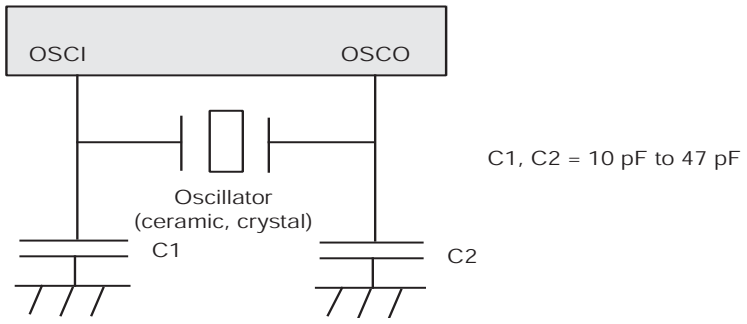


Figure:1.5.1 Oscillation

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
Ta = -40 °C to 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSCI (OSCO left open)							
B4	Clock frequency	F_{cp}	-	5.0	-	15.0	MHz
B5	High-level pulse width	t_{wh1}	Figure:1.5.2	25.0	-	-	ns
B6	Low-level pulse width	t_{wl1}		25.0	-	-	ns
B7	Rise time	t_{wr1}		-	-	5.0	ns
B8	Fall time	t_{wf1}		-	-	5.0	ns

Note: Be sure that the clock duty ratio is 45 % to 55 %.

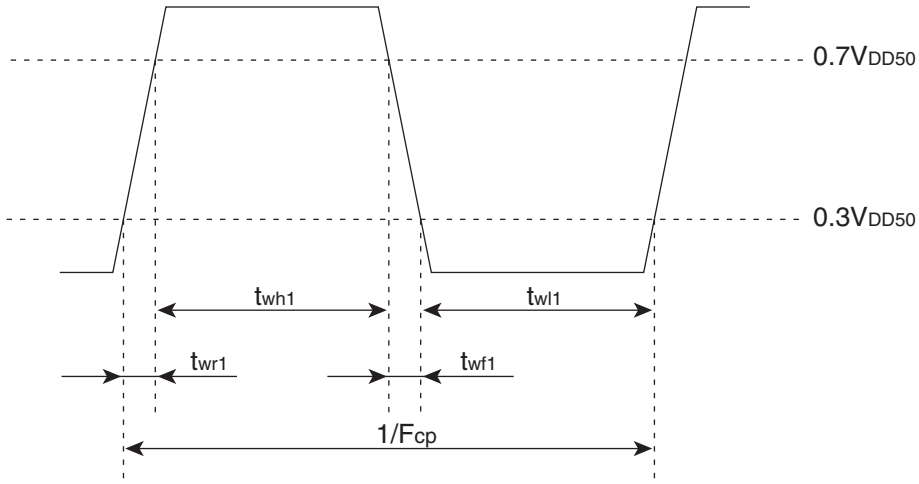


Figure:1.5.2 OSCI Timing Chart

1.5.3 DC Characteristics

DC Characteristics

$V_I = V_{DD50}$ or V_{SS}
Output open
V_{SS} = 0.0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C1	Power supply current during operation (V_{DD50} pin)	I_{DD1}	V_{DD50} = 5.0 V Internal regulator used. PLL used. External Oscilation: 10 MHz MCLK = 60 MHz IOCLK = 30 MHz	-	25	40	mA
C2	Power supply current during SLEEP mode (V_{DD50} pin)	I_{DD2}	V_{DD50} = 5.0 V Internal regulator used. PLL used. External Oscilation: 10 MHz IOCLK = 30 MHz	-	10	20	mA
C3	Power supply current during HALT mode (V_{DD50} pin)	I_{DD3}	V_{DD50} = 5.0 V Internal regulator used. PLL used. External Oscilation: 10 MHz IOCLK = 30 MHz	-	4	6	mA
C4	Power supply current during STOP mode (V_{DD50} pin)	I_{DD4}	V_{DD50} = 5.0 V External Oscilation is stopped Ta = 25 °C	-	150	-	µA
C5	Power supply current during STOP mode (V_{DD50} pin)	I_{DD5}	V_{DD50} = 5.0 V External Oscilation is stopped Ta = 85 °C	-	-	400	µA

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
Ta = - 40 °C to + 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin <output: push/pull / input: CMOS level> P00 to P07, P20 to P25, P30 to P33, P40 to P47, P50, P51, P54, P55, P60, P61, P64, P80 to P85, P90 to P95, PB0, PB1, PC2 to PC7, PD2 to PD7 *1							
C6	Input voltage High level	V_{IH1}	-	V_{DD50} x 0.7	-	V_{DD50}	V
C7	Input voltage Low level	V_{IL1}	-	0.0	-	V_{DD50} x 0.3	V
C8	Input current Low level	I_{IH1}	V_I = 0 V Pull-up resistor is used	-334	-167	-84	µA
C9	Output voltage High level	V_{OH1}	I_O = -2.5 mA	V_{DD50} - 0.5	-	-	V
C10	Output voltage Low level	V_{OL1}	I_O = 2.5 mA	-	-	0.5	V
C11	Output leak current	I_{OZ1}	V_O = Hi-Z status	-5	-	5	µA

*1 The I/O pin that doesn't exist in the MN103SFJ7A and MN103SFN0/N1/N4/N5 series has been described either.

Value of Internal pull-up resistor
The standard value of internal pull-up resistor is 30 kΩ when V_{DD50} = 5.0 V and V_I = 0.0 V.
However, this value may change greatly depending on temperature. In the range from -40 °C to 85 °C.the value may be 15 kΩ to 60 kΩ.

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
Ta = -40 °C to 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pins < input: CMOS level> VGA0(+), VGA0(-), VGA1(+), VGA1(-) (input pin for VGA) *2							
C12	Input voltage range 1	V_{IV1}	When VGA is used, Gain = 2.05	-1.00	-	1.00	V
C13	Input voltage range 2	V_{IV2}	When VGA is used, Gain = 3.05	-0.66	-	0.66	V
C14	Input voltage range 3	V_{IV3}	When VGA is used, Gain = 4.00	-0.50	-	0.50	V
C15	Input voltage range 4	V_{IV4}	When VGA is used, Gain = 4.98	-0.40	-	0.40	V
C16	Input voltage range 5	V_{IV5}	When VGA is used, Gain = 5.96	-0.34	-	0.34	V
C17	Input voltage range 6	V_{IV6}	When VGA is used, Gain = 7.90	-0.26	-	0.26	V
C18	Input voltage range 7	V_{IV7}	When VGA is used, Gain = 9.83	-0.20	-	0.20	V
C19	Input voltage range 8	V_{IV8}	When VGA is used, Gain is 19.40	-0.10	-	0.10	V
C20	Input voltage range 9	V_{IV9}	When VGA unused	AV_{SS}	-	AV_{DD50}	V

*2 The VGA pins are only in the MN103SFN4/N5/N6 series.

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
Ta = -40 °C to 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pins < input: CMOS level> NRST							
C21	Input voltage High level	V_{IH2}	-	V_{DD50} x 0.7	-	V_{DD50}	V
C22	Input voltage Low level	V_{IL2}	-	0.0	-	V_{DD50} x 0.3	V
C23	Input current Low level	I_{IL2}	V_I=0 V Pull-up resistor is used	-334	-167	-84	μA

Value of internal pull-up resisor of NRST pin
The standard value of internal pull-up resistor is 30 kΩ when V_{DD50} = 5.0 V and V_I = 0.0 V.
However, this value may change greatly depending on temperature. In the range from -40 °C to +85 °C, the value may be 15 kΩ to 60 kΩ.

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
Ta = -40 °C to 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pins < input: CMOS level>
SCLK, SDATA, TEST							
C24	Input voltage High level	V_{IH3}	-	V_{DD50} x 0.7	-	V_{DD50}	V
C25	Input voltage Low level	V_{IL3}	-	0.0	-	V_{DD50} x 0.3	V

How to use test pin and debugging pins
These pins need to connect the pull-up resistor.
SCLK ... Connect to pull-up resistor of 2 kΩ or more.
SDATA ... Connect to pull-up resistor of 2 kΩ or more.
TEST ... Connect to pull-up resistor of 2 kΩ or more.

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
Ta = -40 °C to 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
OSCI pin							
C26	Input voltage High level	V_{IH3}	When external clock is input	V_{DD05} x 0.7	-	V_{DD50}	V
C27	Input voltage Low level	V_{IL3}	When external clock is input	0.0	-	V_{DD50} x 0.3	V
C28	Internal feedback resistor	R_{FB}	$V_I = V_{DD50}$ or V_{SS}	-	1.2	-	MΩ
Regulator output pin V_{OUT18} *							
C29	Output voltage range	V_{OUT18}	-	1.65	1.8	1.95	V

* Use the regulator output as power supply only for the microcontroller.

1.5.4 A/D Converter Characteristics

A/D Characteristics

AV_{DD50} = 5.0 V
AV_{SS} = 0.0 V
Ta = 25 °C

A/D0, A/D1

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	Resolution	-	-	-	-	10	Bits
D2	Non-linearity error	-	Sampling time ≥ 133 ns A/D conversion clock ≤ 30 MHz	-2	-	+2	LSB
D3	Differential linearity error	-		-3	-	+3	LSB
D4	Zero transition voltage	-		-20	-	20	mV
D5	Full-scale transition voltage	-		4980	-	5020	mV
D6	A/D conversion time	-	-	0.5	-	-	µs
D7	Analog input voltage	V_{IA}	-	AV_{SS}	-	AV_{DD50}	V
D8	Analog input leakage current	I_{LA}	Unselected channel V_{IA} = 0 V to AV_{DD50}	-5	-	+5	µA
D9	Power supply current during operation (AV_{DD50} pin)	I_{AD}	A/D 1unit operation (A/D conversion clock ≤ 30 MHz)	-	1	-	mA

1.5.5 VGA Characteristics

VGA Characteristics
VGA are only in the MN103SFN4/N5/N6 series.
VGA0, VGA1

AV_{DD50} = 5.0 V
AV_{SS} = 0.0 V
Ta = 25 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
E1	Gain error	V_{gaerr1}	Gain = 2.045	-	-	1.5	%
		V_{gaerr2}	Gain = 3.030	-	-	1.3	
		V_{gaerr3}	Gain = 4.010	-	-	1.3	
		V_{gaerr4}	Gain = 4.990	-	-	1.2	
		V_{gaerr5}	Gain = 5.970	-	-	1.3	
		V_{gaerr6}	Gain = 7.920	-	-	1.3	
		V_{gaerr7}	Gain = 9.860	-	-	1.3	
		V_{gaerr8}	Gain = 19.500	-	-	1.5	
E2	Input offset voltage	V_{off1}	Gain = 2.045	-48.2	-	48.2	mV
		V_{off2}	Gain = 3.030	-32.6	-	32.6	
		V_{off3}	Gain = 4.010	-24.6	-	24.6	
		V_{off4}	Gain = 4.990	-20.8	-	20.8	
		V_{off5}	Gain = 5.970	-17.4	-	17.4	
		V_{off6}	Gain = 7.920	-13.7	-	13.7	
		V_{off7}	Gain = 9.860	-11.0	-	11.0	
		V_{off8}	Gain = 19.500	-6.1	-	6.1	
E3	Through rate	V_{gathr}	-	4.0	6.0	-	V/µs
E4	Power supply current during operation (AV_{DD50} pin)	I_{VGA}	VGA 1unit operation	-	1.5	-	mA

1.5.6 AC Characteristics

Reset signal input timing

V_{SS} = 0.0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F1	Reset signal pulse width (NRST)	t_{RSTW}	-	1	-	-	ms
F2	Reset release timing (NRST)	t_{RSTS}	-	1	-	-	ms

Insert capacitor of over 0.1 μF between NRST pin and ground.

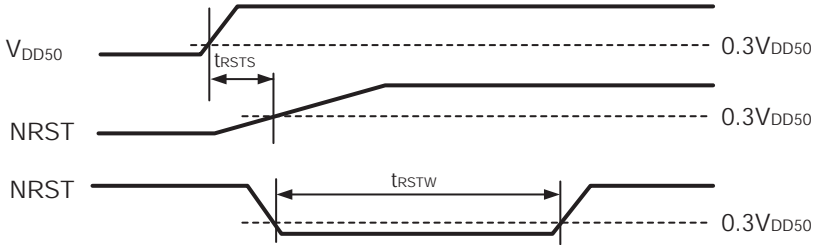


Figure:1.5.3 Reset Signal Input Timing

Interrupt signal input timing
(External interrupt pins : From IRQ00 to IRQ11)

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F3	Interrupt signal pulse width (In not using noise filter)	t_{IRQW1}	Tmclk = 1/MCLK Tsmp = n/IOCLK (n = 4, 8, 16, 32)	Tmclk x 3 *1	-	-	ns
F4	Interrupt signal pulse width (In using noise filter)	t_{IRQW2}		Tsmp x 3 *2	-	-	ns

*1 When no noise filter is used, the minimum pulse width is determined by system clock (MCLK). Maintain the interrupt signal for a minimum of 3 cycles of MCLK.
*2 When noise filter is used, the minimum pulse width is determined by sampling clock. Maintain the interrupt signal for a minimum of 3 cycles of sampling clock.
Refer to [Chapter 11 11.3 Interrupt Controller Operation] for further details.

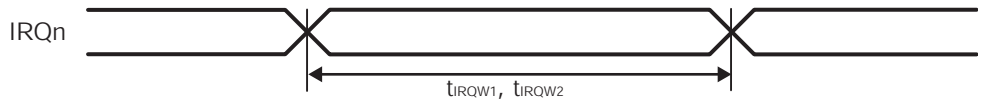


Figure:1.5.4 Interrupt Signal Input Timing

V_{SS} = 0.0 V

Power supply detection circuit characteristics

Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F5	Power supply detection level	V_{RST}	-	3.6	-	4.3	V
F6	Rate of change for power supply voltage	ΔV_{DD50}	-	0.2	-	-	ms/V

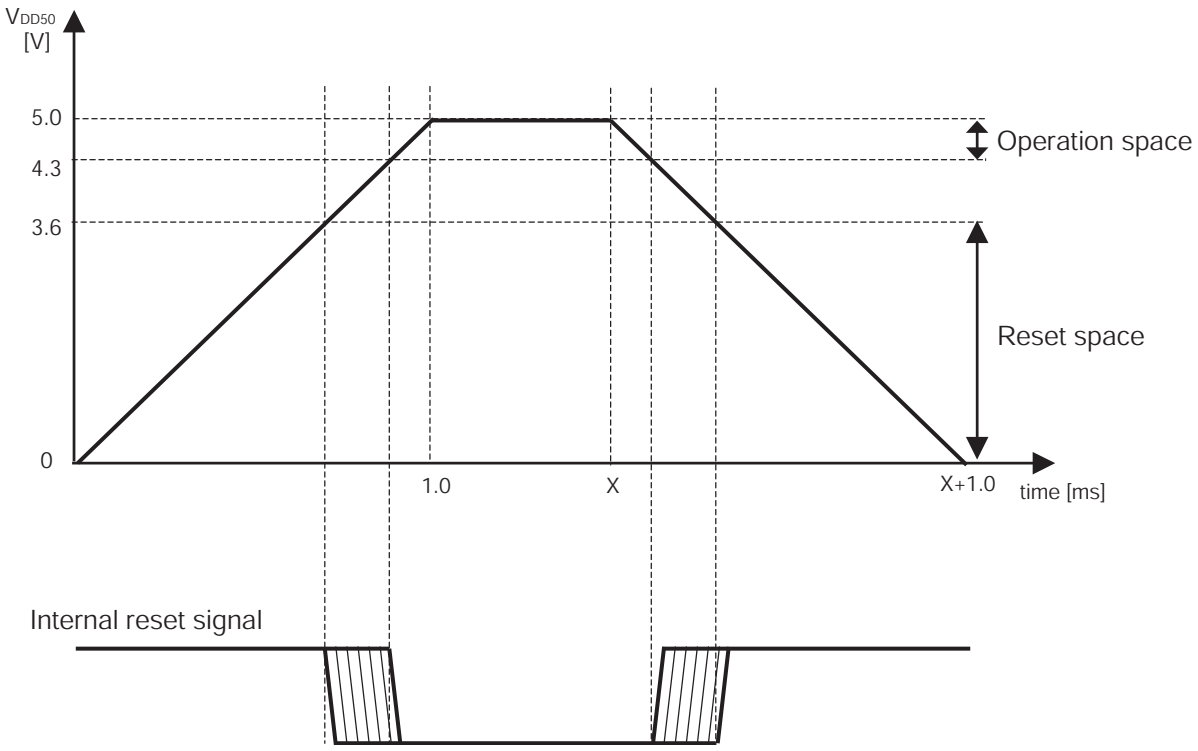


Figure:1.5.5 Power Supply Detection Level

1.5.7 Internal Low-speed Oscillation Circuit Characteristics

V_{DD50} = V_{RST} to 5.5 V
V_{SS} = 0.0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
G1	Internal low-speed oscillation circuit frequency	f_{rc}	V_{DD50} = V_{RST} to 5.5 V	-	280	-	kHz
G2	Temperature dependence of oscillation frequency	f_{rc1}	Ta = -40 °C to +85 °C	-20	-	20	%

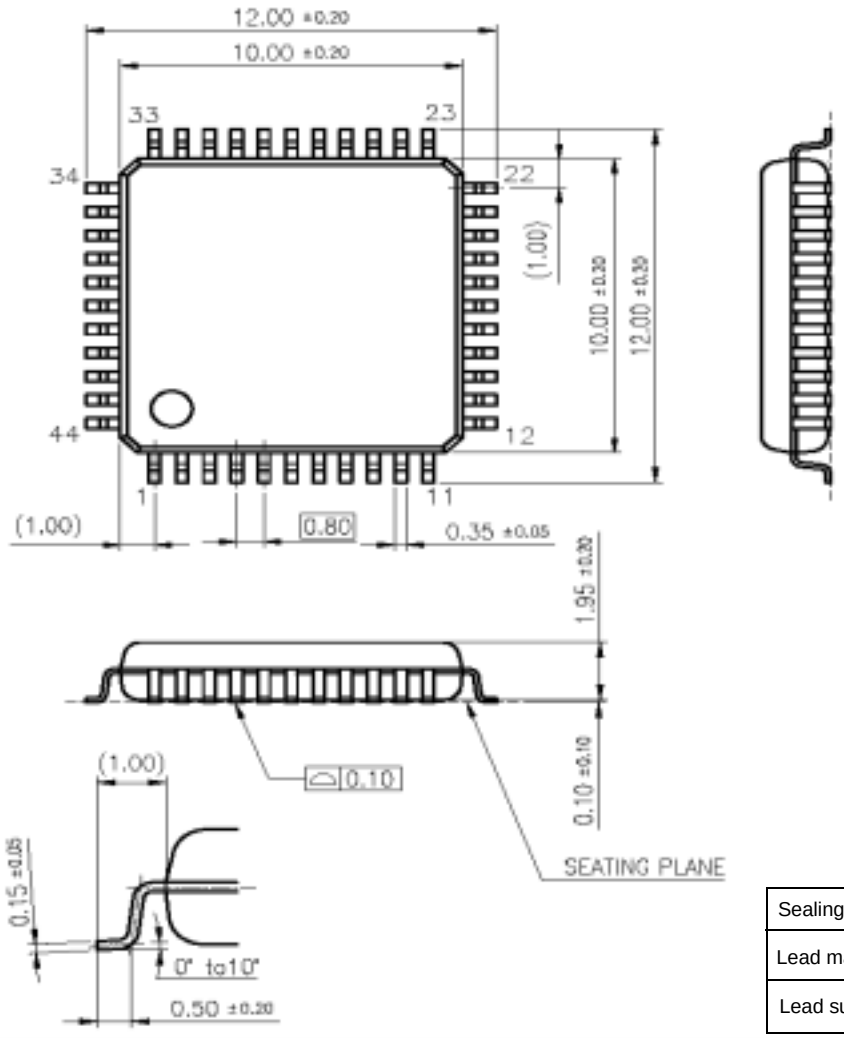
1.5.8 Flash EEPROM E/W Characteristics

V_{DD50} = 5.0 V
V_{SS} = 0.0 V
Ta= -40 °C to +85 °C

Parameter			Symbol	Conditions	Rating			Unit
					MIN	TYP	MAX	
H1	Power supply at E/W		V_{DD50EW}	-	V_{RST}	5.0	5.5	V
H2	Ambient temperature at E/W		T_{OPREW}	-	-40	-	85	°C
H3	Permissible rewriting times	Large sector (sector size:32 KB)	E_{MAX1}	-	-	-	1000	Times
H4		Small sector (sector size:8 KB)	E_{MAX2}	-	-	-	100000	Times
H5	Data retention period		T_{HOLD}	Ta = -40 °C to +125 °C	10	-	-	Years

1.6 Package Dimension

Units: mm

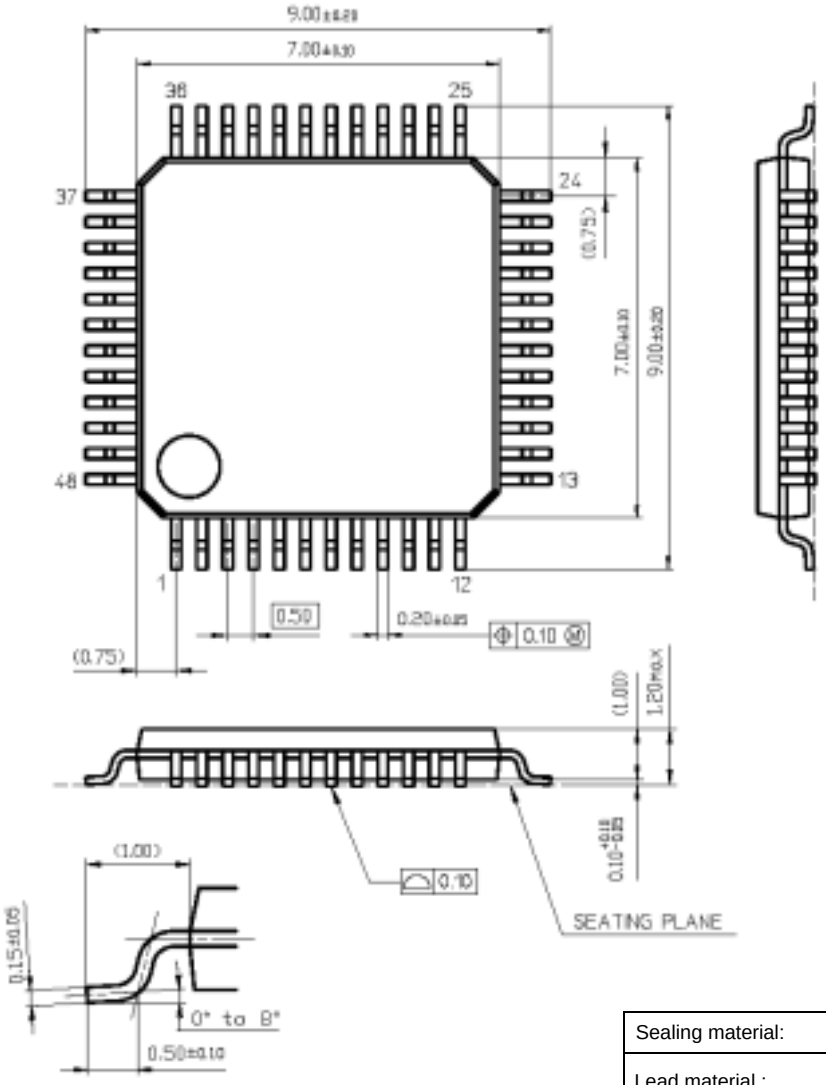


Sealing material:	EPOXY resin
Lead material :	Cu alloy
Lead surface processing :	Pd plating

Figure:1.6.1 Package Dimension of MN103SFN0/N4 series (QFP 44 pin)

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

Units: mm

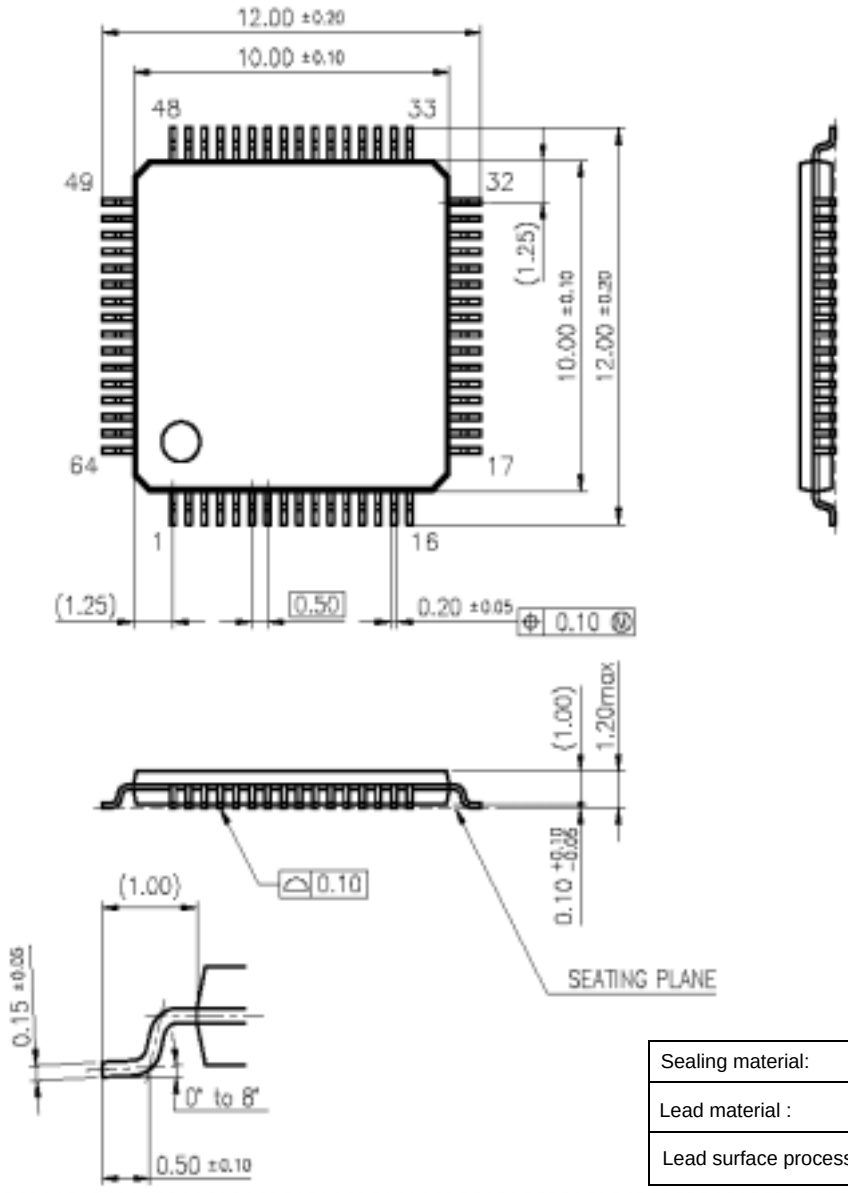


Sealing material:	EPOXY resin
Lead material :	Cu alloy
Lead surface processing :	Pd plating

Figure:1.6.2 Package Dimension of MN103SFJ7A and MN103SFN0/N4 series (TQFP 48 pin)

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

Units: mm



Sealing material:	EPOXY resin
Lead material :	Cu alloy
Lead surface processing :	Pd plating

Figure:1.6.3 Package Dimension of MN103SFN1/N5 series (TQFP 64 pin)

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

Units: mm

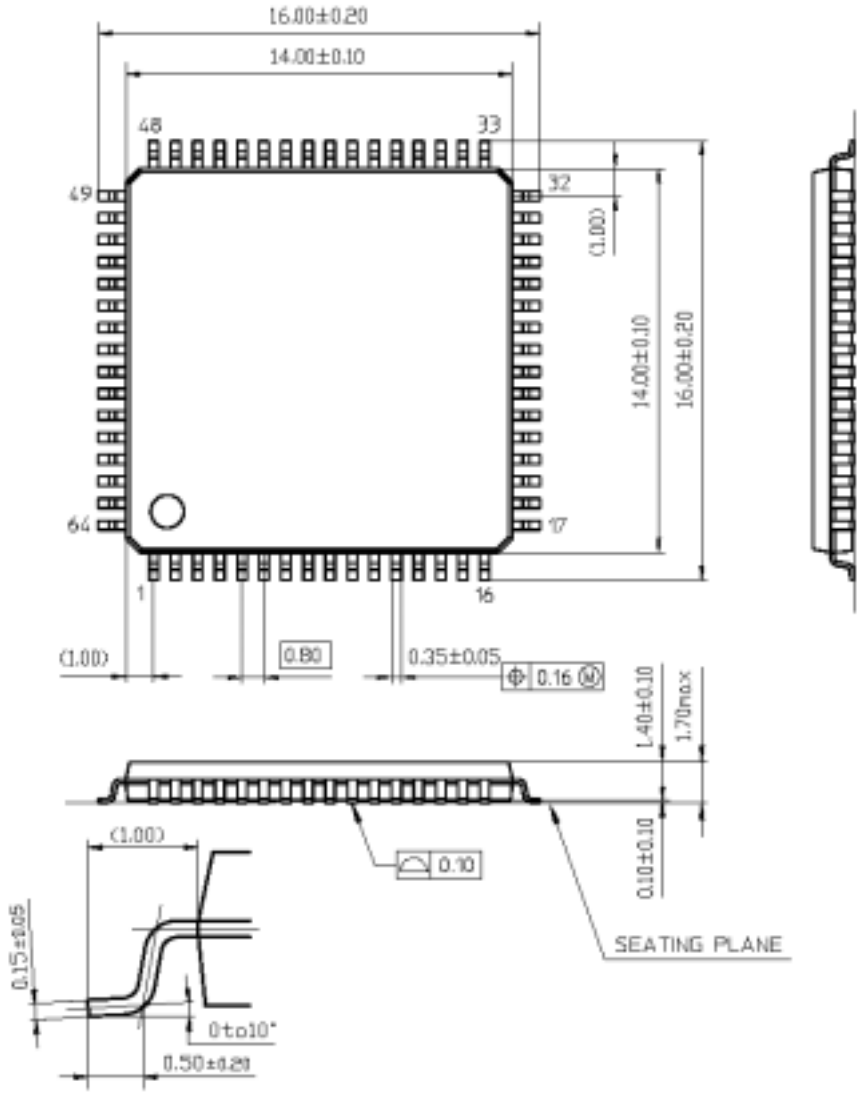
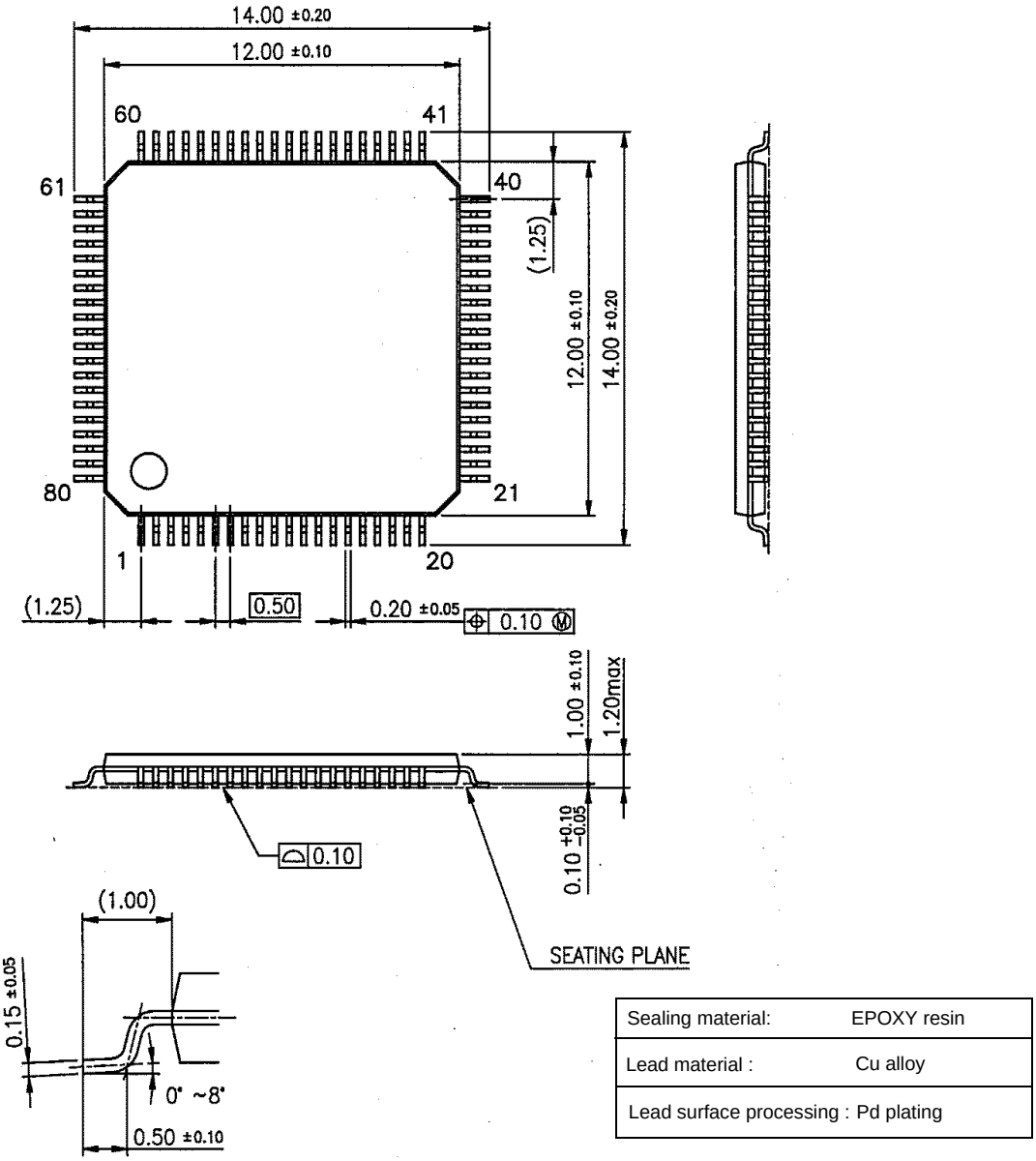


Figure:1.6.4 Package Dimension of MN103SFN1/N5 series (LQFP 64 pin)

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

Units: mm



Sealing material:	EPOXY resin
Lead material :	Cu alloy
Lead surface processing :	Pd plating

Figure:1.6.5 Package Dimension of MN103SFN2/N6 series

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

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