

Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

※ Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan

1.1 Overview

1.1.1 Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for in-vehicle body control, in-vehicle AV, camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set.

MN101EFC3D has an internal 76 KB of ROM and 6 KB of RAM. MN101EFC3Y has an internal 76 KB of ROM and 10 KB of RAM. MN101EFC3G has an internal 128 KB of ROM and 6 KB of RAM. MN101EFC3Z has an internal 128 KB of ROM and 10 KB of RAM. MN101EFD3D has an internal 76 KB of ROM and 10 KB of RAM. MN101EFD3G has an internal 128 KB of ROM and 10 KB of RAM. Peripheral functions include 5 external interrupts, 34 internal interrupts including NMI, 12 timer counters, 4 types of serial interfaces, CAN controller (on MN101EFD3D/G) based on CAN 2.0B, A/D converter, LCD driver, 2 types of watchdog timer, and data automatic function. The system configuration is suitable for in-vehicle body control microcontroller such as in-vehicle body control, heater control, relay BOX, or various motor controls.

With 5 oscillation systems (high-speed (internal frequency: 20 MHz), high-speed (crystal/ceramic frequency: max. 10 MHz) / low-speed (internal frequency: 30 kHz), low-speed (crystal/ceramic frequency: 32.768 kHz) and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode), or to low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has the normal mode which is based on the clock dividing f_{pll} , (f_{pll} is generated by original oscillation and PLL), by 2 ($f_{pll}/2$), and the double speed mode which is based on the clock not dividing f_{pll} .

A machine cycle (minimum instruction execution time) in the normal mode is 200 ns when the original oscillation f_{osc} is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when f_{osc} is 10 MHz. A machine cycle in the PLL mode and in the double speed mode when the internal oscillation f_{rc} is 20 MHz (PLL is not used) is 50 ns (maximum).

1.1.2 Product Summary

This manual describes the following model.

Table:1.1.1 Product Summary

Table remarks O: With function -: Without function

Model	ROM Size	RAM Size	CAN Controller	Classification	Package
MN101EFC3D	76 KB	6 KB	-	Flash EEPROM version	TQFP064-P-1010D LQFP064-P-1414
MN101EFC3Y	76 KB	10 KB	-	Flash EEPROM version	
MN101EFC3G	128 KB	6 KB	-	Flash EEPROM version	
MN101EFC3Z	128 KB	10 KB	-	Flash EEPROM version	
MN101EFD3D	76 KB	10 KB	O	Flash EEPROM version	
MN101EFD3G	128 KB	10 KB	O	Flash EEPROM version	



Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.
When using ICE version, connect pull-up resistor to DMOD on the target board.

1.2 Hardware Functions

■ Feature

- ROM capacity: 76 KB to 128 KB
- RAM capacity: 6 KB to 10 KB
- Package: TQFP064-P-1010D (10 mm × 10 mm / 0.5 mm pitch/ Halogen free *)
LQFP064-P-1414 (14 mm × 14 mm / 0.8 mm pitch)
 - * Panasonic's "halogen free" semiconductor products refer to the products made of molding resin and interposer which conform to the following standards.
 - Bromine: 900 ppm (Maximum Concentration Value)
 - Chlorine: 900 ppm (Maximum Concentration Value)
 - Bromine + Chlorine: 1500 ppm (Maximum Concentration Value)
 - The above-mentioned standards are based on the numerical value described in IEC61249-2-21. Antimony and its compounds are not added intentionally.
- Machine Cycle:
 - High-speed mode
 - 0.05 μ s/20 MHz (2.7 V to 5.5 V)
 - 0.125 μ s/8 MHz (1.8 V to 5.5 V)
 - Low-speed mode
 - 62.5 μ s/32 kHz (1.8 V to 5.5 V)
- Clock Gear Circuit:
 - Internal system clock speed is changeable by selecting division ratio of oscillation clock.
(Divided by 1, 2, 4, 16, 32, 64, 128)
- Oscillation Circuit: 4 types
 - High-speed (Internal oscillation: frc), High-speed (crystal/ceramic: fosc),
 - Low-speed (Internal oscillation: frcs), Low-speed (crystal/ceramic: fx)
 - High-speed internal oscillation 20 MHz / 16 MHz (selectable)
 - Low-speed internal oscillation 30 kHz
- Clock Multiplication Circuit:
 - PLL circuit output clock (fp11) fosc multiplied by 2, 3, 4, 5, 6, 8, 10,
1/2xfrc multiplied by 4, 5 enabled
 - * When clock multiplication circuit is not used, fp11 = fosc or fp11 = frc
 - * Selectable from high-speed clock for peripheral functions (fp11-div) fp11, fp11 divided by 2, 4, 8, 16

- Operation Mode

NORMAL mode (high-speed mode)

PLL mode

SLOW mode (low-speed mode)

HALT mode

STOP mode

and operation clock switching

- Operating Voltage: 1.8 V to 5.5 V

- Operation ambient temperature: -40 °C to +85 °C (Product guaranteed 105 °C is available)

- interrupt: 35 sets

<Overrun interrupt>

- Non-maskable interrupt (NMI)

<Timer interrupt>

- Timer 0 interrupt

- Timer 1 interrupt

- Timer 2 interrupt

- Timer 3 interrupt

- Timer 4 interrupt

- Timer 6 interrupt

- Time-base interrupt

- Timer 7 interrupt

- Timer 7 compare register 2 match interrupt

- Timer 8 interrupt

- Timer 8 compare register 2 match interrupt

- PWM overflow interrupt

- PWM under flow interrupt

- Timer 9 compare register 2 match interrupt

- 24H timer interrupt

- Alarm match interrupt

<Serial interrupt>

- CAN interrupt

- LIN interrupt

- Serial 0 interrupt

- Serial 0 UART reception interrupt

- Serial 1 interrupt

- Serial 1 UART reception interrupt

- Serial 2 interrupt

- Serial 2 UART reception interrupt

- Serial 4 interrupt

- Serial 4 stop condition interrupt

<A/D interrupt>

- A/D conversion interrupt
 - <Data automatic transfer interrupt>
 - ATC1 interrupt
 - <Low voltage detection interrupt>
 - Low voltage detection interrupt
 - <External interrupt>
 - IRQ0 : Edge selection, noise filter connectable
 - IRQ1 : Edge selection, noise filter connectable
 - IRQ2 : Edge selection, noise filter connectable, both edge interrupt
 - IRQ3 : Edge selection, noise filter connectable, both edge interrupt
 - IRQ4 : Edge selection, noise filter connectable, both edge interrupt, key scan interrupt
-
- Timer Counter x 12 sets
 - General-purpose 8-bit timer x 5 sets
 - General-purpose 16-bit timer x 2 sets
 - Motor control 16-bit timer x 1 set
 - 8-bit free-run timer x 1 set
 - Time-base timer x 1 set
 - Baud rate timer x 1 set
 - 24H timer x 1 set

Timer 0 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), added pulse (2bit) type PWM output can be output to large current pin TM0IOB, event count, simple pulse width measurement
- Clock source
fppll-div, fppll-div/4, fppll-div/16, fppll-div/32, fppll-div/64, fppll-div/128,
fs/2, fs/4, fs/8, fslow, external clock, timer A output
- Real-time control
Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 1 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), event count
16-bit cascade connection (connected with timer 0), timer synchronous output
- Clock source
fppll-div, fppll-div/4, fppll-div/16, fppll-div/32, fppll-div/64, fppll-div/128,
fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 2 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), added pulse (2bit) type PWM output can be output to large current pin TM2IOB, event count, simple pulse width measurement,
24-bit cascade connection (connected with timer 0, 1), timer synchronous output

- Double-buffered compare register (x1)
- Clock source
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
fs/2, fs/4, fs/8, fslow, external clock, timer A output
- Real-time control
Timer (PWM) output is controlled among the three values: “Fixed to High”, “Fixed to Low”, or
“Hi-Z” at falling edge of external interrupt 0 (IRQ0)

Timer 3 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), event count
16-bit cascade connection (connected with timer 2),
32-bit cascade connection (connected with timer 0, 1, 2)
- Double-buffered compare register (x1)
- Clock source
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 4 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), added pulse (2bit) type PWM output,
event count, simple pulse width measurement
- Clock source
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 6 (8-bit free-run timer, time-base timer)

8-bit free-run timer

- Clock source
fpll-div, fpll-div/2², fpll-div/2³, fpll-div/2¹², fpll-div/2¹³, fs, fslow,
fslow/2², fslow/2³, fslow/2¹², fslow/2¹³

Time-base timer

- Interrupt generation cycle
fpll-div/2⁷, fpll-div/2⁸, fpll-div/2⁹, fpll-div/2¹⁰, fpll-div/2¹³,
fpll-div/2¹⁵, fslow/2⁷, fslow/2⁸, fslow/2⁹, fslow/2¹⁰, fslow/2¹³, fslow/2¹⁵

Timer 7 (General-purpose 16-bit timer)

- Clock source
fpll-div, fs, external clock, timer A output, serial 0 transfer clock output,
timer 6 compare match cycle divided by 1, 2, 4, 16
- Hardware configuration
Double-buffered compare register (x2)
Double-buffered input capture register (x2)
Timer interrupt (x2 vector)
- Timer function
Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous
changeable) can be output to large current pin TM7IOB, timer synchronous output, event count,
input capture function (both edges operable)

- Real-time control
Timer (PWM) output is controlled among the three values: “Fixed to High”, “Fixed to Low”, or “Hi-Z” at falling edge of external interrupt 0 (IRQ0)

Timer 8 (General-purpose 16-bit timer)

- Clock source
fppll-div, fs, external clock, timer A output, timer 6 compare match cycle divided by 1, 2, 4, 16
- Hardware configuration
Double-buffered compare register (x2)
Double-buffered input capture register (x1)
Timer interrupt (x2 vector)
- Timer function
Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture function (both edges operable)
32-bit cascade connection (connected with timer 7), 32-bit PWM output,
Input capture is available in 32-bit cascade

Timer 9 (Motor control 16-bit timer)

- Clock source
fppll-div, fs, external clock, Timer A output divided by 1, 2, 4, 16
- Hardware configuration
Double-buffered compare register (x2)
Timer interrupt (x3 vector)
- Timer function
Square wave output (Timer pulse output), switchable to large current output, complementary 3-phase PWM output,
Triangle wave and saw tooth wave are supported, dead time insertion available, event count
- Pin output control
PWM output control is possible by external interrupt 0 to 4 (IRQ 0 to 4)
("Hi-z", output data fixed)

Timer A (baud rate timer)

Clock output for peripheral functions

- Clock source
fppll-div divided by 1/1, 2, 4, 8, 16, 32, and fs divided by 2, 4

24H timer

- Clock source (Usable frequency)
fppll (4 MHz, 4.19 MHz, 5 MHz, 8 MHz, 8.38 MHz, 10 MHz, 16 MHz, 16.77 MHz, 20 MHz) fx (32.768 kHz), frc (20 MHz, 16 MHz), frcs (30 kHz)
- Hardware configuration
0.5 seconds counter, minute counter, hour counter
Alarm compare register (in 0.5 seconds, in minutes, in hours) (x1)
Timer interrupt (x2 vector)
- Timer function
Interval function (interrupts every 0.5 seconds, 1 second, 1 minute, 1 hour, 24 hours)
Alarm function

- Watchdog timer
 - Overrun detection cycle is selectable from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
 - Forced to reset inside LSI by hardware when a software processing error is detected twice
- Watchdog timer2
 - Overrun detection cycle is selectable from $frcs/2^4$, $frcs/2^5$, $frcs/2^6$, $frcs/2^7$, $frcs/2^8$, $frcs/2^9$, $frcs/2^{10}$, $frcs/2^{11}$, $frcs/2^{12}$, $frcs/2^{13}$, $frcs/2^{14}$, $frcs/2^{15}$
 - Forced to reset inside LSI by hardware when a software processing error is detected twice
- Synchronous output function (Timer synchronous output, interrupt synchronous output)
 - Latch data is output from port 8 at the event timing of synchronous output signal of timer 1, timer 2, timer 7, or external interrupt2 (IRQ2)
- A/D converter 10 bit x 12 channels
- Data automatic transfer 1 system
 - ATC1
 - Data is automatically transferred in all memory space
 - External interrupt activation/internal event activation/software activation
 - Max. 255 byte continuous transfer
 - Serial continuous transmission and reception is supported
 - Burst transfer function (Including interrupt emergency stop)
- CAN Controller
 - Channels: 1 channel
 - CAN 2.0B specification basis
 - Communication method: NRZ (Non-Return to Zero)
 - Transmission line: Bidirectional 2-wire serial communication
 - Communication speed: Max. 1 Mbps
 - Data length: 0 to 8 byte
 - Message frame: Standard frame and extended frame are supported
 - Standard frame format ID: 11 bits
 - Extended frame format ID: 29 bits
 - Buffer size: 32 messages (32 x 132 bit)
 - Interrupt 1 set
 - Interrupt source
 - Transition from bus off state to error active state, or back transition

- Transition from warning error condition (error counter indicates 96 or more) to warning error condition released (error counter indicates less than 96) or back transition
- Transmission completion
- Transmission/reception error (Ack/Form/Stuff/Bit1/Bit0/CRC errors)

- Serial Interface: 4 systems

Serial 0 (Hardware LIN / Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)

- Parity check, overrun error/framing error are detected
- Transfer bits 7 to 8 are selectable
- Hardware LIN
Synch Break generation, Wake-up detection, Synch Break detection, Synch Field measurement are available

Serial 1 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)

- Parity check, overrun error/framing error are detected
- Transfer bits 7 to 8 are selectable

serial 2 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)

- Parity check, overrun error/framing error are detected
- Transfer bits 7 to 8 are selectable

Serial 4 (Multi master IIC / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Multi master IIC

- 7, 10-bit slave address is settable
- General call communication mode is supported

- Auto reset circuit

- Low voltage detection circuit

- Clock monitoring function

- LED driver: 6 sets

- LCD driver

LCD driver pins

Segment output: Max. 32 pins (SEG0-31)

SEG0-31 can be switched to I/O port in pins.
(Note) At reset, SEG0-31 are input ports.

Common output pins: 4 pins

COM0-3 can be switched to I/O port in pins.

Display mode selection

Static

1/2 duty, 1/2 bias

1/3 duty, 1/3 bias

1/4 duty, 1/3 bias

LCD driver clock

- When source clock is main clock (fpll)
 $1/2^{18}, 1/2^{17}, 1/2^{16}, 1/2^{15}, 1/2^{14}, 1/2^{13}, 1/2^{12}, 1/2^{11}$
- When source clock is sub clock (fslow)
 $1/2^9, 1/2^8, 1/2^7, 1/2^6$
- Timer 0 to 4, Timer A output

LCD power

LCD power is separated from V_{DD50} (can be used when $V_{LC1} \leq V_{DD50}$)

Supply voltage can be selected externally.

(External supply voltage is supplied from VLC1, VLC2, and VLC3 pins, or can be used by dividing the voltage added to VLC1 pin by internal resistor.)

- Ports

I/O ports	54 pins
LCD segment	32 pins
LCD common	4 pins
CAN	4 pins
Serial	15 pins
Timer I/O	21 pins
A/D input	12 pins
External interrupt	5 pins
LCD power	3 pins
LED (large current) driver	6 pins
High-speed oscillation	2 pins
Low-speed oscillation	2 pins
Special pins	10 pins
Operating mode input pins	3 pins
Reset input pins	1 pin
Analog reference voltage input pin	1 pin
Power pins	4 pins

1.3 Pin Description

1.3.1 Pin configuration

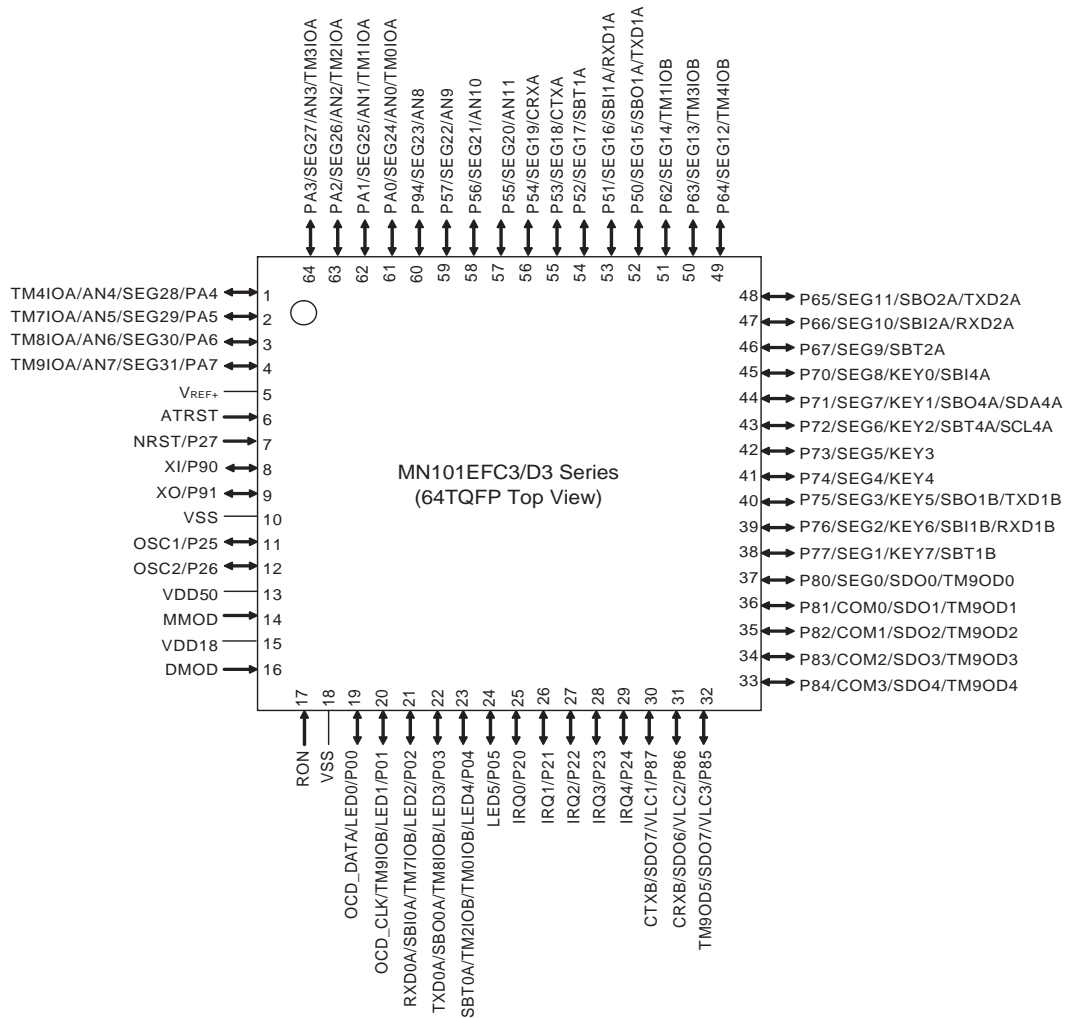


Figure:1.3.1 Pin Configuration

1.3.2 Pin Specification

Table:1.3.1 Pin Specification

Pins	Special functions	I/O	Direction control	Pin control	Function Description	
P00 P01 P02 P03 P04 P05	LED0 LED1 OCD_CLK LED2 SBI0A LED3 SBO0A LED4 TM2IOB LED5	OCD_DATA TM9IOB TM7IOB RXD0A TM8IOB TXD0A TM0IOB SBT0A	in/out in/out in/out in/out in/out in/out in/out	P0DIR0 P0DIR1 P0DIR2 P0DIR3 P0DIR4 P0DIR5	P0PLUD0 P0PLUD1 P0PLUD2 P0PLUD3 P0PLUD4 P0PLUD5	LED0: LED driver pin 0 LED1: LED driver pin 1 OCD_CLK: On-board programmer Clock supply pin LED2: LED driver pin 2 SBI0A: Serial 0 data input LED3: LED driver pin 3 SBO0A: Serial 0 data output LED4: LED driver pin 4 TM2IOB: Timer 2 I/O LED5: LED driver pin 5 OCD_DATA: On-board programmer Data pin TM9IOB: Timer 9 I/O TM7IOB: Timer 7 I/O RXD0A: UART0 data input TM8IOB: Timer 8 I/O TXD0A: UART0 data I/O TM0IOB: Timer 0 I/O SBT0A: Serial 0 clock I/O
P20 P21 P22 P23 P24 P25 P26 P27	IRQ0 IRQ1 IRQ2 IRQ3 IRQ4 OSC1 OSC2 NRST		in/out in/out in/out in/out in/out in/out in/out	P2DIR0 P2DIR1 P2DIR2 P2DIR3 P2DIR4 P2DIR5 P2DIR6 P2DIR7	P2PLU0 P2PLU1 P2PLU2 P2PLU3 P2PLU4 P2PLU5 P2PLU6 P2PLU7	IRQ0: External interrupt 0 IRQ1: External interrupt 1 IRQ2: External interrupt 2 IRQ3: External interrupt 3 IRQ4: External interrupt 4 OSC1: Ceramic / crystal high-speed clock input OSC2: Ceramic / crystal high-speed clock output NRST: Reset
P50 P51 P52 P53 P54 P55 P56 P57	SBO1A SEG15 SBI1A SEG16 SBT1A SEG18 SEG19 SEG20 SEG21 SEG22	TXD1A RXD1A SEG17 CTXA CRXA AN11 AN10 AN9	in/out in/out in/out in/out in/out in/out in/out	P5DIR0 P5DIR1 P5DIR2 P5DIR3 P5DIR4 P5DIR5 P5DIR6 P5DIR7	P5PLUD0 P5PLUD1 P5PLUD2 P5PLUD3 P5PLUD4 P5PLUD5 P5PLUD6 P5PLUD7	SBO1A: Serial 1 data output SEG15: Segment 15 output SBI1A: Serial 1 data input SEG16: Segment 16 output SBT1A: Serial 1 clock I/O SEG18: Segment 18 output SEG19: Segment 19 output SEG20: Segment 20 output SEG21: Segment 21 output SEG22: Segment 22 output TXD1: UART1 data input RXD1A: UART1 data output SEG17: Segment 17 output CTXA: CAN data transmission pin A CRXA: CAN data reception pin A AN11: Analog 11 input AN10: Analog 10 input AN9: Analog 9 input
P62 P63 P64 P65 P66 P67	TM1IOB TM3IOB TM4IOB SBO2A SEG11 SBI2A SEG10 SBT2A	SEG14 SEG13 SEG12 TXD2A RXD2A SEG9	in/out in/out in/out in/out in/out in/out	R6DIR2 R6DIR3 R6DIR4 R6DIR5 R6DIR6 R6DIR7	P6PLU2 P6PLU3 P6PLU4 P6PLU5 P6PLU6 P6PLU7	TM1IOB: Timer 1 I/O TM3IOB: Timer 3 I/O TM4IOB: Timer 4 I/O SBO2A: Serial 2 data output SEG11: Segment output 11 SBI2A: Serial 2 data output SEG10: Segment output 10 SBT2A: Serial 2 clock I/O SEG14: Segment 14 output SEG13: Segment 13 output SEG12: Segment 12 output TXD2A: UART2 data output RXD2A: UART2 data input SEG9: Segment output 9
P70 P71 P72 P73 P74 P75 P76 P77	KEY0 SEG8 KEY1 SDA4A KEY2 SCL4A KEY3 KEY4 KEY5 TXD1B KEY6 RXD1B KEY7 SEG1	SBI4A SBO4A SEG7 SBT4A SEG6 SEG5 SEG4 SBO1B SEG3 SBI1B SEG2 SBT1B	in/out in/out in/out in/out in/out in/out in/out in/out	P7DIR0 P7DIR1 P7DIR2 P7DIR3 P7DIR4 P7DIR5 P7DIR6 P7DIR7	P7PLUD0 P7PLUD1 P7PLUD2 P7PLUD3 P7PLUD4 P7PLUD5 P7PLUD6 P7PLUD7	KEY0: KEY interrupt input 0 SEG8: Segment output 8 KEY1: KEY interrupt input 1 SDA4A: IIC4 data I/O KEY2: KEY interrupt input 2 SCL4A: IIC clock I/O KEY3: KEY interrupt input 3 KEY4: KEY interrupt input 4 KEY5: KEY interrupt input 5 TXD1B: UART1 data output KEY6: KEY interrupt input 6 RXD1B: UART1 data input KEY7: KEY interrupt input 7 SEG1: Segment output 1 SBI4A: Serial 4 data output SBO4A: Serial 4 data output SEG7: Segment output 7 SBT4A: Serial 4 clock I/O SEG6: Segment output 6 SEG5: Segment output 5 SEG4: Segment output 4 SBO1B: Serial 1 data output SEG3: Segment output 3 SBI1B: Serial 1 data output SEG2: Segment output 2 SBT1B: Serial 1 clock I/O
P80 P81 P82 P83 P84 P85	SDO0 SEG0 SDO1 COM0 SDO2 COM1 SDO3 COM2 SDO4 COM3 SDO5 VLC3	TM9OD0 TM9OD1 TM9OD2 TM9OD3 TM9OD4 TM9OD5	in/out in/out in/out in/out in/out in/out	P8DIR0 P8DIR1 P8DIR2 P8DIR3 P8DIR4 P8DIR5	P8PLU0 P8PLU1 P8PLU2 P8PLU3 P8PLU4 P8PLU5	SDO0: Timer synchronous output 0 SEG0: Segment output 0 SDO1: Timer synchronous output 1 COM0: LCD common output SDO2: Timer synchronous output 2 COM1: LCD common output SDO3: Timer synchronous output 3 COM2: LCD common output SDO4: Timer synchronous output 4 COM3: LCD common output SDO5: Timer synchronous output 5 VLC3: LCD power TM9OD0: Timer 9 output TM9OD1: Timer 9 output TM9OD2: Timer 9 output TM9OD3: Timer 9 output TM9OD4: Timer 9 output TM9OD5: Timer 9 output

Pins	Special functions	I/O	Direction control	Pin control	Function Description		
P86	SDO6 VLC2	CRXB	in/out	P8DIR6	P8PLU6	SDO6: Timer synchronous output 6 VLC2: LCD power	CRXB: CAN data reception pin B
P87	SDO7 VLC1	CTXB	in/out	P8DIR7	P8PLU7	SDO7: Timer synchronous output 7 VLC1: LCD power	CTXB: CAN data transmission pin B
P90	XI		in/out	P9DIR0	P9PLU0	XI: Ceramic / crystal low-speed clock input	
P91	XO		in/out	P9DIR1	P9PLU1	XO: Ceramic / crystal low-speed clock output	
P94	AN8	SEG23	in/out	P9DIR4	P9PLU4	AN12: Analog 8 input	SEG29: Segment output 23
PA0	AN0 SEG24	TM0IOA	in/out	PADIR0	PAPLUD0	AN0: Analog 0 input SEG24: Segment output 24	TM0IOA: Timer 0 I/O
PA1	AN1 SEG25	TM1IOA	in/out	PADIR1	PAPLUD1	AN1: Analog 1 input SEG25: Segment output 25	TM1IOA: Timer 1 I/O
PA2	AN2 SEG26	TM2IOA	in/out	PADIR2	PAPLUD2	AN2: Analog 2 input SEG26: Segment output 26	TM2IOA: Timer 2 I/O
PA3	AN3 SEG27	TM3IOA	in/out	PADIR3	PAPLUD3	AN3: Analog 3 input SEG27: Segment output 27	TM3IOA: Timer 3 I/O
PA4	AN4 SEG28	TM4IOA	in/out	PADIR4	PAPLUD4	AN4: Analog 4 input SEG28: Segment output 28	TM4IOA: Timer 4 I/O
PA5	AN5 SEG29	TM7IOA	in/out	PADIR5	PAPLUD5	AN5: Analog 5 input SEG29: Segment output 29	TM7IOA: Timer 7 I/O
PA6	AN6 SEG30	TM8IOA	in/out	PADIR6	PAPLUD6	AN6: Analog 6 input SEG30: Segment output 30	TM8IOA: Timer 8 I/O
PA7	AN7 SEG31	TM9IOA	in/out	PADIR7	PAPLUD7	AN7: Analog 7 input SEG31: Segment output 31	TM9IOA: Timer 9 I/O

1.3.3 Pin Functions

Table:1.3.2 Pin Functions

Pins	Pin No.	I/O	Other Functions	Functions	Descriptions
VSS VDD50	10, 18 13	-		Power supply pins	Supply 1.8 V to 5.5 V to VDD50, and 0 V to VSS. Connect 0.1 μ F and more than 1 μ F of bypass capacitor for internal power stabilization.
VDD18	15	-		Internal power output pin	Outputs internal power voltage 1.8 V. Connect 0.1 μ F and 1 μ F of bypass capacitor between VDD18 and VSS pins for internal power stabilization. This is the power pin for microcontroller internal power supply. Do not connect external power supply from this pin.
OSC1 OSC2	11 12	Input Output	P25 P26	High-speed operation clock input pin High-speed operation clock output pin	Connect these oscillation pins to ceramic oscillator or crystal oscillator for high-speed operation clock. For external clock input, input to OSC1 and open OSC2. The chip will not operate with an external clock when using either STOP mode or SLOW mode.
XI XO	8 9	Input Output	P90 P91	Low-speed operation clock input pin Low-speed operation clock output pin	Connect these oscillation pins to ceramic oscillator or crystal oscillator for low-speed operation clock. For external clock input, input to XI and open XO. The chip will not operate with an external clock when using STOP mode.
NRST	7	Input	P27	Reset pin [Active low]	This pin resets the chip at power on, is allocated as P27 and contains an internal pull-up resistor (Type. 50 k Ω). Setting this pin low initializes the internal state of the LSI. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if "0" is written to P27 and the reset is initiated by software, a low level will be output. The output has an Nch open-drain configuration. If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and V _{DD50} .
ATRST	6	Input		Auto reset setting pin	Input "H" to enable auto reset function and "L" to disable this function
P00 P01 P02 P03 P04 P05	19 20 21 22 23 24	I/O	LED0 LED1 OCD_CLK LED2 SBI0A LED3 SBO0A LED4 TM2IOB LED5	OCD_DATA TM9IOB TM7IOB RXD0A TM8IOB TXD0A TM0IOB SBT0A	I/O port 0 6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P0PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P20 P21 P22 P23 P24 P25 P26	25 26 27 28 29 11 12	I/O	IRQ0 IRQ1 IRQ2 IRQ3 IRQ4 OSC1 OSC2		I/O port 2 7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P27	7	Input	NRST		Input port 2 P27 is an Nch open-drain port. When "0" is written and the reset is initiated by software, a low level will be output.

Pins	Pin No.	I/O	Other Functions	Functions	Descriptions	
P50	52	I/O	SBO1A SEG15	TXD1A	I/O port 5 8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P5PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)	
P51	53		SBI1A SEG16	RXD1A		
P52	54		SBT1A	SEG17		
P53	55		SEG18	CTXA		
P54	56		SEG19	CRXA		
P55	57		SEG20	AN11		
P56	58		SEG21	AN10		
P57	59		SEG22	AN9		
P62	51	I/O	TM1IOB TM3IOB	SEG14 SEG13	I/O port 6 6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)	
P63	50		TM4IOB	SEG12		
P64	49		SBO2A	TXD2A		
P65	48		SEG11			
P66	47		SBI2A SEG10	RXD2A		
P67	46		SBT2A	SEG9		
P70	45	I/O	KEY0 SEG8	SBI4A	I/O port 7 8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P7PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)	
P71	44		KEY1 SDA4A	SBO4A SEG7		
P72	43		KEY2 SCL4A	SBT4A SEG6		
P73	42		KEY3	SEG5		
P74	41		KEY4	SEG4		
P75	40		KEY5 TXD1B	SBO1B SEG3		
P76	39		KEY6 RXD1B	SBI1B SEG2		
P77	38		KEY7 SEG1	SBT1B		
P80	37	I/O	SDO0 SEG0	TM9OD0		I/O port 8 8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P81	36		SDO1 COM0	TM9OD1		
P82	35		SDO2 COM1	TM9OD2		
P83	34		SDO3 COM2	TM9OD3		
P84	33		SDO4 COM3	TM9OD4		
P85	32		SDO5 VLC3	TM9OD5		
P86	31		SDO6 VLC2	CRXB		
P87	30		SDO7 VLC1	CTXB		
P90	8	I/O	XI		I/O port 9 3-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)	
P91	9		XO			
P94	60		AN8	SEG23		

Pins	Pin No.	I/O	Other Functions	Functions	Descriptions	
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	61 62 63 64 1 2 3 4	I/O	AN0 SEG24 AN1 SEG25 AN2 SEG26 AN3 SEG27 AN4 SEG28 AN5 SEG29 AN6 SEG30 AN7 SEG31	TM0IOA TM1IOA TM2IOA TM3IOA TM4IOA TM7IOA TM8IOA TM9IOA	I/O port A	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up /pull-down resistor for each bit can be selected individually by the PAPLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD2 register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
SBO0A SBO1A SBO1B SBO2A SBO4A	22 52 40 48 44	I/O	P03 TM8IOB P50 TXD1A P75 TXD1B P65 TXD2A P71 SDA4A	TXD0A LED3 SEG15 SEG3 KEY5 SEG11 SEG7 KEY1	Serial interface transmission data output pins	Transmission data output pins for serial interface 0, 1, 2, and 4. The output configuration, either COMS push-pull or Nch open-drain can be selected by the P0ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P5PLUD, P6PLU and P7PLUD registers. Select the output mode by the P0DIR, P5DIR, P6DIR and P7DIR registers to select serial data output by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0A SBI1A SBI1B SBI2A SBI4A	21 53 39 47 45	I/O	P02 TM7IOB P51 RXD1A P76 RXD1B P66 RXD2A P70 KEY0	RXD0A LED2 SEG16 SEG2 KEY6 SEG10 SEG8	Serial interface reception data input pins	Reception data input pins for serial interface 0, 1, 2, and 4. Pull-up resistor can be selected by the P0PLUD, P5PLUD, P6PLU and P7PLUD registers. Select input mode by the P0DIR, P5DIR, P6DIR and P7DIR registers to select serial data input by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBT0A SBT1A SBT1B SBT2A SBT4A	23 54 38 46 43	I/O	P04 TM0IOB P52 P77 KEY7 P67 P72 SCL4A	TM2IOB LED4 SEG17 SEG1 SEG9 SEG6 KEY2	Serial interface clock I/O pins	Clock I/O pins for serial interface 0, 1, 2, and 4. The output configuration, either CMOS push-pull or Nch open-drain can be selected with the P0ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P5PLUD, P6PLU and P7PLUD registers. Select input mode or output mode by the P0DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1, SC1MD1, SC2MD1 to SC4MD1) according to the communication mode. These can be used as normal I/O pins when the serial interface is not used.
TXD0A TXD1A TXD1B TXD2A	22 52 40 48	Output	P03 TM8IOB P50 SBO1A P75 SBO1B P65 SBO2A	SBO0A LED3 SEG15 SEG3 KEY5 SEG11	UART transmission data output pins	In the serial interface 0, 1, and 2 in UART mode, these pins are configured as the transmission data output pin. The output configuration, either CMOS push-pull or Nch open-drain can be selected with the P0ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P5PLUD, P6PLU, and P7PLUD registers. Select output mode by the P0DIR, P5DIR, P6DIR and P7DIR registers to select serial data output by the serial mode register 1 (SC0MD1 to SC2MD1). These can be used as normal I/O pins when the serial interface is not used.

Pins	Pin No.	I/O	Other Functions	Functions	Descriptions	
RXD0A RXD1A RXD1B RXD2A	21 53 39 47	Input	P02 TM710B P51 SB11A P76 SB11B P66 SBI2A	SB10A LED2 SEG16 SEG2 KEY6 SEG10	UART reception data input pins	In the serial interface 0, 1, and 2 in UART mode, these pins are configured as the reception data input pin. Pull-up resistor can be selected by the P0PLUD, P5PLUD, P6PLU, and P7PLUD registers. Select input mode by the P0DIR, P5DIR, P6DIR and P7DIR registers to select serial data input by the serial mode register 1 (SC0MD1 to SC2MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA4A	44	I/O	P71 SBO4A	SEG7 KEY1	IIC data I/O pins	In the serial interface 4 in IIC mode, these pins are configured as the data input / output pin. For the output configuration, select Nch open-drain by the P7ODC register to select pull-up resistor by the P7PLUD register. Select output mode by the P7DIR register to select serial data input / output by the serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SCL4A	43	I/O	P72 SBT4A	SEG6 KEY2	IIC clock I/O pins	In the serial interface 4 in IIC mode, these pins are configured as the clock input / output pin. For the output configuration, select Nch open-drain by the P7ODC register to select pull-up resistor by the P7PLUD register. Select output mode by the P7DIR register to select clock data input / output by the serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
CTXA CTXB	55 30	Output	P53 P87 VLC1	SEG18 SDO7	CAN data transmission pins	CAN controller transmission data output pin. Pull-up resistor can be selected by the P8PLU and P5PLUD registers. Nch open-drain can be selected by the P8ODC and the P5ODC registers. Select CAN output by the CANPMD register to select output mode by the P8DIR and P5DIR registers. These can be used as normal I/O pins when the CAN controller is not used.
CRXA CRXB	56 31	Input	P54 P86 VLC2	SEG19 SDO6	CAN data reception pins	CAN controller reception data input pin. Pull-up resistor can be selected by the P8PLU and P5PLUD registers. Nch open-drain can be selected by the P8ODC and the P5ODC registers. Select CAN input by the CANPMD register to select input mode by the P8DIR and P5DIR registers. These can be used as normal I/O pins when the CAN controller is not used.
TM0IOA TM0IOB TM1IOA TM1IOB TM2IOA TM2IOB TM3IOA TM3IOB TM4IOA TM4IOB	61 23 62 51 63 23 64 50 1 49	I/O	PA0 SEG24 P04 TM2IOB PA1 SEG25 P62 PA2 AN2 P04 TM0IOB PA3 SEG27 P63 PA4 SEG28 P64	AN0 SBT0A LED4 AN1 SEG14 SEG26 SBT0A LED4 AN3 SEG13 AN4 SEG12	Timer I/O pins	Event count clock input, timer output, and PWM signal output pins for 8-bit timer 0 to 4. To use these pins for event clock input, input mode can be selected by the P0DIR, P6DIR, PADIR, TMCKSEL1, TMINSEL1, and TMINSEL2 registers. In input mode, pull-up resistors can be selected by the P0PLUD, P6PLU, and PAMPLUD register. To use these pins for timer output or PWM signal output, select special function pins by the port 0 output mode register, port 6 output mode register, and port A output mode register (P0OMD1, P0OMD2, P6OMD, and PAOMD1) to select output mode by the P0DIR, P6DIR, and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.

Pins	Pin No.	I/O	Other Functions		Functions	Descriptions
TM7IOA	2	I/O	PA5	AN5	Timer I/O pins	Event count clock input, timer output, and PWM signal output pins for 16-bit timer 7, 8, and 9. To use these pins for event clock input, input mode can be selected by the P0DIR and PADIR registers. In input mode, pull-up resistors can be selected by the P0PLUD and PAPLUD register. To use these pins for timer output or PWM signal output, select special function pins by the port 0 output mode register and port A output mode register (P0OMD1, PAOMD1) to select output mode by the P0DIR and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.
TM7IOB	21		SEG29	RXD0A		
TM8IOA	3		P02	LED02		
TM8IOB	22		SBIOA	AN6		
TM9IOA	4		PA6	AN6		
TM9IOB	20		SEG30	TXD0A		
			SBO0A	LED3		
			PA7	AN7		
			SEG31	OCD_CLK		
			P01			
			LED1			
TM9OD0	37	Output	P80	SEG0	Timer output pins	Timer output and PWM signal output pins for 16-bit timer 7, 8, and 9. To use these pins for timer output or PWM signal output, select special function pins by the P8OMD register to select output mode by the P8DIR register. These can be used as normal I/O pins when not used as timer I/O pins.
TM9OD1	36		SD00	COM0		
TM9OD2	35		P81	COM1		
TM9OD3	34		SD01	COM2		
TM9OD4	33		P82	COM3		
TM9OD5	32		SD02	VCL3		
			P83			
		P84				
		SD03				
		P85				
		SD04				
		P86				
		SD05				
SDO0	37	Output	P80	SEG0	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 8 synchronous output control register (P8SYO). To use these pins for synchronous output, set output mode by the P8DIR register. These pins can be used as normal I/O pins when not used as synchronous output pins.
SDO1	36		TM9OD0	COM0		
SDO2	35		P81	COM1		
SDO3	34		TM9OD1	COM2		
SDO4	33		P82	COM3		
SDO5	32		TM9OD2	VCL3		
SDO6	31		P83	VCL2		
SDO7	30		TM9OD3	VCL1		
			P84			
		TM9OD4				
		P85				
		TM9OD5				
		P86				
		CRXB				
		P87				
		CTXB				
Vref+	5	-			Plus power supply pin for A/D converter	Reference power supply pin for the A/D converter. This pin is generally used as $V_{ref+} = V_{DD50}$.

Pins	Pin No.	I/O	Other Functions	Functions	Descriptions
AN0	61	Input	PA0	TM0IOA	Analog input pins Analog input pins for 12-channel, 10-bit A/D converter. These pins can be used as normal I/O pins when not used as analog input pins.
AN1	62		SEG24	TM1IOA	
AN2	63		PA1	TM2IOA	
AN3	64		SEG25	TM3IOA	
AN4	1		PA2	TM4IOA	
AN5	2		SEG26	TM5IOA	
AN6	3		PA3	TM6IOA	
AN7	4		SEG27	TM7IOA	
AN8	60		PA4	SEG23	
AN9	59		SEG28	SEG22	
AN10	58		PA5	SEG21	
AN11	57		SEG29	SEG20	
IRQ0	25	Input	P20		External interrupt input pins External interrupt input pins. The valid edge for IRQ0 to 4 can be selected by the IRQnICR register. For IRQ2, IRQ3, and IRQ4, interrupt setting can be configured at both edges at pin voltage level. These pins can be used as normal I/O pins when not used as external interrupt pins.
IRQ1	26		P21		
IRQ2	27		P22		
IRQ3	28		P23		
IRQ4	29		P24		
KEY0	45		P70	SEG8	Key interrupt input pins Input pins for interrupt based on ORed result of pin inputs. These can be set as key input pins in increments of one bit by the key interrupt control registers (KEYT3_1IMD, KEYT3_2IMD). These pins can be used as normal I/O pins when not used as the key input pins.
KEY1	44		SBI4A	SEG7	
KEY2	43		SDA4A	SBO4A	
KEY3	42		P72	SEG6	
KEY4	41		SCL4A	SBT4A	
KEY5	40		P73	SEG5	
KEY6	39		P74	SEG4	
KEY7	38		P75	SEG3	
LED0	19		P00	OCD_DAT A	LED driver pins Large current output pins. These pins can be used as normal I/O pins when not used as the LED driver pins.
LED1	20		P01	TM9IOB	
LED2	21		OCD_CLK	TM7IOB	
LED3	22		P02	SBI0A	
LED4	23		RXD0A	TM8IOB	
LED5	24		P03	SB00A	
			P04	TM0IOB	
		SBT0A	TM2IOB		
		P05			

Pins	Pin No.	I/O	Other Functions	Functions	Descriptions
COM0	36	Output	P81 SDO1	TM9OD1	LCD common output pin These pins output common signal of required timing for LCD display. Connect to the common pins of LCD display panel. When the LCD functions are not used, these pins can be used as normal ports by the setting of the LCD output control register LCCTR0.
COM1	35		P82 SDO2	TM9OD2	
COM2	34		P83 SDO3	TM9OD3	
COM3	33		P84 SDO4	TM9OD4	
VLC1	30	-	P87 SDO7	CTXB	LCD power supply pins Supply for LCD power. Apply voltage of $5.5\text{ V} \geq \text{VLC1} \geq \text{VLC2} \geq \text{VLC3} \geq 0\text{ V}$. When LCD is not used, VLC1 to VLC3 can be used as normal ports by the setting of the LCD output control register 0 (LCCTR0).
VLC2	31		P86 SDO6	CRXB	
VLC3	32		P85 SDO5	TM9OD5	

Pins	Pin No.	I/O	Other Functions	Functions	Descriptions	
SEG0	37	Output	P80	TM9OD0	LCD segment output pins	These pins output segment signal of required timing for LCD display. Connect to the segment pins of the LCD panel. When LCD display is turned off, VSS level is output. These pins can be used as normal ports by the setting of the LCD output control register LCCTR1 to 4. SEGs for each bit can be individually set as a segment pin or a normal port.
SEG1	38		SDO0	SBT1B		
SEG2	39		KEY7	SBI1B		
SEG3	40		P76	SBO1B		
SEG4	41		KEY6	TXD1B		
SEG5	42		RXD1B	KEY5		
SEG6	43		P75	KEY4		
SEG7	44		P74	KYE3		
SEG8	45		P73	SCL4A		
SEG9	46		P72	SBT4A		
SEG10	47		P71	SDA4A		
SEG11	48		P70	SBO4A		
SEG12	49		KEY0	SBI4A		
SEG13	50		P67	SBT2A		
SEG14	51		P66	RXD2A		
SEG15	52		P66	SBI2A		
SEG16	53		P65	TXD2A		
SEG17	54		P65	SBO2A		
SEG18	55		P64	TM4IOB		
SEG19	56		P63	TM3IOB		
SEG20	57		P62	TM1IOB		
SEG21	58		P50	TXD1A		
SEG22	59		P50	SBO1A		
SEG23	60		P51	SBI1A		
SEG24	61		RXD1A			
SEG25	62		P52	SBT1A		
SEG26	63		P53	CTXA		
SEG27	64		P54	CRXA		
SEG28	1		P55	AN11		
SEG29	2		P56	AN10		
SEG30	3		P57	AN9		
SEG31	4	P94	AN8			
MMOD	14	Input	PA0	AN0	Memory mode switch input pins	Fix this pin at V _{SS} level. When flash memory rewriting method is used, refer to [Chapter Internal Flash Memory] of LSI User's Manual for the setting of this pin.
DMOD	16		TM0IOA			
RON	17		PA1	AN1		
			TM1IOA			
			PA2	AN2		
			TM2IOA			
			PA3	AN3		
			TM3IOA			
			PA4	AN4		
			TM4IOA			
		PA5	AN5			
		TM7IOA				
		PA6	AN6			
		TM8IOA				
		PA7	AN7			
		TM9IOB				
				Mode switch input pins	Fix this pin at V _{DD50} level. Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.	
				Regulator control pin	Fix this pin at V _{DD50} level.	

Pins	Pin No.	I/O	Other Functions		Functions	Descriptions
OCD_DATA	19	I/O	P00	LED0	On-board programmer Data pin.	For detail, refer to [Chapter 23 23.3.2 Pin Configuration in Serial Programmer Rewriting] .
OCD_CLK	20	I/O	P01 TM9IOB	LED1	On-board programmer Clock supply in pin.	For detail, refer to [Chapter 23 23.3.2 Pin Configuration in Serial Programmer Rewriting] .



Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.
When using ICE version, connect pull-up resistor to DMOD on the target board.

1.4 Block Diagram

1.4.1 Block Diagram

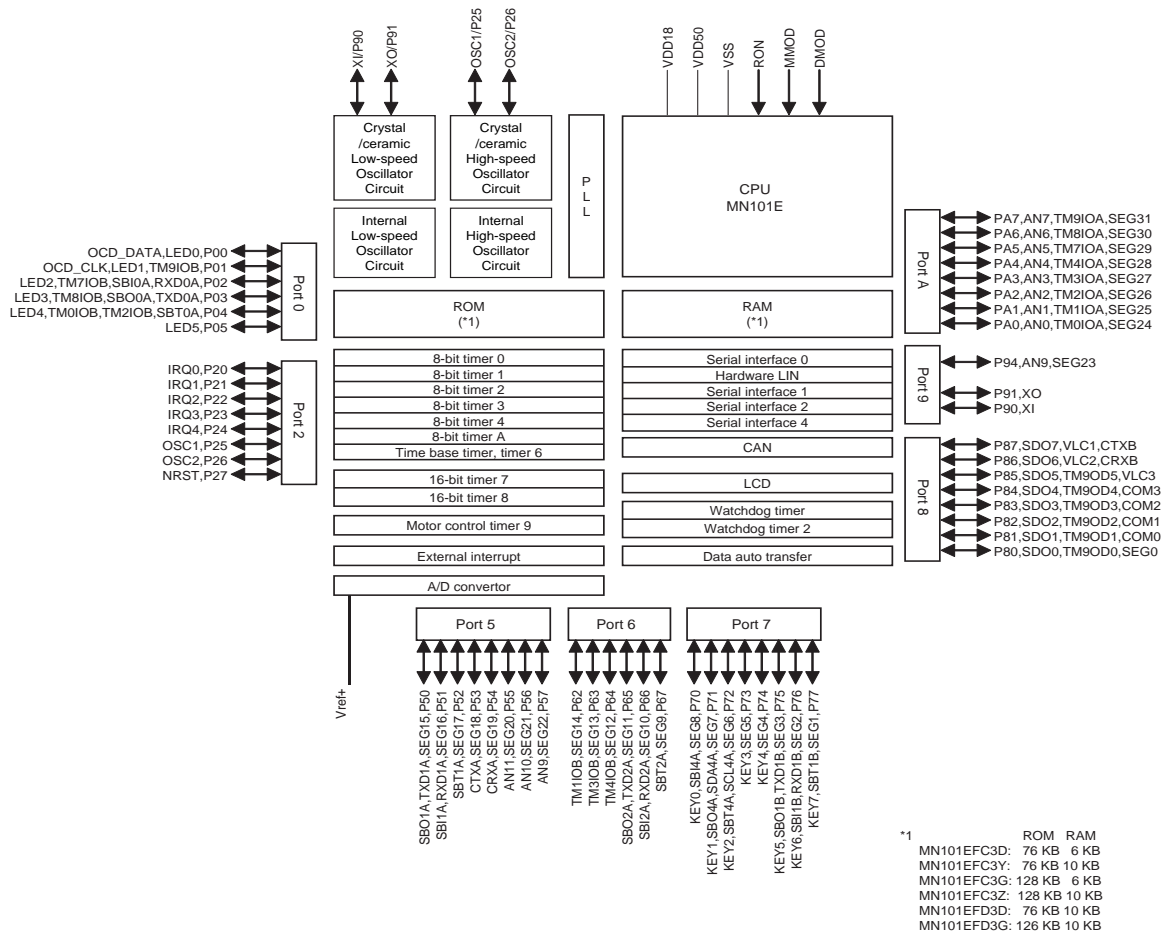


Figure:1.4.1 Block Diagram

1.5 Electrical Characteristics

This LSI manual describes standard specifications.

When using our LSI, please ask our sales offices for the product specifications.

Structure	CMOS integrated circuit
Application	General-purpose
Function	CMOS, 8-bit, single chip microcomputer

1.5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *2 *3 *4

$V_{SS} = 0\text{ V}$

Parameter		Symbol	Rating	Unit		
A1	Power supply voltage	V_{DD50A}	-0.3 to +7.0	V		
A2	Power supply voltage	V_{DD18A}	-0.3 to +2.5			
A3	Input pin voltage	V_{IA}	-0.3 to $V_{DD50} + 0.3$ (upper limit 7.0 V)	V		
A4	Output pin voltage	V_{OA}	-0.3 to $V_{DD50} + 0.3$ (upper limit 7.0 V)			
A5	I/O pin voltage	V_{IO1A}	-0.3 to $V_{DD50} + 0.3$ (upper limit 7.0 V)			
A6	Peak output current	Per pin	"Low-level" output (LED output)	I_{OL1A} (peak)	30	mA
A7			"Low-level" output (Other than LED output)	I_{OL2A} (peak)	20	
A8			"High-level" output	I_{OH_A} (peak)	-10	
A9	Average output current *1	Per pin	"Low-level" output (LED output)	I_{OL1A} (avg)	20	
A10			"Low-level" output (Other than LED output)	I_{OL2A} (avg)	15	
A11			"High-level" output	I_{OHA} (avg)	-5	
A12	Power dissipation	P_{TA}	400	mW		
A13	Operating ambient temperature	T_{oprA}	-40 to +85	°C		
A14	Storage temperature	T_{STGA}	-55 to +125			

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 10 μF or larger between VDD50 pin and GND for the internal power voltage stabilization.

*3 Connect appropriate 0.1 μF or 1.0 μF capacitor between VDD18 pin and VSS pin, near the microcontroller according to the figure shown below for the internal power supply stabilization.

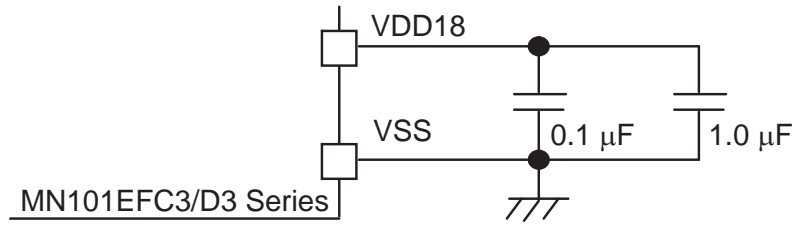


Figure:1.5.1 Capacitor Connection between VDD18 and VSS Pins

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

1.5.2 Operating Conditions

B. Operating Conditions

$V_{SS}=0\text{ V}$
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

Power supply voltage *5

B1	Power supply voltage	V_{DD1}	$f_s \leq 20\text{ MHz}$ *7	2.7		5.5	V
B2		V_{DD2}	$f_s \leq 10\text{ MHz}$ *8	2.7		5.5	
B3		V_{DD3}	$f_s \leq 8\text{ MHz}$ *7	1.8		5.5	
B4		V_{DD4}	$f_s \leq 8\text{ MHz}$ *7, When using internal oscillation *9	2.0		5.5	
B5		V_{DD5}	$f_s \leq 4\text{ MHz}$ *8	1.8		5.5	
B6		V_{DD6}	$f_s \leq 4\text{ MHz}$ *8, When using internal oscillation *10	2.0		5.5	
B7		V_{DD7}	$f_s = 16.384\text{ kHz}$	1.8		5.5	
B8	RAM retention power supply voltage	V_{DD8}	During STOP mode	1.8		5.5	

Operating speed *6

B9	Instruction execution time f_s	t_{c1}	$V_{DD50} = 2.7\text{ V to }5.5\text{ V}$ *7	0.05			μs
B10		t_{c2}	$V_{DD50} = 2.7\text{ V to }5.5\text{ V}$ *8	0.10			
B11		t_{c3}	$V_{DD50} = 1.8\text{ V to }5.5\text{ V}$ *7	0.125			
B12		t_{c4}	$V_{DD50} = 2.0\text{ V to }5.5\text{ V}$ *7, When using internal oscillation *9	0.125			
B13		t_{c5}	$V_{DD50} = 1.8\text{ V to }5.5\text{ V}$ *8	0.25			
B14		t_{c6}	$V_{DD50} = 2.0\text{ V to }5.5\text{ V}$ *8, When using internal oscillation *10	0.25			
B15		t_{c7}	$V_{DD50} = 1.8\text{ V to }5.5\text{ V}$	61.0			

*5 f_s : Machine clock frequency

*6 t_{c1} to 2: when the machine clock is selected from external high-speed oscillation, internal high-speed oscillation, or both the oscillations multiplied by PLL.

t_{c7} : when the machine clock is selected from external low-speed oscillation or internal low-speed oscillation.

*7 When bp2 of the HANDSHAKE register (0x03F06) is set to "1'b1"

*8 When bp2 of the HANDSHAKE register (0x03F06) is set to "1'b0"

*9 When setting $f_{rc}=16\text{ MHz}$, $f_s=f_{rs}/2$

*10 When setting $f_{rc}=16\text{ MHz}$, $f_s=f_{rs}/4$

$V_{SS}=0\text{ V}$

$T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

External Oscillator 1 Figure:1.5.2

B16	Frequency	f_{xtal1}	V_{DD50} is within the specified operating power supply voltage range. ÂiSee the ratings of B1 to B6 for the operating supply voltage range)	2.0	10	MHz
B17	Internal feedback resistor	R_{f10}	$V_{\text{DD50}} = 5.0\text{ V}$		980	$\text{k}\Omega$

External Oscillator 2 Figure:1.5.3

B18	Frequency	f_{xtal2}	$V_{\text{DD50}} = 1.8\text{ V to }5.5\text{ V}$		32.768	kHz
B19	Internal feedback resistor	R_{f20}	$V_{\text{DD50}} = 5.0\text{ V}$		6.2	$\text{M}\Omega$

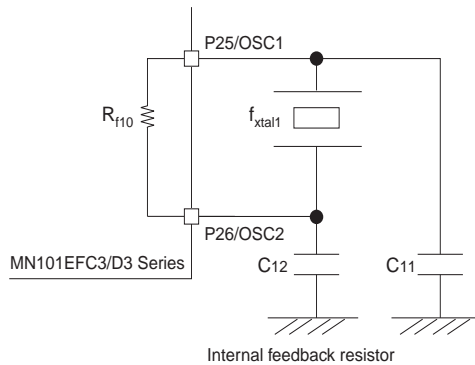


Figure:1.5.2 External Oscillator 1

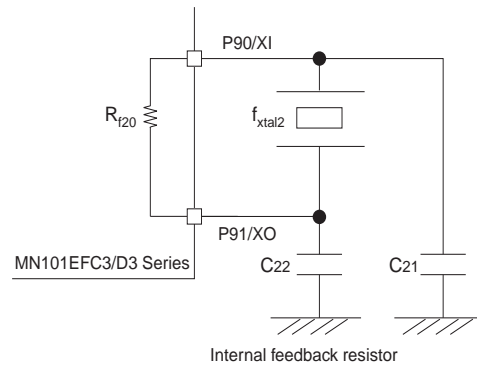


Figure:1.5.3 External Oscillator 2



Connect external capacitors suited for the used oscillator.
When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed depending on the value of capacitor. For external capacity value, please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

$V_{DD50}=1.8\text{ V to }5.5\text{ V}$

$V_{SS}=0\text{ V}$

$T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

External clock input 1 OSC1 (OSC2 is unconnected)

B20	Clock frequency	f_{OSC}		2		10.0	MHz
B21	High-level pulse width *11	t_{wh1}	Figure:1.5.4	45			ns
B22	Low-level pulse width *11	t_{wl1}		45			
B23	Rising time *12	t_{wr1}	Figure:1.5.4	0		5.0	
B24	Falling time *12	t_{wf1}		0		5.0	

External clock input 2 XI (XO is unconnected)

B25	Clock frequency	f_x			32.768		kHz
B26	High-level pulse width *11	t_{wh2}	Figure:1.5.5		4.5		μs
B27	Low-level pulse width *11	t_{wl2}			4.5		
B28	Rising time *12	t_{wr2}	Figure:1.5.5	0		20	ns
B29	Falling time *12	t_{wf2}		0		20	

*11 The clock duty ratio should be 45% to 55%

*12 Rising time and falling time differ depending on the oscillation frequency.

The max value is not a specified value but a rough value.

Please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

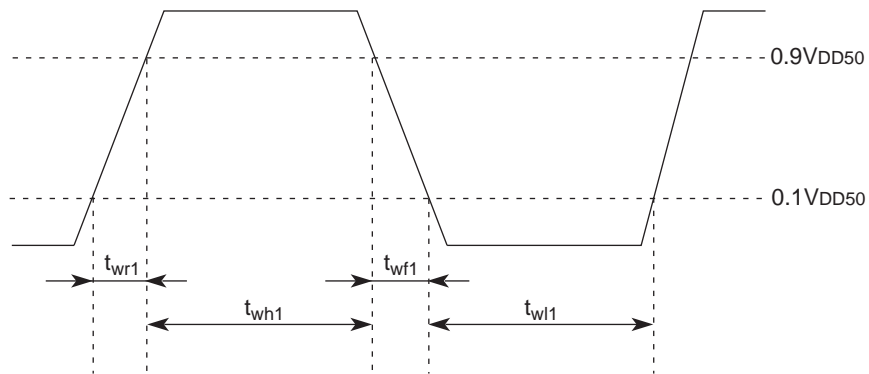


Figure:1.5.4 OSC1 Timing Chart

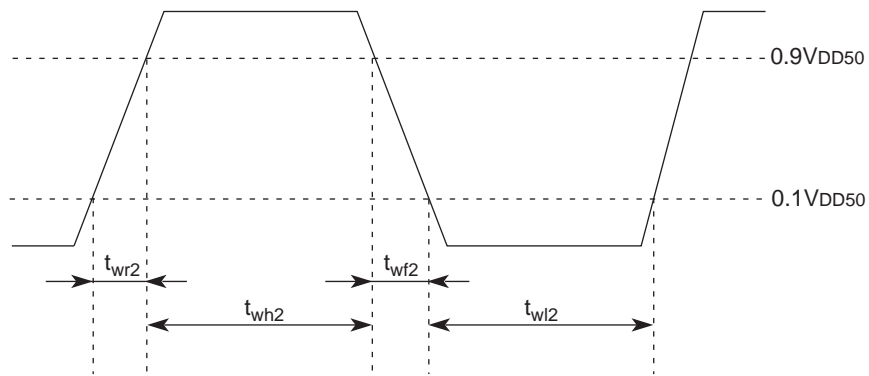


Figure:1.5.5 XI Timing Chart

1.5.3 DC Characteristics

C. DC Characteristics

$V_{SS}=0\text{ V}$

$T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Power supply current *13						
C1	Power supply current during operation	I_{DD1}	fosc=10 MHz [Double-speed mode:fs=fosc] $V_{DD50}=5\text{ V}$ (PLL is not used) *14	5	14	mA
C2		I_{DD2}	fosc=10 MHz [Double-speed mode:fs=fosc] $V_{DD50}=3\text{ V}$ (PLL is not used) *14	5.5		
C3		I_{DD3}	fosc=8 MHz [Double-speed mode:fs=fosc] $V_{DD50}=5\text{ V}$ (PLL is not used) *14	4.5	13	
C4		I_{DD4}	fosc=8 MHz [Double-speed mode:fs=fosc] $V_{DD50}=3\text{ V}$ (PLL is not used) *14	4.5		
C5		I_{DD5}	fosc=4 MHz [Double-speed mode:fs=fosc] $V_{DD50}=5\text{ V}$ (PLL is not used) *15	3.5	11	
C6		I_{DD6}	fosc=4 MHz [Double-speed mode:fs=fosc] $V_{DD50}=3\text{ V}$ (PLL is not used) *15	3.5		
C7		I_{DD7}	fosc=4 MHz [Multiplied by 10:fs=20 MHz] $V_{DD50}=5\text{ V}$ (PLL is used) *14	8	18	
C8		I_{DD8}	fosc=4 MHz [Multiplied by 10:fs=20 MHz] $V_{DD50}=3\text{ V}$ (PLL is used) *14	9		
C9		I_{DD9}	frc=20 MHz [Double-speed mode:fs=frc] $V_{DD50}=5\text{ V}$ (PLL is not used) *14	7.5	16	
C10		I_{DD10}	frc=20 MHz [Double-speed mode:fs=frc] $V_{DD50}=3\text{ V}$ (PLL is not used) *14	8.5		
C11	Power supply current during HALT1	I_{DD11}	frcs=30 kHz [fs=frcs/2] $V_{DD50}=3\text{ V}$ $T_a=25\text{ }^\circ\text{C}$ ROM is executed.	50	65	μA
C12			frcs=30 kHz [fs=frcs/2] $V_{DD50}=3\text{ V}$ $T_a=85\text{ }^\circ\text{C}$ ROM is executed.		150	
C13		I_{DD12}	frcs=30 kHz [fs=frcs/2] $V_{DD50}=3\text{ V}$ $T_a=25\text{ }^\circ\text{C}$ RAM is executed. *16	10	25	
C14			frcs=30 kHz [fs=frcs/2] $V_{DD50}=3\text{ V}$ $T_a=85\text{ }^\circ\text{C}$ RAM is executed. *16		65	
C15	Power supply current during HALT1	I_{DD13}	frcs=30 kHz, $V_{DD50}=3\text{ V}$ $T_a=25\text{ }^\circ\text{C}$	6	15	μA
C16			frcs=30 kHz, $V_{DD50}=3\text{ V}$ $T_a=85\text{ }^\circ\text{C}$		55	
C17	Power supply current during STOP	I_{DD14}	$V_{DD50}=5\text{ V}$, $T_a=25\text{ }^\circ\text{C}$	1	3.5	μA
C18			$V_{DD50}=5\text{ V}$, $T_a=85\text{ }^\circ\text{C}$		50	

*13 Measured without loading (pull-up and pull-down resistors are not connected.)

To measure the power supply current during operation IDD1, 2, 3, 4, and 5:

1, set the all I/O pins to input mode,

2, set the CPU mode to <NORMAL>,

3, fix the MMOD pin at V_{SS} level and input pin at V_{DD50} level

4, and input the rectangular wave of 10 MHz (8 MHz, 4 MHz), which has amplitude of V_{DD50} and V_{SS} potential, from the OSC11 pin.

To measure the power supply current during operation IDD6,

1, set the all I/O pins to input mode,

2, set the CPU mode to <SLOW>,

3, and fix the MMOD pin at V_{SS} level and input pin at V_{DD50} level.

clock is supplied from the internal low-speed oscillation circuit.

To measure the power supply current during HALT1 IDD7,

1, set the all I/O pins to input mode,

2, set the CPU mode to <HALT1>,

3, and fix the MMOD pin at V_{SS} level and input pin at V_{DD50} level.

To measure the power supply current during STOP IDD8,

1, set the CPU mode to <STOP>,

2, and fix the MMOD pin at V_{SS} level and input pin at V_{DD50} level

3, and open the OSC1 pin.

*14 When bp2 of the HANDSHAKE register (0x03F06) is set to "1'b1"

*15 When bp2 of the HANDSHAKE register (0x03F06) is set to "1'b0"

*16 When bp3 of the FEWSPD register (0x03FBF) to "1'b1"

$V_{DD50}=1.8\text{ V to }5.5\text{ V}$ $V_{SS}=0\text{ V}$

$T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

Input pin 1 ATRST, MMOD

C19	Input high voltage	V_{IH1}		$0.8V_{DD50}$		V_{DD50}	V
C20	Input low voltage	V_{IL1}		0		$0.2V_{DD50}$	
C21	Input leakage current	I_{LK1}	$V_{IN} = 0\text{ V to }V_{DD50}$			± 2	μA

Input pin 2 RON

C22	Input high voltage	V_{IH2}		$0.8V_{DD50}$		V_{DD50}	V
C23	Input low voltage	V_{IL2}		0		$0.2V_{DD50}$	
C24	Pull-up resistor	R_{RH1}	$V_{DD50}=5\text{ V}, V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100	$\text{k}\Omega$

Input pin 3 DMOD *17

C25	Input high voltage	V_{IH8}		$0.8V_{DD50}$		V_{DD50}	V
C26	Input low voltage	V_{IL12}		0		$0.2V_{DD50}$	
C27	Pull-up resistor	R_{RH7}	$V_{DD50}=5\text{ V}, V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100	$\text{k}\Omega$

*17 Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.

When using ICE version, connect pull-up resistor to DMOD on the target board

$V_{DD50}=1.8\text{ V to }5.5\text{ V}$ $V_{SS}=0\text{ V}$
 $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

Input pin 4 P27/NRST

C28	Input high voltage	V_{IH3}		$0.8V_{DD50}$		V_{DD50}	V
C29	Input low voltage	V_{IL3}		0		$0.15V_{DD50}$	
C30	Pull-up resistor	R_{RH2}	$V_{DD50}=5\text{ V}$, $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100	k Ω

I/O pin 5 P00 to P05

C31	Input high voltage	V_{IH4}		$0.8V_{DD50}$		V_{DD50}	V
C32	Input low voltage 1	V_{IL4}	Flash option = Normal input level	0		$0.2V_{DD50}$	
C33	Input low voltage 2	V_{IL5}	Flash option = Extended input level $V_{DD50}=4.5\text{ V to }5.5\text{ V}$	0		$0.45V_{DD50}$	
C34	Input leakage current	I_{LK2}	$V_{IN}=0\text{ V to }V_{DD50}$			± 2	μA
C35	Pull-up resistor	R_{RH3}	$V_{DD50}=5\text{ V}$, $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100	k Ω
C36	Pull-down resistor	R_{RL1}	$V_{DD50}=5\text{ V}$, $V_{IN}=V_{DD50}$ Pull-down resistor ON	10	50	100	
C37	Output high voltage	V_{OH1}	$V_{DD50}=5.0\text{ V}$, $I_{OH}=-0.5\text{ mA}$	4.5			V
C38	Output low voltage 1	V_{OL1}	$V_{DD50}=5.0\text{ V}$, $I_{OL}=1.0\text{ mA}$ LED output OFF			0.5	
C39	Output low voltage 2	V_{OL2}	$V_{DD50}=5.0\text{ V}$, $I_{OL}=15.0\text{ mA}$ LED output ON			1.0	

$V_{DD50}=1.8\text{ V to }5.5\text{ V}$ $V_{SS}=0\text{ V}$
 $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

Input pin 6 P20 to P26, P62 to P67, P80 to P87, P90,P91, P94

C40	Input high voltage	V_{IH5}		$0.8V_{DD50}$		V_{DD50}	V
C41	Input low voltage 1	V_{IL6}	Flash option = Normal input level	0		$0.2V_{DD50}$	
C42	Input low voltage 2	V_{IL7}	Flash option = Extended input level $V_{DD50}=4.5\text{ V to }5.5\text{ V}$	0		$0.45V_{DD50}$	
C43	Input leakage current	I_{LK3}	$V_{IN}=0\text{ V to }V_{DD50}$			± 2	μA
C44	Pull-up resistor	R_{RH4}	$V_{DD50}=5.0\text{ V}$, $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100	$\text{k}\Omega$
C45	Output high voltage	V_{OH2}	$V_{DD50}=5.0\text{ V}$, $I_{OH}=-0.5\text{ mA}$	4.5			V
C46	Output low voltage 1	V_{OL3}	$V_{DD50}=5.0\text{ V}$, $I_{OL}=1.0\text{ mA}$			0.5	

Input pin 7 P50 to P57, P70 to P77

C47	Input high voltage	V_{IH6}		$0.8V_{DD50}$		V_{DD50}	V
C48	Input low voltage 1	V_{IL8}	Flash option = Normal input level	0		$0.2V_{DD50}$	
C49	Input low voltage 2	V_{IL9}	Flash option = Extended input level $V_{DD50}=4.5\text{ V to }5.5\text{ V}$	0		$0.45V_{DD50}$	
C50	Input leakage current	I_{LK4}	$V_{IN}=0\text{ V to }V_{DD50}$			± 2	μA
C51	Pull-up resistor	R_{RH5}	$V_{DD50}=5.0\text{ V}$, $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100	$\text{k}\Omega$
C52	Pull-down resistor	R_{RL2}	$V_{DD50}=5.0\text{ V}$, $V_{IN}=V_{DD50}$ Pull-down resistor ON	10	50	100	
C53	Output high voltage	V_{OH3}	$V_{DD50}=5.0\text{ V}$, $I_{OH}=-0.5\text{ mA}$	4.5			V
C54	Output low voltage 1	V_{OL4}	$V_{DD50}=5.0\text{ V}$, $I_{OL}=1.0\text{ mA}$			0.5	

Input pin 8 PA0 to PA7

C55	Input high voltage	V_{IH7}		$0.8V_{DD50}$		V_{DD50}	V
C56	Input low voltage 1	V_{IL10}	Flash option = Normal input level	0		$0.2V_{DD50}$	
C57	Input low voltage 2	V_{IL11}	Flash option = Extended input level $V_{DD50}=4.5\text{ V to }5.5\text{ V}$	0		$0.45V_{DD50}$	
C58	Input leakage current	I_{LK5}	$V_{IN}=0\text{ V to }V_{DD50}$			± 2	μA
C59	Pull-up resistor	R_{RH6}	$V_{DD50}=5.0\text{ V}$, $V_{IN}=V_{SS}$ Pull-up resistor ON	10	50	100	$\text{k}\Omega$
C60	Output high voltage	V_{OH4}	$V_{DD50}=5.0\text{ V}$, $I_{OH}=-0.5\text{ mA}$	4.5			V
C61	Output low voltage	V_{OL5}	$V_{DD50}=5.0\text{ V}$, $I_{OL}=1.0\text{ mA}$			0.5	

$V_{DD50}=1.8\text{ V to }5.5\text{ V}$ $V_{SS}=0\text{ V}$

$T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

Display output pin 1 COM0 to COM3 (At V_{LC1} , V_{SS} Voltage output) *18

C62	Output impedance	Z_{OCOM1}	$V_{DD50}=V_{LC1}=5.0\text{ V}$ $I_{com}=10\text{ }\mu\text{A}$			0.6	V
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Display output pin 2 SEG0 to SEG31 (At V_{LC1} , V_{SS} Voltage output) *19

C63	Output impedance	Z_{OSEG1}	$V_{DD50}=V_{LC1}=5.0\text{ V}$ $I_{seg}=2\text{ }\mu\text{A}$			0.6	V
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Display power pin 1 V_{LC1} , V_{LC2} , V_{LC3}

C64	Internal dividing resistor	R_{VL1}	$T_a=+25\text{ }^\circ\text{C}$ (Impedance between V_{LC1} and V_{SS}) *20	15	30	60	k Ω
C65		R_{VL2}		30	60	120	
C66		R_{VL3}		145	300	570	
C67		R_{VL4}		320	660	1260	

*18 However, COM0 to COM3 are also used as P81 to P84.

*19 However, SEG0 to SEG31 are also used as P50 to P57, P62 to P67, P70 to P77 and P80, P94, and PA0 to PA7.

*20 Summation of 3 resistors among V_{LC1} and V_{LC2} , V_{LC2} and V_{LC3} , V_{LC3} and V_{SS}

1.5.4 A/D Converter Characteristics *21

D. A/D Converter Characteristics *21

$V_{DD50}=5.0\text{ V}$ $V_{SS}=0\text{ V}$

$T_a = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
D1	Resolution				10	Bits
D2	Non-linearity error 1	$V_{DD50}=5.0\text{ V}$, $V_{SS}=0\text{ V}$ $V_{ref+}=5.0\text{ V}$ $T_{AD}=800\text{ ns}$			± 3	LSB
D3	Differential linearity error 1				± 3	
D4	Zero transition voltage	$V_{DD50}=5.0\text{ V}$, $V_{SS}=0\text{ V}$ $V_{ref+}=5.0\text{ V}$ $T_{AD}=800\text{ ns}$		10	30	mV
D5	Full-scale transition voltage		4970	4990		
D6	A/D conversion time	$T_{AD}=800\text{ ns}$	12.93			μs
D7		$f_x=32.768\text{ kHz}$, $T_{AD}=15.26\text{ }\mu\text{s}$	427.25			
D8		$T_{AD}=800\text{ ns}$	1.6			
D9	Sampling time	$f_x=32.768\text{ kHz}$, $T_{AD}=15.26\text{ }\mu\text{s}$	30.52			
D10	Reference voltage	V_{ref+}	1.8		V_{DD50}	V
D11	Analog input voltage		V_{SS}		V_{ref+}	
D12	Analog input leakage current	Channel OFF $V_{ADIN}=V_{SS}$ to V_{DD50}			± 2	μA
D13	Reference voltage pin input leakage current	Ladder resistor OFF $V_{SS} \leq V_{ref+} \leq V_{DD50}$			± 5	
D14	Ladder resistance	R_{LADD} $V_{DD50}=5.0\text{ V}$	15	40	80	$\text{k}\Omega$

*21 T_{AD} is A/D conversion clock cycle.

The values of E2 to E5 are guaranteed on the condition of $V_{DD50}=V_{ref+}=5\text{ V}$, $V_{SS}=0\text{ V}$.

1.5.5 Auto Reset Characteristics

E. Auto Reset Characteristics

$V_{DD50}=V_{RST}$ to 5.5 V $V_{SS}=0$ V
 $T_a = -40$ °C to $+85$ °C

Parameter	Symbol	Conditions	Rating			Unit	
			MIN	TYP	MAX		
Power supply voltage							
E1	Operating supply voltage	V_{DD9}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
E2	Power detection level	V_{RST1}	At rising	2.90	3.20	3.45	V
E3	Power detection level	V_{RST2}	At falling	2.70	2.90	3.10	V
E4	Supply voltage change rate	$\Delta t1/\Delta V$		2			ms/V
E5	Supply voltage change rate	$\Delta t2/\Delta V$	When 0.1 μ F capacity is connected to NRST pin.	0.2			ms/V
Consumption current							
E6	Auto reset power consumption	I_{DD15}	$V_{DD50}=5$ V (at not detection)		3	5	μ A
E7	Auto reset power consumption	I_{DD16}	$V_{DD50}=1.9$ V (at detection)		5		

1.5.6 Power Supply Voltage Detection Circuit

$V_{DD50} = 1.8 \text{ V to } 5.5 \text{ V}$ $V_{SS} = 0 \text{ V}$
 $T_a = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

Power supply voltage

F1	Power supply detection level 1-1	V_{LVI11}	At rising	3.8	4.0	4.2	V
F2	Power supply detection level 1-2	V_{LVI12}	At falling	3.7	3.9	4.1	
F3	Power supply detection level 2-1	V_{LVI21}	At rising	3.6	3.8	4.0	
F4	Power supply detection level 2-2	V_{LVI22}	At falling	3.5	3.7	3.9	
F5	Power supply detection level 3-1	V_{LVI31}	At rising	3.4	3.6	3.8	
F6	Power supply detection level 3-2	V_{LVI32}	At falling	3.3	3.5	3.7	
F7	Power supply detection level 4-1	V_{LVI41}	At rising	3.2	3.4	3.6	
F8	Power supply detection level 4-2	V_{LVI42}	At falling	3.1	3.3	3.5	
F9	Power supply detection level 5-1	V_{LVI51}	At rising	3.0	3.2	3.4	
F10	Power supply detection level 5-2	V_{LVI52}	At falling	2.9	3.1	3.3	
F11	Power supply detection level 6-1	V_{LVI61}	At rising	2.8	3.0	3.2	
F12	Power supply detection level 6-2	V_{LVI62}	At falling	2.7	2.9	3.1	
F13	Power supply detection level 7-1	V_{LVI71}	At rising	2.7	2.8	2.9	
F14	Power supply detection level 7-2	V_{LVI72}	At falling	2.6	2.7	2.8	
F15	Power supply detection level 8-1	V_{LVI81}	At rising	2.5	2.6	2.7	
F16	Power supply detection level 8-2	V_{LVI82}	At falling	2.4	2.5	2.6	
F17	Power supply detection level 9-1	V_{LVI91}	At rising	2.3	2.4	2.5	
F18	Power supply detection level 9-2	V_{LVI92}	At falling	2.2	2.3	2.4	
F19	Power supply detection level 10-1	V_{LVI101}	At rising	2.1	2.2	2.3	
F20	Power supply detection level 10-2	V_{LVI102}	At falling	2.0	2.1	2.2	

F21	Minimum pulse width	T_W		20	60		μs
F22	Supply voltage change rate	$\Delta t / \Delta V$		2			ms/V

Consumption current

F23	Consumption current in power supply detection circuit	I_{DD17}	$V_{DD50}=5.0 \text{ V}$ (at not detection)		4	6	μA
F24	Consumption current in power supply detection circuit	I_{DD18}	$V_{DD50}=4.0 \text{ V}$ (at detection)		20		

1.5.7 Internal Oscillation Circuit

G. Internal High-speed Oscillation Circuit

$V_{DD50} = 2.0\text{ V to }5.5\text{ V}$ $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
G1	frc20	Ta=-40 °C to +85 °C		20		MHz
G2	frc16			16		
G3	frc1	Ta=25 °C	-1.0		1.0	%
G4	frc2	Ta=-40 °C to +85 °C (General products)	-1.6		1.6	
G5	frc3	Ta=-40 °C to +85 °C (In-vehicle products)	-1.8		1.8	

H. Internal Low-speed Oscillation Circuit

$V_{DD50} = 1.8\text{ V to }5.5\text{ V}$ $V_{SS} = 0\text{ V}$
Ta=-40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
H1	frcs		27	30	33	kHz

1.5.8 Flash EEPROM Program Conditions

I. Flash EEPROM Program Conditions

$V_{DD50} = 0 \text{ V to } 5.5 \text{ V}$ $V_{SS} = 0 \text{ V}$
 $T_a = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
I1	Data retention period	Guaranteed programming times 1000 times (General products) *22	10			Year
I2		Guaranteed programming times 100 times (In-vehicle products) *22	15			Year

*22 The range of power supply voltage is $V_{DD50} = 2.7 \text{ V to } 5.5 \text{ V}$ at programming.

1.6 Package Dimension

■ Package code: TQFP064-P-1010D Unit: mm

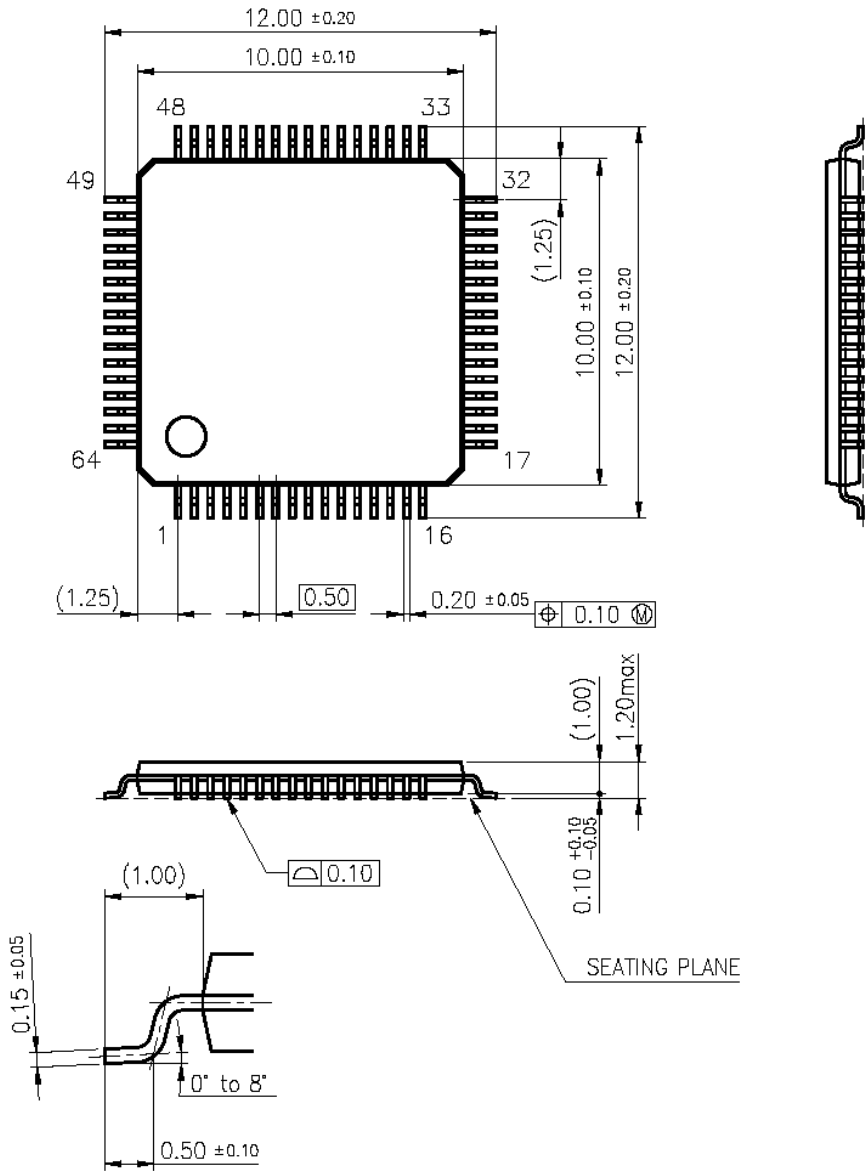


Figure:1.6.1 64 Pin TQFP Package Dimension



This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

- Package code: LQFP064-P-1414 Unit: mm

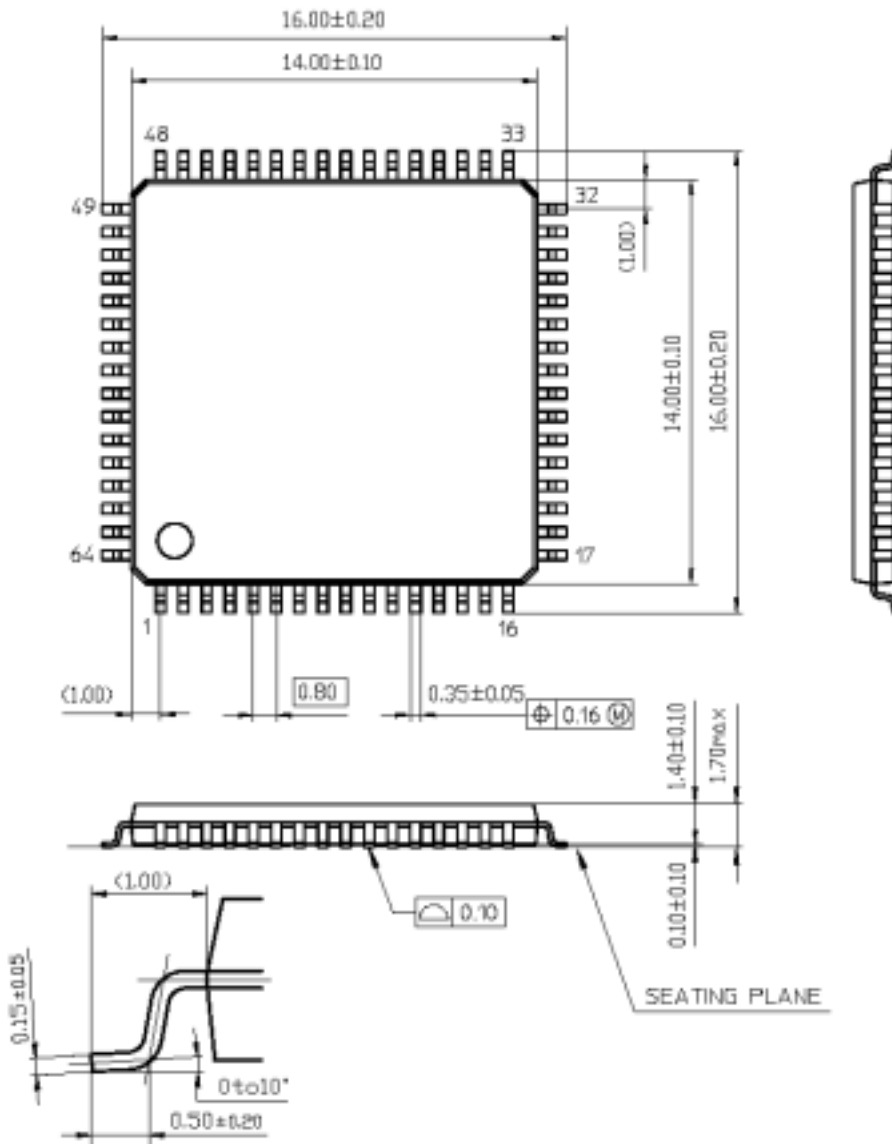


Figure:1.6.2 64 Pin LQFP Package Dimension



This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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