Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

1.1 Overview

1.1.1 Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for automotive power window, camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EFC2A has an internal 32 KB of ROM and 1 KB of RAM. Peripheral functions include 4 external interrupts, 18 internal interrupts including NMI, 8 timer counters, 2 types of serial interfaces, A/D converter, 2 types of watchdog timer. The system configuration is suitable for system control microcontroller such as camera, timer selector for VCR, CD player, or minicomponent.

With 5 oscillation systems (high-speed (internal frequency: 20 MHz), high-speed (crystal/ceramic frequency: max. 10 MHz) / low-speed (internal frequency: 30 kHz), low-speed (crystal/ceramic frequency: 32.768 kHz) and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode), or to low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has the normal mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in the normal mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

1.1.2 Product Summary

This manual describes the following model.

Table:1.1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Package
MN101EFC2 Series	32 KB	1 KB	Flash EEPROM version	TQFP032-P-0707B

Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.
When using In-circuit Emulator version, connect pull-up resistor to DMOD on the target board.

1.2 Hardware Functions

■ Feature

- ROM capacity: 32 KB

- RAM capacity: 1 KB

- Package:
  32-Pin TQFP (7 mm x 7 mm / 0.8mm pitch/ Halogen free *)

* Panasonic's "halogen free" semiconductor products refer to the products made of molding resin and interposer which conform to the following standards.
  - Bromine : 900 ppm (Maximum Concentration Value)
  - Chlorine : 900 ppm (Maximum Concentration Value)
  - Bromine + Chlorine: 1500 ppm (Maximum Concentration Value)
  The above-mentioned standards are based on the numerical value described in IEC61249-2-21.
  Antimony and its compounds are not added intentionally.

- Machine Cycle:

  High-speed mode

  0.05 µs / 20 MHz (2.7 V to 5.5 V)

  0.125 µs / 8 MHz (1.8 V to 5.5 V)

  Low-speed mode

  62.5 µs / 32 kHz (1.8 V to 5.5 V)

- Clock Gear Circuit:

  Internal system clock speed is changeable by selecting division ratio of oscillation clock.
  (Divided by 1, 2, 4, 16, 32, 64, 128)

- High-speed Clock (fpll-div) Gear Circuit for peripheral functions:

  Can be selected among "stop", fpll/1, fpll/2, fpll/4, fpll/8, and fpll/16.

- Oscillation Circuit: 4 types

  High-speed (Internal oscillation: frc), High-speed (crystal/ceramic: fosc),

  Low-speed (Internal oscillation: frcs), Low-speed (crystal/ceramic: fx)

  High-speed internal oscillation 20 MHz / 16 MHz (selectable)

  Low-speed internal oscillation 30 kHz

- Clock Multiplication Circuit:

  PLL circuit output clock (fpll) fosc multiplied by 2, 3, 4, 5, 6, 8, 10,

  1/2xfrc multiplied by 4, 5 enabled

* When clock multiplication circuit is not used, fpll = fosc or fpll = frc

- Operation Mode

NORMAL mode (high-speed mode)

PLL mode

SLOW mode (low-speed mode)

HALT mode

STOP mode

and operation clock switching

- Operating Voltage: 1.8 V to 5.5 V

- Operation ambient temperature: -40 °C to +85 °C

- interrupt: 22 sets

<Overrun interrupt>

- Non-maskable interrupt (NMI)

<Timer interrupt>

- Timer 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 6 interrupt
- Time-base interrupt
- Timer 7 interrupt
- Timer 7 compare register 2 match interrupt
- Timer 9 overflow interrupt
- Timer 9 underflow interrupt
- Timer 9 compare register 2 match interrupt

<Serial interrupt>

- LIN interrupt
- Serial 0 interrupt
- Serial 0 UART reception interrupt
- Serial 4 interrupt
- Serial 4 stop condition interrupt

<A/D interrupt>

- A/D conversion interrupt

<Low voltage detection interrupt>

- Low voltage detection interrupt

<External interrupt>

- IRQ0 : Edge selection, noise filter connectable
- IRQ1 : Edge selection, noise filter connectable
- IRQ2 : Edge selection, noise filter connectable, both edge interrupt
- IRQ3 : Edge selection, noise filter connectable, both edge interrupt
- IRQ4 : noise filter connectable, key scan interrupt

- Timer Counter x 8 sets
  - General-purpose 8-bit timer x 3 sets
  - General-purpose 16-bit timer x 1 sets
  - Motor control 16-bit timer x 1 set
  - 8-bit free-run timer x 1 set
  - Time-base timer x 1 set
  - Baud rate timer x 1 set

Timer 0 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), added pulse (2bit) type PWM output can be output to large current pin TM0IOB, event count, remote control carrier, simple pulse width measurement
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
  fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 1 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output) can be output to large current pin TM1IOB, event count, 16-bit cascade connection (connected with timer 0)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
  fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 2 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), added pulse (2bit) type PWM output can be output to large current pin TM2IOB, event count, simple pulse width measurement,
  24-bit cascade connection (connected with timer 0, 1)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
  fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 6 (8-bit free-run timer, time-base timer)

8-bit free-run timer

- Clock source
  fpll-div, fpll-div/2^{12}, fpll-div/2^{13}, fs, fslow, fslow/2^{12}, fslow/2^{13}

Time-base timer

- Interrupt generation cycle
  fpll-div/2^{7}, fpll-div/2^{8}, fpll-div/2^{9}, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15},
  fslow/2^{7}, fslow/2^{8}, fslow/2^{9}, fslow/2^{10}, fslow/2^{13}, fslow/2^{15}

Timer 7 (General-purpose 16-bit timer)

- Clock source
fpll-div, fs, external clock, timer A output,
timer 6 compare match cycle divided by 1, 2, 4, 16,
external clock, timer A output divided by 1, 2, 4, 16

- Timer function
Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM7IOB, event count, input capture function (both edges operable)

Timer 9 (Motor control 16-bit timer)

- Clock source
fpll-div, fs, external clock, Timer A output divided by 1, 2, 4, 16

- Timer function
Square wave output (Timer pulse output), complementary 3-phase PWM output can be output to large current pin TM9OD0 to 5
Triangle wave and saw tooth wave are supported, dead time insertion available, event count

- Pin output control
PWM output control is possible by external interrupt 0 to 4 (IRQ 0 to 4).
("Hi-z", output data fixed)

Timer A (baud rate timer)

Clock output for peripheral functions

- Clock source
fpll-div divided by 1, 2, 4, 8, 16, 32, and fs divided by 2, 4

- Watchdog timer

- Software processing error detection cycle is selectable from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$

- System reset is generated by the hardware when software processing error is detected twice

- Watchdog timer2

- Software processing error detection cycle is selectable from $frcs/2^4$, $frcs/2^5$, $frcs/2^6$, $frcs/2^7$, $frcs/2^8$, $frcs/2^9$, $frcs/2^{10}$, $frcs/2^{11}$, $frcs/2^{12}$, $frcs/2^{13}$, $frcs/2^{14}$, $frcs/2^{15}$

- System reset is generated by the hardware when software processing error is detected twice

- Remote control carrier output

- Remote control carrier of 1/2 or 1/3 duty cycle can be output based on timer 0

- A/D converter 10 bit x 8 channels (MN101EFC2 Series)

- Serial Interface: 3 systems

Serial 0 (Hardware LIN/Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
  Timer 0 to 2, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits are selectable.
- Continuous transmission, continuous reception, continuous transmission/reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 2, or timer A)

- Parity check, overrun error/framing error are detected
- Transfer bits of 7 to 8 are selectable
- Hardware LIN
  Synch Break generation, Wake-up detection, Synch Break detection,
  Synch Field measurement are available

Serial 4 (Multi master IIC / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4,
  Timer 0 to 2, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits are selectable.
- Continuous transmission, continuous reception, continuous transmission/reception are available.

Multi master IIC

- 7-bit slave address is settable
- General call communication mode is supported

- Auto reset circuit

- Power supply voltage detection circuit

- LED driver: 8 sets

- Ports

I/O ports	24 pins
Serial interface dual ports	9 pins
Timer I/O dual ports	9 pins
A/D input dual ports	8 pins
External interrupt dual ports	4 pins
LED (large current) driver dual ports	8 pins
High/Low-speed oscillation	2 pins
Special function pins	8 pins
Operating mode control input pins	3 pins
Reset input dual pin	1 pin
Analog reference voltage input pin	1 pin
Power supply pins	3 pins

1.3 Pin Description

1.3.1 Pin configuration

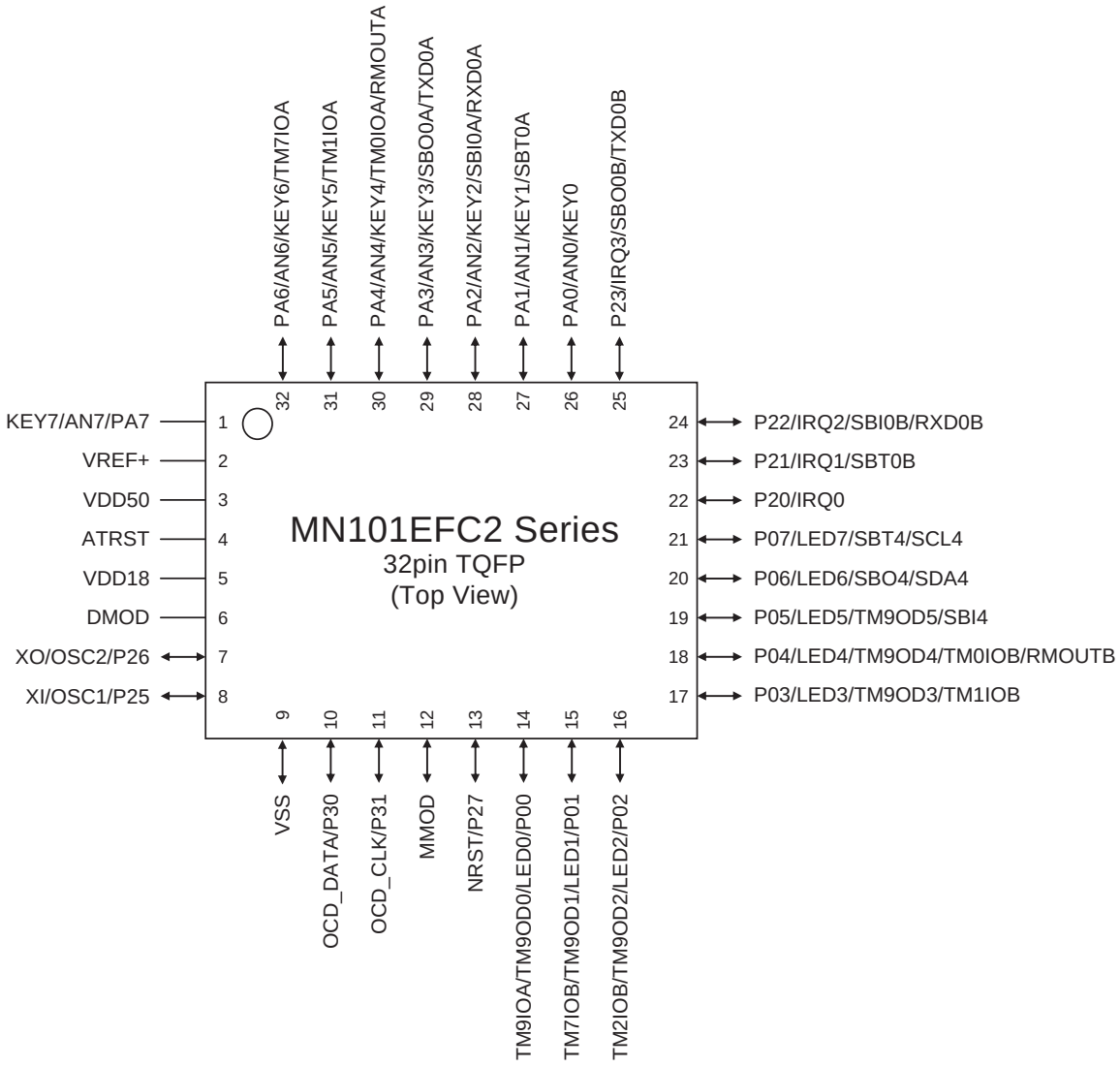

Figure:1.3.1 Pin Configuration

1.3.2 Pin Specification

Table remarks O: With function -: Without function

Pins	MN101 EFC2 Series 32pin TQFP	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P00	O	LED0	TM9IOA	in/out	P0DIR0	P0PLU0	LED0:LED driving pin 0	TM9IOA:Timer 9 in/output
	O	TM9OD0					TM9OD0:Timer 9 output	
P01	O	LED1	TM7IOB	in/out	P0DIR1	P0PLU1	LED1:LED driving pin 1	TM7IOB:Timer 7 in/output
	O	TM9OD1					TM9OD1:Timer 9 output	
P02	O	LED2	TM2IOB	in/out	P0DIR2	P0PLU2	LED2:LED driving pin 2	TM2IOB:Timer 2 in/output
	O	TM9OD2					TM9OD2:Timer 9 output	
P03	O	LED3	TM1IOB	in/out	P0DIR3	P0PLU3	LED3:LED driving pin 3	TM1IOB:Timer 1 in/output
	O	TM9OD3					TM9OD3:Timer 9 output	
P04	O	LED4	TM0IOB	in/out	P0DIR4	P0PLU4	LED4:LED driving pin 4	TM0IOB:Timer 0 in/output
	O	TM9OD4	RMOUTB				TM9OD4:Timer 9 output	RMOUTB:Remote control carrier output
P05	O	LED5	SBI4	in/out	P0DIR5	P0PLU5	LED5:LED driving pin 5	SBI4:Srial 4 data input
	O	TM9OD5					TM9OD5:Timer 9 output	
P06	O	LED6	SBO4	in/out	P0DIR6	P0PLU6	LED6:LED driving pin 6	SBO4:Srial 4 data in/output
	O	SDA4					SDA4:Multi-master IIC4 data in/output	
P07	O	LED7	SBT4	in/out	P0DIR7	P0PLU7	LED7:LED driving pin 7	SBT4:Srial 4 clock in/output
	O	SCL4					SCL4:Multi-master IIC4 clock in/output	
P20	O	IRQ0		in/out	P2DIR0	P2PLU0	IRQ0:External interrupt 0	
P21	O	IRQ1	SBT0B	in/out	P2DIR1	P2PLU1	IRQ1:External interrupt 1	SBT0B:Srial 0 clock in/output
P22	O	IRQ2	SBI0B	in/out	P2DIR2	P2PLU2	IRQ2:External interrupt 2	SBI0B:Srial 0 data input
	O	RXD0B					RXD0B:UART0 data input	
P23	O	IRQ3	SBO0B	in/out	P2DIR3	P2PLU3	IRQ3:External interrupt 3	SBO0B:Srial 0 data in/output
	O	TXD0B					TXD0B:UART0 data in/output	
P24	-	IRQ4		in/out	P2DIR4	P2PLU4	IRQ4:External interrupt 4	
P25	O	OSC1	XI	in/out	P2DIR5	P2PLU5	OSC1:Seramic/crystal high-speed clock input	XI:Seramic/crystal low-speed clock input
P26	O	OSC2	XO	in/out	P2DIR6	P2PLU6	OSC2:Seramic/crystal high-speed clock output	XO:Seramic/crystal low-speed clock output
P27	O	NRST		in/out	-	-	NRST:Reset	
P30	O	OCD_DATA		in/out	P3DIR0	P3PLU0	OCD_DATA:On-board programmer data pin	
P31	O	OCD_CLK		in/out	P3DIR1	P3PLU1	OCD_CLK:On-board programmer clock supply pin	
P32	-	BUZZER		in/out	P3DIR2	P3PLU2	BUZZER:Buzzer output	
P33	-	NBUZZER		in/out	P3DIR3	P3PLU3	NBUZZER:Buzzer reverse output	
P34	-	SBO1	TXD1	in/out	P3DIR4	P3PLU4	SBO1:Srial 1 data in/output	TXD1:UART1 data in/output
P35	-	TM2IOA	SBI1	in/out	P3DIR5	P3PLU5	TM2IOA:Timer 2 in/output	SBI1:Srial 1 data input
	-	RXD1					RXD1:UART1 data input	
P36	-	SBT1		in/out	P3DIR6	P3PLU6	SBT1:Srial 1 clock in/output	
P40	-	TM0IOC	RMOUTC	in/out	P4DIR0	P4PLUD0	TM0IOC:Timer 0 in/output	RMOUTC:Remote control carrier output
P41	-	TM1IOC		in/out	P4DIR1	P4PLUD1	TM1IOC:Timer 1 in/output	
P42	-	AN11	TM2IOC	in/out	P4DIR2	P4PLUD2	AN11:Analog 11 input	TM2IOC:Timer 2 in/output
P43	-	AN10	TM7IOC	in/out	P4DIR3	P4PLUD3	AN10:Analog 10 input	TM7IOC:Timer 7 in/output
P44	-	AN9	TM9IOC	in/out	P4DIR4	P4PLUD4	AN9:Analog 9 input	TM9IOC:Timer 9 in/output
P45	-	AN8		in/out	P4DIR5	P4PLUD5	AN8:Analog 8 input	
PA0	O	AN0	KEY0	in/out	PADIR0	PAPLU0	AN0:Analog 0 input	KEY0:Key interrupt 0
PA1	O	AN1	KEY1	in/out	PADIR1	PAPLU1	AN1:Analog 1 input	KEY1:Key interrupt 1
	O	SBT0A					SBT0A:Srial 0 clock in/output	
PA2	O	AN2	KEY2	in/out	PADIR2	PAPLU2	AN2:Analog 2 input	KEY2:Key interrupt 2
	O	SBI0A	RXD0A				SBI0A:Srial 0 data input	RXD0A:UART0 data input

Table remarks O: With function -: Without function

Pins	MN101 EFC2 Series 32pin TQFP	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
PA3	O	AN3	KEY3	in/out	PADIR3	PAPLU3	AN3:Analog 3 input	KEY3:Key interrupt 3
	O	SBO0A	TXD0A				SBO0A:Srial 0 data in/output	TXD0A:UART0 data in/output
PA4	O	AN4	KEY4	in/out	PADIR4	PAPLU4	AN4:Analog 4 input	KEY4:Key interrupt 4
	O	TM0IOA	RMOUTA				TM0IOA:Timer 0 in/output	RMOUTA:Remote control carrier output
PA5	O	AN5	KEY5	in/out	PADIR5	PAPLU5	AN5:Analog 5 input	KEY5:Key interrupt 5
	O	TM1IOA					TM1IOA:Timer 1 in/output	
PA6	O	AN6	KEY6	in/out	PADIR6	PAPLU6	AN6:Analog 6 input	KEY6:Key interrupt 6
	O	TM7IOA					TM7IOA:Timer 7 in/output	
PA7	O	AN7	KEY7	in/out	PADIR7	PAPLU7	AN7:Analog 7 input	KEY7:Key interrupt 7

1.3.3 Pin Functions

Table remarks -: Without function

Pins	MN101EFC2 Series 32pin TQFP	I/O	Other Function	Function	Description
VDD50	3	-		Power connect pins	Apply 1.8 V to 5.5 V to VDD50 and 0 V to VSS connect 0.1 μF + 1 μF or larger bypass capacitor for internal power stabilization.
VSS	9	-			
VDD18	5	-		Internal power output pin	This pin is output 1.8 V from internal power circuit. Don't use the power supply to external device. For internal power circuit output stability, connect at least 0.1 μF + 1 μF one bypass capacitor between VDD18 and VSS.
OSC1	8	Input	P25,XI	High speed operation clock input pin	Connect these oscillation pins to ceramic or crystal ocsillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
OSC2	7	Output	P26,XO	High speed operation clock output pin	
XI	8	Input	P25,OSC1	Low speed operation clock input pin	Connect these oscillation pins to crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. the chip will not operate with an external clock when using the STOP mode.
XO	7	Output	P26,OSC2	Low speed operation clock output pin	
NRST	13	I/O	P27	Reset pins [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and VDD50.
ATRST	4	Input		Auto reset setting pin	Input "H" to enable auto reset function and "L" to disable this function
P00 P01 P02 P03 P04 P05 P06 P07	14 15 16 17 18 19 20 21	I/O	LED0,TM9IOA,TM9OD0 LED1,TM7IOB,TM9OD1 LED2,TM2IOB,TM9OD2 LED3,TM1IOB,TM9OD3 LED4,TM0IOB,RMOUTB, TM9OD4 LED5,SBI4,TM9OD5 LED6,SBO4,SDA4 LED7,SBT4,SCL4	I/O port 0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. Direct LED drive is available at output. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P20 P21 P22 P23 P24 P25 P26	22 23 24 25 - 8 7	I/O	IRQ0 IRQ1,SBT0B IRQ2,SBI0B,RXD0B IRQ3,SBO0B,TXD0B IRQ4 OSC1,XI OSC2,XO	I/O port 2	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance)
P27	13	Input	NRST	Input port 2	Port P27 has an N-channel open-drain configuration.

Table remarks -: Without function

Pins	MN101EFC2 Series 32pin TQFP	I/O	Other Function	Function	Description
P30 P31 P32 P33 P34 P35 P36	10 11 - - - - -	I/O	OCD_DATA OCD_CLK BUZZER NBUZZER SBO1,TXD1 TM2IOA,SBI1,RXD1 SBT1	I/O port 3	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance)
P40 P41 P42 P43 P44 P45	- - - - - -	I/O	TM0IOC,RMOUTC TM1IOC AN11,TM2IOC AN10,TM7IOC AN9,TM9IOC AN8	I/O port 4	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P4PLUD register. A pull-up/down resistor connection for each port can be selected individually in the SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistor is disabled (high impedance) P40 denotes N.C. for QFN package.
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	26 27 28 29 30 31 32 1	I/O	AN0,KEY0 AN1,KEY1,SBT0A AN2,KEY2,SBI0A,RXD0A AN3,KEY3,SBO0A,TXD0A AN4,KEY4,TM0IOA,RMOUTA AN5,KEY5,TM1IOA AN6,KEY6,TM7IOA AN7,KEY7	I/O port A	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up resistor for each bit can be selected individually by the PAPLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance)
SBO0A SBO0B SBO1 SBO4	29 25 - 20	Output	PA3,AN3,KEY3,TXD0A P23,IRQ3,TXD0B P34,TXD1 P06,LED6,SDA4	Serial interface transmission data output pins	Transmission data output pins for serial interface 0,1,4. The output configuration, either COMS push-pull or n-channel open-drain can be selected in the P0ODC, P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected in the P0PLU, P2PLU, P3PLU and PAPLU registers. Select the output mode in the P0DIR, P2DIR, P3DIR and PADIR registers and set serial data output mode in serial mode register 1 (SC0MD1, SC1MD1, SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0A SBI0B SBI1 SBI4	28 24 - 19	Input	PA2,AN2,KEY2,RXD0A P22,IRQ2,RXD0B P35,TM2IOA,RXD1 P05,LED5,TM9OD5	Serial interface reception data output pins	Reception data input pins for serial interface 0,1,4. Pull-up resistor can be selected in the P0PLU, P2PLU, P3PLUand PAPLU registers. Select the output mode in the P0DIR, P2DIR, P3DIR and PADIR registers and select serial data input mode in serial mode register 1 (SC0MD1, SC1MD1, SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBT0A SBT0B SBT1 SBT4	27 23 - 21	I/O	PA1,AN1,KEY1 P21,IRQ1,SBT0B P36 P07,LED7,SCL4	Serial interface Clock I/O pins	Clock I/O pins for serial interface 0,1,4. The output configuration, either COMS push-pull or n-channel open-drain can be selected in the P0ODC, P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected in the P0PLU, P2PLU, P3PLU and PAPLU registers. Select clock I/O in the P0DIR, P2DIR, P3DIR and PADIR registers and serial mode register 1 (SC0MD1, SC1MD1, SC4MD1) with the communication mode. These can be used as normal I/O pins when the serial interface is not used.

Table remarks -: Without function

Pins	MN101EFC2 Series 32pin TQFP	I/O	Other Function	Function	Description
TXD0A TXD0B TXD1	29 25 -	Output	PA3,AN3,KEY3,SBO0A P23,IRQ3,SBO0B P34,SBO1	UART transmission data output pins	In the serial interface0,1 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either COMS push-pull or n-channel open-drain can be selected in the P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected by the P2PLU, P3PLU and PAPLU registers. Select the output mode in the P2DIR, P3DIR and PADIR registers and select serial data output mode in serial mode register 1 (SC0MD1, SC1MD1). These can be used as normal I/O pins when the serial interface is not used.
RXD0A RXD0B RXD1	28 24 -	Input	PA2,AN2,KEY2,SBI0A P22,IRQ2,SBI0B P35,TM2IOA,SBI1	UART reception data output pins	In the serial interface0,1 in UART mode, this pin is configured as the reception data input pin. Pull-up resistor can be selected in the P2PLU, P3PLU and PAPLU registers. Select the input mode in the P2DIR, P3DIR and PADIR registers and select serial input in serial mode register 1 (SC0MD1, SC1MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA4	20	I/O	P06,LED6,SBO4	IIC data I/O pins	In the serial interface4 in IIC mode, this pin is configured as the data I/O pin. For the output configuration, select n-channel open-drain in the P0ODC registers and set pull-up resistor in the P0PLU registers. Select the output mode in the P0DIR register and select serial data I/O mode by serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SCL4	21	I/O	P07,LED7,SBT4	IIC clock I/O pins	In the serial interface4 in IIC mode, this pin is configured as the clock I/O pin. For the output configuration, select n-channel open-drain in the P0ODC register and set pull-up resistor by the P0PLU register. Select the output mode at the P0DIR register and select clock I/O mode in serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used
TM0IOA TM0IOB TM0IOC TM1IOA TM1IOB TM1IOC TM2IOA TM2IOB TM2IOC	30 18 - 31 17 - - 16 -	I/O	PA4,AN4,KEY4,RMOUTA P04,LED4,RMOUTB,TM9OD4 P40,RMOUTC PA5,AN5,KEY5 P03,LED3,TM9OD3 P41 P35,SBI1,RXD1 P02,LED2,TM9OD2 P42,AN11	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 2. To use this pin as event clock input, configure it as input by P0DIR register, P3DIR register, P4DIR register and PADIR register. In the input mode, pull-up resistor can be selected in the P0PLU register, P3PLU register, P4PLU register and PAPLU register. For timer output, PWM signal output, select the special function pin in port 0 output mode register, port 3 output mode register, port 4 output mode register and port A output mode register (P0OMD, P3OMD, P4OMD and PAOMD), and set to the output mode in P0DIR register, P3DIR register, P4DIR register and PADIR register. These can be used as normal I/O pins when the Timer I/O pin is not used. TM0IOC denotes N.C. for QFN package.
RMOUTA RMOUTB RMOUTC	30 18 -	Output	PA4,AN4,KEY4,TM0IOA P04,LED4,TM0IOB,TM9OD4 P40,TM0IOC	Remote control transmission signal output pins	Output pin for remote control transmission with a carrier signal. For remote control carrier output, select the special function pin by the port 0 output mode register, port 4 output mode register and port A output mode register (P0OMD, P4OMD and PAOMD), and set the P0DIR register, P1DIR register, P6DIR register and PADIR register to the output mode. At the same time, select remote control carrier output in remote control carrier control register (RMCTR). These can be used as normal I/O pins when the remote control is not used. RMOUTC denotes N.C. for QFN package.

Table remarks -: Without function

Pins	MN101EFC2 Series 32pin TQFP	I/O	Other Function	Function	Description
BUZZER NBUZZER	- -	Output	P32 P33	Buzzer output pins	Piezoelectric buzzer driving pin. Buzzer output is available to port3. The driving frequency can be set in the DLYCTR register. In order to select buzzer output to port 3, select the special function pin in the port 3 output mode register (PA3MD), and set the P3DIR register to the output mode. At the same time, select buzzer output in the oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when the serial interface is not used.
TM7IOA TM7IOB TM7IOC TM9IOA TM9IOC	32 15 - 14 -	I/O	PA6,AN6,KEY6 P01,LED1,TM9OD1 P43,AN10 P00,LED0,TM9OD0 P44,AN9	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7 and 9. To use this pin as event clock input, configure it as input with the P0DIR register, P4DIR register, PADIR register. In the input mode, pull-up resistor can be selected by P0PLU register, P4PLU register and PAPLU register. For timer output, PWM signal output, select the special function pin in the port 0 output mode register, port 4 output mode register and port A output mode register, and set to the output mode in P0DIR register, P4DIR register and PADIR register. These can be used as normal I/O pins when not used as timer I/O pins.
TM9OD0 TM9OD1 TM9OD2 TM9OD3 TM9OD4 TM9OD5	14 15 16 17 18 19	Output	P00,LED0,TM9IOA P01,LED1,TM7IOB P02,LED2,TM2IOB P03,LED3,TM1IOB P04,LED4,TM0IOB,RMOUTB P05,LED5,SBI4	Timer PWM output	PWM signal output pin for 16-bit timer 9. Select the special function pin in the port 0 output mode register, and set to the output mode in P0DIR register,. These can be used as normal I/O pins when not used as timer I/O pins.
VREF+	2	-		A/D reference voltage input pin	Reference power supply pin for the A/D converter. Normally, the values of $V_{REF+} = V_{DD50}$ is used.
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7 AN8 AN9 AN10 AN11	26 27 28 29 30 31 32 1 - - - -	Input	PA0,KEY0 PA1,KEY1,SBT0A PA2,KEY2,SBI0A,RXD0A PA3,KEY3,SBO0A,TXD0A PA4,KEY4,TM0IOA,RMOUTA PA5,KEY5,TM1IOA PA6,KEY6,TM7IOA PA7,KEY7 P45 P44,TM9IOC P43,TM7IOC P42,TM2IOC	Analog input pins	Analog input pins for an 12-channel, 10-bit A/D converter. Select the analog input by the PAIMD register. When not used for analog input, these pins can be used as normal input pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4	22 23 24 25 -	Input	P20 P21,SBT0B P22,SBI0B,RXD0B P23,SBO0B,TXD0B P24	External interrupt	External interrupt input pins. Select the external interrupt input enable by the IRQCNT register. The valid edge for IRQ0 to 4 can be selected with the IRQnICR register. IRQ2 to IRQ4 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins.

Table remarks -: Without function

Pins	MN101EFC2 Series 32pin TQFP	I/O	Other Function	Function	Description
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	26 27 28 29 30 31 32 1	Input	PA0,AN0 PA1,SBT0A,AN1 PA2,SBI0A,RXD0A,AN2 PA3,SBO0A,TXD0A,AN3 PA4,TM0IOA,RMOUTA,AN4 PA5,TM1IOA,AN5 PA6,TM7IOA,AN6 PA7,AN7	Key interrupt input pins	Input pins for key interrupt based on OR condition result of pin inputs. These can be set to key input pins by 1-bit with the key interrupt control register (KEYT3_1IMD). When not used for KEY input, these pins can be used as normal I/O pins.
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7	14 15 16 17 18 19 20 21	Output	P00,TM9IOA,TM9OD0 P01,TM7IOB,TM9OD1 P02,TM2IOB,TM9OD2 P03,TM1IOB,TM9OD3 P04,TM0IOB,RMOUTB, TM9OD4 P05,SBI4,TM9OD5 P06,SBO4,SDA4 P07,SBT4,SCL4	LED drive pins	Large current output pins. Select the large current output by the P0LED register. When not used for LED output, these pins can be used as normal I/O pins.
DMOD	6	Input		Mode switch input pins	Set always to V_{DD50} This pin contains an internal pull-up resister only flash EEPROM version
MMOD	12	Input		ROM area switch input pins at start	Set always to V_{SS}
OCD_DATA	10	I/O	P30	On-board debugger communication data I/O pin	Refer to [Chapter Internal Flash Memory] of LSI User's Manual for details.
OCD_CLK	11	Input	P31	On-board debugger communication clock input pin	Refer to [Chapter Internal Flash Memory] of LSI User's Manual for details.

Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.
When using In-circuit Emulator version, connect pull-up resistor to DMOD on the target board.

For the MMOD setup in rewriting the flash memory, refer to [Chapter Internal Flash Memory] of LSI User's Manual.

1.4 Block Diagram

1.4.1 Block Diagram

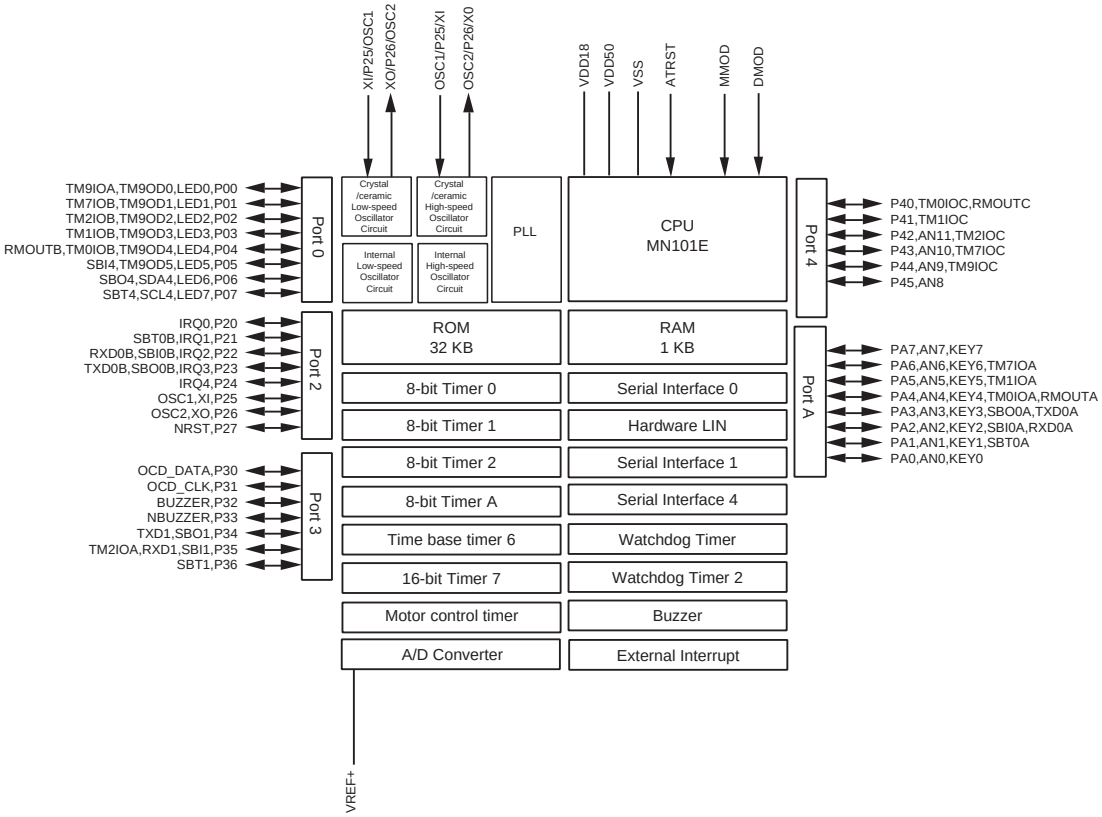

Figure:1.4.1 Block Diagram

* Varies depending on models.
  Refer to [Chapter 1 1.1.2 Product Summary] and [Chapter 1 1.3.3 Pin Functions].

1.5 Electrical Characteristics

This LSI manual describes standard specifications.

When using this LSI, consult our sales offices for the product specifications.

Structure	CMOS integrated circuit
Application	General-purpose
Function	CMOS 8-bit single chip microcomputer

1.5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *2 *3 *4 V_{SS} = 0 V

Parameter				Symbol	Rating	Unit
A1	Power supply voltage			V_{DD50A}	-0.3 to +7.0	V
A2	Power supply voltage			V_{DD18A}	-0.3 to +2.5	
A3	Input pin voltage			V_{IA}	-0.3 to V_{DD50} +0.3 (upper limit: 7.0 V)	
A4	Output pin voltage			V_{OA}	-0.3 to V_{DD50} +0.3 (upper limit: 7.0 V)	
A5	I/O pin voltage			V_{IO1A}	-0.3 to V_{DD50} +0.3 (upper limit: 7.0 V)	
A6	Peak output current	LED output		I_{OL1A} (peak)	30	mA
A7		Other than LED output		I_{OL2A} (peak)	20	
A8		All pins		I_{OHA} (peak)	-10	
A9	Average output current *1	LED output		I_{OL1A} (avg)	20	
A10		Other than LED output		I_{OL2A} (avg)	15	
A11		All pins		I_{OHA} (avg)	-5	
A14	Power dissipation	MN101EFC2 Series	32pin TQFP	P_{D3A}	400	mW
A15	Operating ambient temperature			T_{oprA}	-40 to +85	°C
A16	Storage temperature			T_{STGA}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1 μF + 1.0 μF or larger between VDD50 pin and GND for the internal power voltage stabilization.

*3 Connect appropriate capacitor about 0.1 μF + 1.0 μF between VDD18 pin and VSS pin, near the microcontroller according to the Figure:1.5.1 shown below for the internal power supply stabilization.

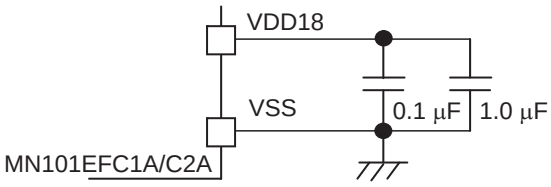

Figure:1.5.1 Capacitor Connection between VDD18 and VSS Pins

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

1.5.2 Operating Conditions

B. Operating Conditions

V_{SS}=0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *5							
B1	Power supply voltage	V_{DD1}	fs ≤ 20 MHz *7	2.7		5.5	V
B2		V_{DD2}	fs ≤ 10 MHz *8	2.7		5.5	
B3		V_{DD3}	fs ≤ 8 MHz *7	1.8		5.5	
B4		V_{DD4}	fs ≤ 8 MHz *7 When using internal oscillation *9	2.0		5.5	
B5		V_{DD5}	fs ≤ 4 MHz *8	1.8		5.5	
B6		V_{DD6}	fs ≤ 4 MHz *8 When using internal oscillation *10	2.0		5.5	
B7		V_{DD7}	fs = 16.384 kHz	1.8		5.5	
B8	RAM retention power supply voltage	V_{DD8}	During STOP mode	1.8		5.5	
Operating speed *6							
B9	Instruction execution time fs	t_{c1}	V_{DD50} = 2.7 V to 5.5 V *7	0.05			µs
B10		t_{c2}	V_{DD50} = 2.7 V to 5.5 V *8	0.10			
B11		t_{c3}	V_{DD50} = 1.8 V to 5.5 V *7	0.125			
B12		t_{c4}	V_{DD50} = 2.0 V to 5.5 V *7 When using internal oscillation *9	0.125			
B13		t_{c5}	V_{DD50} = 1.8 V to 5.5 V *8	0.25			
B14		t_{c6}	V_{DD50} = 2.0 V to 5.5 V *8 When using internal oscillation *10	0.25			
B15		t_{c7}	V_{DD50} = 1.8 V to 5.5 V	61			

*5 fs : Machine clock frequency

*6 tc1 to 6 : when the machine clock is selected from external high-speed oscillation, internal high-speed oscillation, or both the oscillations multiplied by PLL.
tc7 : when the machine clock is selected from external high-speed oscillation or internal high-speed oscillation.

*7 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b1”

*8 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b0”

*9 When setting frc=16 MHz, fs=frc/2

*10 When setting frc=16 MHz, fs=frc/4

V_{SS}=0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
External Oscillator 1 Figure:1.5.2							
B16	Frequency	f_{hosc1}	V_{DD50} is within the specified operating power supply voltage range. (Refer to the ratings of B1 to B6 for the operating supply voltage range)	2.0		10	MHz
B17	Internal feedback resistor	R_{f10}	V_{DD50} = 5.0 V		980		kΩ
External Oscillator 2 Figure:1.5.3							
B18	Frequency	f_{sosc1}	V_{DD50} = 1.8 V to 5.5 V		32.768		kHz
B19	Internal feedback resistor	R_{f20}	V_{DD50} = 5.0 V		6.2		MΩ

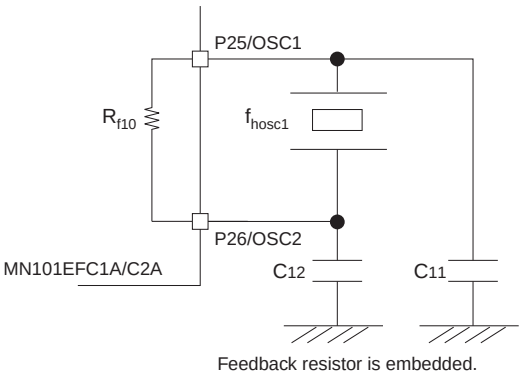

Figure:1.5.2 External Oscillator 1

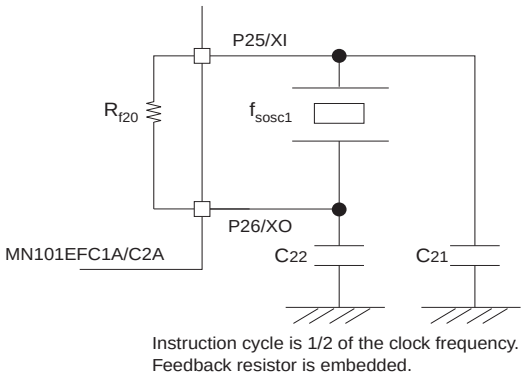

Figure:1.5.3 External Oscillator 2

Connect external capacitors suited for the used oscillator.
The reference value denotes external capacity value based on our matching result.
When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed depending on the value of capacitor. For external capacity value, please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

V_{DD50}=1.8 V to 5.5 V
V_{SS}=0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
B20	Clock frequency	f_{hosc2}		2		10.0	MHz
B21	High-level pulse width *11	t_{wh1}	Figure:1.5.4	45			ns
B22	Low-level pulse width *11	t_{wl1}		45			
B23	Rising time *12	t_{wr1}	Figure:1.5.4	0		5.0	
B24	Falling time *12	t_{wf1}		0		5.0	
External clock input 2 XI (XO is unconnected)							
B25	Clock frequency	f_{sosc2}			32.768		kHz
B26	High-level pulse width *11	t_{wh2}	Figure:1.5.5		4.5		µs
B27	Low-level pulse width *11	t_{wl2}			4.5		
B28	Rising time *12	t_{wr2}	Figure:1.5.5	0		20	ns
B29	Falling time *12	t_{wf2}		0		20	

*11 The clock duty ratio should be 45 % to 55 %

*12 Rising time and falling time differ depending on the oscillation frequency.
The max value is not a specified value but a rough value.
Please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

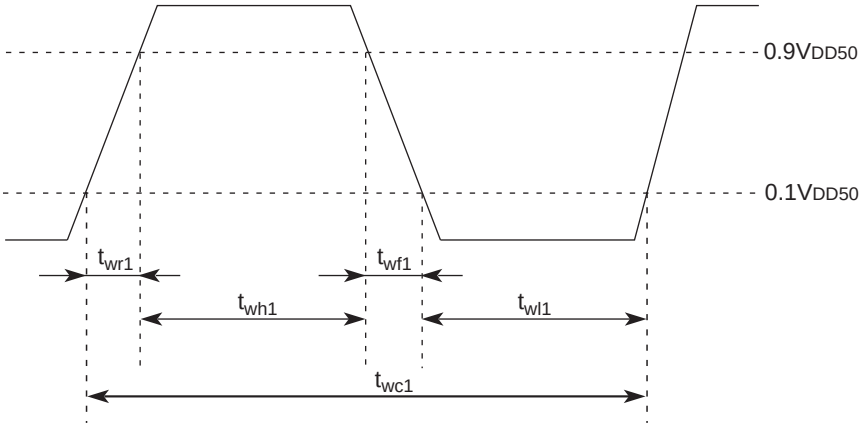

Figure:1.5.4 OSC1 Timing Chart

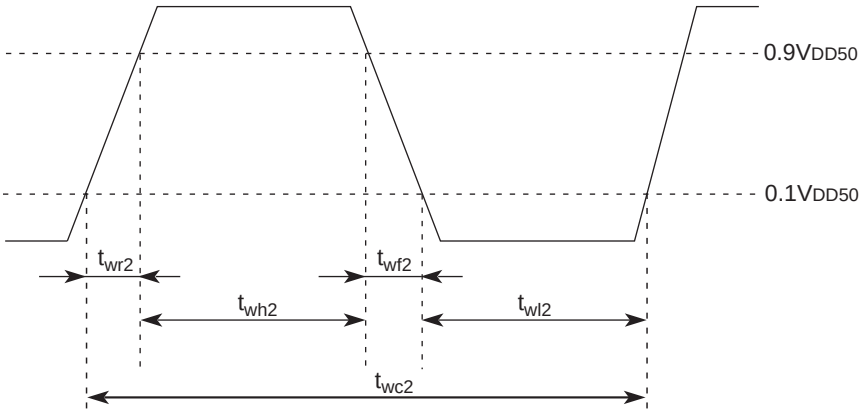

Figure:1.5.5 XI Timing Chart

1.5.3 DC Characteristics

C. DC Characteristics

V_{SS}=0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current *13							
C1	Power supply current during operation	I_{DD1}	fosc=10 MHz [Double-speed mode:fs=fosc] V_{DD50}=5 V (PLL is not used) *14		5	14	mA
C2		I_{DD2}	fosc=10 MHz [Double-speed mode:fs=fosc] V_{DD50}=3 V (PLL is not used) *14		5.5		
C3		I_{DD3}	fosc=8 MHz [Double-speed mode:fs=fosc] V_{DD50}=5 V (PLL is not used) *14		4.5	13	
C4		I_{DD4}	fosc=8 MHz [Double-speed mode:fs=fosc] V_{DD50}=3 V (PLL is not used) *14		4.5		
C5		I_{DD5}	fosc=4 MHz [Double-speed mode:fs=fosc] V_{DD50}=5 V (PLL is not used) *15		3.5	11	
C6		I_{DD6}	fosc=4 MHz [Double-speed mode:fs=fosc] V_{DD50}=3 V (PLL is not used) *15		3.5		
C7		I_{DD7}	fosc=4 MHz [Multiplied by 10:fs=20 MHz] V_{DD50}=5 V (PLL is used) *14		8	18	
C8		I_{DD8}	fosc=4 MHz [Multiplied by 10:fs=20 MHz] V_{DD50}=3 V (PLL is used) *14		9		
C9		I_{DD9}	frc=20 MHz [Double-speed mode:fs=frc] V_{DD50}=5 V (PLL is not used) *14		7.5	16	
C10		I_{DD10}	frc=20 MHz [Double-speed mode:fs=frc] V_{DD50}=3 V (PLL is not used) *14		8.5		
C11		I_{DD11}	frcs=30 kHz [fs=frcs/2] V_{DD50}=3 V Ta=25 °C ROM is executed.		50	65	µA
C12			frcs=30 kHz [fs=frcs/2] V_{DD50}=3 V Ta=85 °C ROM is executed.			150	
C13		I_{DD12}	frcs=30 kHz [fs=frcs/2] V_{DD50}=3 V Ta=25 °C RAM is executed. *16		10	25	
C14			frcs=30 kHz [fs=frcs/2] V_{DD50}=3 V Ta=85 °C RAM is executed. *16			65	
C15	Power supply current during HALT1	I_{DD13}	frcs=30 kHz, V_{DD50}=3 V Ta=25 °C		6	15	
C16			frcs=30 kHz, V_{DD50}=3 V Ta=85 °C			55	
C17	Power supply current during STOP	I_{DD14}	V_{DD50}=5 V, Ta=25 °C		1	5	
C18			V_{DD50}=5 V, Ta=85 °C			40	

*13 Measured without loading (pull-up and pull-down resistors are not connected.)

To measure the power supply current during operation IDD1 to 10:
1, set the all I/O pins to input mode,
2, set the CPU mode to <NORMAL>,
3, fix the MMOD pin at V_{SS} level and input pin at V_{DD50} level
4, and input the rectangular wave of 10 MHz (8 MHz, 4 MHz), which has amplitude of V_{DD50} and V_{SS} potential, from the OSCI1 pin.

To measure the power supply current during operation IDD11,12:
1, set the all I/O pins to input mode,
2, set the CPU mode to <SLOW>,
3, and fix the MMOD pin at V_{SS} level and input pin at V_{DD50} level.
clock is supplied from the internal low-speed oscillation circuit.

To measure the power supply current during HALT1 IDD13,
1, set the all I/O pins to input mode,
2, set the CPU mode to <HALT1>,
3, and fix the MMOD pin at V_{SS} level and input pin at V_{DD50} level.

To measure the power supply current during STOP IDD14,
1, set the CPU mode to <STOP>,
2, and fix the MMOD pin at V_{SS} level and input pin at V_{DD50} level
3, and open the OSC1 pin.

*14 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b1”

*15 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b0”

*16 When bp3 of the FEWSPD register (0x03FBF) to “1'b1”

V_{DD50}=1.8 V to 5.5 V V_{SS}=0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 ATRST, MMOD							
C19	Input high voltage	V_{IH1}		0.8V_{DD50}		V_{DD50}	V
C20	Input low voltage	V_{IL1}		0		0.2V_{DD50}	
C21	Input leakage current	I_{LK1}	V_{IN} = 0 V to V_{DD50}			± 2	µA
Input pin 2 P27/NRST							
C22	Input high voltage	V_{IH2}		0.8V_{DD50}		V_{DD50}	V
C23	Input low voltage	V_{IL2}		0		0.15V_{DD50}	
C24	Pull-up resistor	R_{RH1}	V_{DD50}=5 V, V_{IN}= V_{SS}	10	50	100	kΩ
I/O pin 3 P00 to P07							
C25	Input high voltage 2	V_{IH4}	2.7 V ≤ V_{DD50} ≤ 5.5 V	0.54V_{DD50}		V_{DD50}	V
C26	Input high voltage 1	V_{IH3}	1.8 V ≤ V_{DD50} < 2.7 V	0.8V_{DD50}		V_{DD50}	
C27	Input low voltage	V_{IL3}		0		0.2V_{DD50}	
C28	Input leakage current	I_{LK2}	V_{IN}=0 V to V_{DD50}			± 2	µA
C29	Pull-up resistor	R_{RH2}	V_{DD50}=5 V, V_{IN}= V_{SS} Pull-up resistor ON	10	50	100	kΩ
C30	Output high voltage	V_{OH1}	V_{DD50}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C31	Output low voltage 1	V_{OL1}	V_{DD50}=5.0 V, I_{OL}=1.0 mA LED output OFF			0.5	
C32	Output low voltage 2	V_{OL2}	V_{DD50}=5.0 V, IOL=15.0 mA LED output ON			1.0	

V_{DD50}=1.8 V to 5.5 V V_{SS}=0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 5 P21, P25 to P26, P30 to P31, PA0 to PA7							
C40	Input high voltage	V_{IH7}		0.8V_{DD50}		V_{DD50}	V
C41	Input low voltage	V_{IL5}		0		0.2V_{DD50}	
C42	Input leakage current	I_{LK4}	V_{IN}=0 V to V_{DD50}			± 2	μA
C43	Pull-up resistor	R_{RH4}	V_{DD50}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C44	Output high voltage	V_{OH3}	V_{DD50}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C45	Output low voltage	V_{OL4}	V_{DD50}=5.0 V, I_{OL}=1.0 mA			0.5	
Input pin 7 DMOD *17							
C53	Input high voltage	V_{IH9}		0.8V_{DD50}		V_{DD50}	V
C54	Input low voltage	V_{IL7}		0		0.2V_{DD50}	
C55	Pull-up resistor	R_{RH6}	V_{DD50}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ

*17 Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.
When using In-circuit Emulator version, connect pull-up resistor to DMOD on the target board.

1.5.4 A/D Converter Characteristics *18

D. A/D Converter Characteristics

V_{DD50}=5.0 V V_{SS}=0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	Resolution					10	Bits
D2	Non-linearity error 1		V_{DD50}=5.0 V, V_{SS}=0 V V_{REF+}=5.0 V T_{AD}=800 ns			± 3	LSB
D3	Differential non-linearity error 1					± 3	
D4	Zero transition voltage		V_{DD50}=5.0 V, V_{SS}=0 V V_{REF+}=5.0 V T_{AD}=800 ns		10	30	mV
D5	Full-scale transition voltage			4970	4990		
D6	A/D conversion time		T_{AD}=800 ns	12.93			µs
D7			f_{slow}=32.768 kHz, T_{AD}=15.26 µs	427.25			
D8	Sampling time		T_{AD}=800 ns	1.6			
D9			f_{slow}=32.768 kHz, T_{AD}=15.26 µs	30.52			
D10	Reference voltage	V_{REF+}	Note)	2.0		V_{DD50}	V
D11	Analog input voltage			V_{SS}		V_{REF+}	
D12	Analog input leakage current		Channel OFF V_{ADIN}=V_{SS} to V_{DD50}			± 2	µA
D13	Reference voltage pin input leakage current		Ladder resistance OFF $V_{SS} \leq V_{REF+} \leq V_{DD50}$			± 5	
D14	Ladder resistance	R_{LADD}	V_{DD50}=5.0 V	15	40	80	kΩ

*18 T_{AD} is A/D conversion clock cycle.
The specification values of D2 to D5 are guaranteed on the condition of V_{DD50}=V_{REF+}=5 V, V_{SS}=0 V.

Note) Whether using the A/D function, the voltage difference between VREF+ and VSS must be set to more than 2.0 V.
When VDD50 is less than 2.0 V, set the condition of V_{DD50}=V_{ref+}.

1.5.5 Auto Reset Characteristics

E. Auto Reset Characteristics

$V_{DD50}=V_{RST}$ to 5.5 V V_{SS}=0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
E1	Operating supply voltage	V_{DD7}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
E2	Power detection level	V_{RST1}	At rising	2.90	3.20	3.45	V
E3	Power detection level	V_{RST2}	At falling	2.70	2.90	3.10	
E4	Supply voltage change rate	$\Delta t1/\Delta V$		2			ms/V
E5	Supply voltage change rate	$\Delta t2/\Delta V$	When 0.1 μF capacity is connected to NRST pin	0.2			ms/V
Consumption current							
E6	Auto reset power consumption	I_{DD15}	V_{DD50} = 5.0 V		1.5	3	μA

1.5.6 Power Supply Voltage Detection Circuit

F. Power Supply Voltage Detection Circuit

V_{DD50} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
F1	Power supply detection level 1-1	V_{LVI11}	At rising	3.8	4.0	4.2	V
F2	Power supply detection level 1-2	V_{LVI12}	At falling	3.7	3.9	4.1	
F3	Power supply detection level 2-1	V_{LVI21}	At rising	3.6	3.8	4.0	
F4	Power supply detection level 2-2	V_{LVI22}	At falling	3.5	3.7	3.9	
F5	Power supply detection level 3-1	V_{LVI31}	At rising	3.4	3.6	3.8	
F6	Power supply detection level 3-2	V_{LVI32}	At falling	3.3	3.5	3.7	
F7	Power supply detection level 4-1	V_{LVI41}	At rising	3.2	3.4	3.6	
F8	Power supply detection level 4-2	V_{LVI42}	At falling	3.1	3.3	3.5	
F9	Power supply detection level 5-1	V_{LVI51}	At rising	3.0	3.2	3.4	
F10	Power supply detection level 5-2	V_{LVI52}	At falling	2.9	3.1	3.3	
F11	Power supply detection level 6-1	V_{LVI61}	At rising	2.8	3.0	3.2	
F12	Power supply detection level 6-2	V_{LVI62}	At falling	2.7	2.9	3.1	
F13	Power supply detection level 7-1	V_{LVI71}	At rising	2.7	2.8	2.9	
F14	Power supply detection level 7-2	V_{LVI72}	At falling	2.6	2.7	2.8	
F15	Power supply detection level 8-1	V_{LVI81}	At rising	2.5	2.6	2.7	
F16	Power supply detection level 8-2	V_{LVI82}	At falling	2.4	2.5	2.6	
F17	Power supply detection level 9-1	V_{LVI91}	At rising	2.3	2.4	2.5	
F18	Power supply detection level 9-2	V_{LVI92}	At falling	2.2	2.3	2.4	
F19	Power supply detection level 10-1	V_{LVI101}	At rising	2.1	2.2	2.3	
F20	Power supply detection level 10-2	V_{LVI102}	At falling	2.0	2.1	2.2	
F21	Minimum pulse width	T_W		20	60		µs
F22	Supply voltage change rate	$\Delta t/\Delta V$		2			ms/V
Consumption current							
F23	Consumption current in power supply detection circuit	I_{DD16}	V_{DD50}=5.0 V		2	4	µA

1.5.7 Internal High-speed Oscillation Circuit

G. Internal High-speed Oscillation Circuit

V_{DD50} = 2.0 V to 5.5 V V_{SS} = 0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
G1	Internal high-speed oscillation circuit frequency	f_{rc20}	Ta = -40 °C to +85 °C		20		MHz
G2		f_{rc16}			16		
G3	Temperature dependence of oscillation frequency (44 pin QFP) *19	f_{rc1}	Ta = 25 °C	-1.1		1.1	%
G4		f_{rc2}	Ta = -40 °C to +85 °C	-1.7		1.7	
G5	Temperature dependence of oscillation frequency (32 pin TQFP) *19	f_{rc3}	Ta = 25 °C	-1.0		1.0	%
G6		f_{rc4}	Ta = -40 °C to +85 °C	-1.6		1.6	

*19 The specification values described in G3 to G6 are for standard application. For special application (such as for automotive equipment) has different value.
Oscillation characteristic improvement product (±1 % Ta=-40 °C to +85 °C) is under development.
When using this LSI, consult our sales offices for the product specifications.

1.5.8 Internal Low-speed Oscillation Circuit

H. Internal Low-speed Oscillation Circuit

V_{DD50} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta=-40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
H1	Internal low-speed oscillation circuit frequency	f_{rcs}		27	30	33	kHz

1.5.9 Flash EEPROM Program Conditions

I. Flash EEPROM Program Conditions

V_{DD50} = 2.7 V to 5.5 V V_{SS} = 0 V
Ta=-40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I1	Data retention period *20		Guaranteed programming times 1000 times	10			Year

*20 The specification values described in I1 are for standard application. For special application (such as for automotive product) has different value.
When using this LSI, consult our sales offices for the product specifications.

1.6 Package Dimension

■ Package code: TQFP032-P-0707BUnit: mm

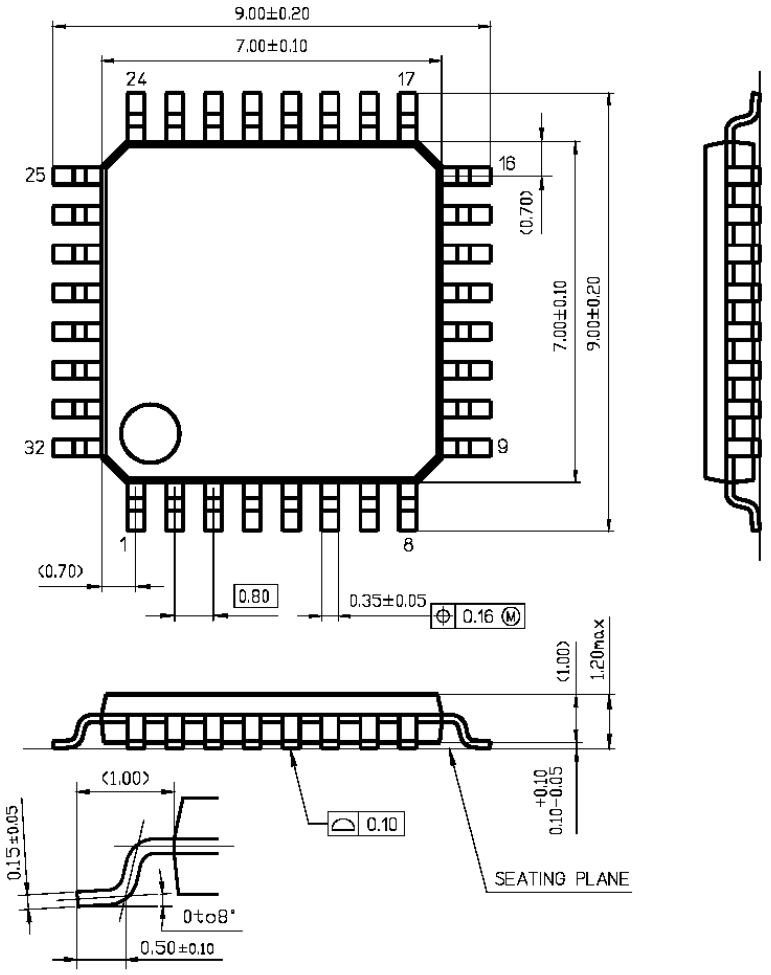

Figure:1.6.1 32-pin TQFP Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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