

Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

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Nuvoton Technology Corporation Japan

MN101E60 Series

8-bit Single-chip Microcontroller

■ Overview

The MN101E series of 8-bit single-chip microcomputers, a memory-expanded version of MN101C series, incorporates multiple types of peripheral functions, and can be used for devices, such as camera, VCR, MD, TV, CD, LD, printer, telephone, HA device, pager, air conditioner, PPC, fax machine, and electronic musical instrument.

This LSI is provided with a flexible and optimized hardware configuration and a simple and efficient instruction system. The MN101EF60D includes an internal ROM of up to 64 KB and a RAM of up to 4 KB, and is equipped with peripheral functions, such as 5 external interrupts, 30 internal interrupts including NMI, 13 timer counters, 3-system serial interface, LCD driver, $\Delta\Sigma$ 16-bit A/D converter, SAR10-bit A/D converter, watchdog timer, and remote control carrier output function providing a system configuration suited for microcomputers for measurement system and controllers, such as for electricity meter.

The LSI also includes a three-system oscillation circuitry (high-speed oscillation of up to 20 MHz, low-speed oscillation of 32 kHz, and RC high-speed oscillation of up to 20 MHz), allowing the system clock to be switched among high-speed oscillation input (high-speed mode), internal RC high-speed oscillation input (RC mode), and low-speed oscillation input (low-speed mode).

The system clock is generated by dividing the oscillation clock frequency. The optimum operation clock for the system can be selected by programmatically switching its frequency-dividing ratio. The high-speed mode and the RC mode include a normal mode which is based on a clock ($f_{osc}/2$) obtained by dividing the original oscillation frequency, f_{osc} , by two, and a double-speed mode which is based on a clock having the same cycle as the original oscillation (f_{osc}).

A machine cycle (minimum instruction execution time) is 100 ns with the original oscillation $f_{osc} = 20$ MHz in the normal mode, and 50 ns with the original oscillation $f_{osc} = 20$ MHz in the double-speed mode, where the CPU is operated at the same clock cycle as the original oscillation. Package type is a 80-pin LQFP.

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Package
MN101EF60D	64 KB	4 KB	Flash EEPROM version	LQFP080-P-1414D

■ Features

- ROM size:
65536 × 8-bits (64 KB)

- RAM size:
4096 × 8-bits (4 KB)

- Package:
LQFP080 (14 mm × 14 mm / 0.65 mm pitch)

- Operating voltage:
1.8 V to 3.6 V
2.7 V to 3.6 V (Flash Memory E/W)
2.7 V to 3.6 V ($\Delta\Sigma$ 16-bit A/D converter operation)

- Machine cycle:
High-speed mode
0.05 μ s / 20 MHz (2.7 V to 3.6 V)
0.125 μ s / 8 MHz (1.8 V to 3.6 V)
Low-speed mode
61 μ s / 32.768 kHz (1.8 V to 3.6 V)

- Internal clock gear circuit:
Able to change the frequency-dividing ratio of the oscillation clock to change the rate of the internal system clock
(Dividing ratios: 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128)

- Oscillation circuit:
Internal three systems of the oscillation circuit
High-speed mode External oscillation frequency : 1 MHz to 20 MHz
High-speed mode Internal RC oscillation frequency : 20 MHz / 16 MHz \pm 5 %
Low-speed mode External oscillation frequency : 32.768 kHz

- Operation mode:
NORMAL mode (High-speed mode)
SLOW mode (Low-speed mode)
HALT mode (High-speed / Low-speed mode)
STOP mode
The operation clock can be switched in each mode.

- Operating ambient temperature:
-40°C to +85°C

- ROM correction:
Up to 7 portions of programs can be modified / changed.

- Extended calculation functions:
16-bit × 16-bit multiplication, 32-bit / 16-bit division

- Automatic reset function

■ Features (continued)

• Interrupt: 30 interrupts

<Processing error interrupt>

NMI - Non-maskable interrupt (NMI)

<External interrupt>

PSELIRQ - External VBAT interrupt (edge selection)

IRQ0 - External interrupt 0 (edge selection, both-edges selection, connectable to noise filter)

IRQ1 - External interrupt 1 (edge selection, both-edges selection, connectable to noise filter)

IRQ2 - External interrupt 2 (edge selection, both-edges selection, connectable to noise filter)

IRQ3 - External interrupt 3 (edge selection, both-edges selection, connectable to noise filter, A/D 1 zero-cross determination)

<Timer interrupt>

TM0IRQ - Timer 0 interrupt (8-bit timer)

TM1IRQ - Timer 1 interrupt (8-bit timer)

TM2IRQ - Timer 2 interrupt (8-bit timer)

TM3IRQ - Timer 3 interrupt (8-bit timer)

TM4IRQ - Timer 4 interrupt (8-bit timer)

TM5IRQ - Timer 5 interrupt (8-bit timer)

TM6IRQ - Timer 6 interrupt (8-bit timer)

TBIRQ - Time-base interrupt

TM7IRQ - Timer 7 interrupt (16-bit timer)

TM7OC2IRQ - Timer 7 compare 2 match interrupt (16-bit timer)

TM8IRQ - Timer 8 interrupt (16-bit timer)

TM8OC2IRQ - Timer 8 compare 2 match interrupt (16-bit timer)

TM9IRQ - Timer 9 interrupt (16-bit timer)

TM9OC2IRQ - Timer 9 compare 2 match interrupt (16-bit timer)

TMAIRQ - Timer A interrupt (16-bit timer)

TMAOC2IRQ - Timer A compare 2 match interrupt (16-bit timer)

<Serial interrupt>

SC0RIRQ - Serial 0 reception interrupt (UART reception)

SC0TIRQ - Serial 0 transmission interrupt (UART transmission, Clock synchronous)

SC1RIRQ - Serial 1 reception interrupt (UART reception)

SC1TIRQ - Serial 1 transmission interrupt (UART transmission, Clock synchronous)

SC3IRQ - Serial 3 interrupt (Single master IIC, Clock synchronous)

<A/D conversion completion interrupt>

AD0IRQ - A/D 0 (SAR ADC) conversion completion interrupt

AD1IRQ - A/D 1 ($\Delta\Sigma$ ADC) conversion completion interrupt

<Power supply monitor interrupt>

PMONIRQ - Power supply monitor interrupt

■ Features (continued)

- Timer Counter: 13 timers, All timer counters generate interrupts

Timer 0 (8-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output, event count, simple pulse width measurement, remote control carrier output base timer

Large current output selectable

Serial interface transfer clock output

Clock source: f_{osc} , $f_{osc}/4$, $f_{osc}/16$, $f_{osc}/32$, $f_{osc}/64$, $f_s/2$, $f_s/4$, f_x , external input (TM0IO)

Timer 1 (8-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output, event count

16-bit cascade connection (with Timer 0)

Serial interface transfer clock output

Clock source: f_{osc} , $f_{osc}/4$, $f_{osc}/16$, $f_{osc}/64$, $f_{osc}/128$, $f_s/2$, $f_s/8$, f_x , external input (TM1IO)

Timer 2 (8-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output, event count, simple pulse width measurement

Large current output selectable

Serial interface transfer clock output

Clock source: f_{osc} , $f_{osc}/4$, $f_{osc}/16$, $f_{osc}/32$, $f_{osc}/64$, $f_s/2$, $f_s/4$, f_x , external input (TM2IO)

Timer 3 (8-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output, event count

16-bit cascade connection (with Timer 2)

Serial interface transfer clock output

Clock source: f_{osc} , $f_{osc}/4$, $f_{osc}/16$, $f_{osc}/64$, $f_{osc}/128$, $f_s/2$, $f_s/8$, f_x , external input (TM3IO)

Timer 4 (8-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output, event count, simple pulse width measurement, remote control carrier output base timer

Large current output selectable

Serial interface transfer clock output

Clock source: f_{osc} , $f_{osc}/4$, $f_{osc}/16$, $f_{osc}/32$, $f_{osc}/64$, $f_s/2$, $f_s/4$, f_x , external input (TM4IO)

Timer 5 (8-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output, event count

16-bit cascade connection (with Timer 4)

Serial interface transfer clock output

Clock source: f_{osc} , $f_{osc}/4$, $f_{osc}/16$, $f_{osc}/64$, $f_{osc}/128$, $f_s/2$, $f_s/8$, f_x , external input (TM5IO)

Timer 6 (8-bit free-running timer, time-base timer)

8-bit free-running timer

Clock source: f_{osc} , f_s , f_x

A one-minute timer can be set in combination with time-base timer

Time-base timer

Clock source: f_{osc} , f_x

Interrupt generation cycle: $f_{osc}/2^7$, $f_{osc}/2^8$, $f_{osc}/2^9$, $f_{osc}/2^{10}$, $f_{osc}/2^{13}$, $f_{osc}/2^{15}$, $f_x/2^7$, $f_x/2^8$, $f_x/2^9$, $f_x/2^{10}$, $f_x/2^{13}$, $f_x/2^{15}$

Timer 7 (16-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output (duty/cycle continuous changeable), pulse width measurement, input capture

Large current output is selectable

Clock source: Any frequency of f_{osc} , f_x , f_s is divided by 1/1, 1/2, 1/4, 1/16

■ Features (continued)

• Timer Counter (continued)

Timer 8 (16-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output (duty/cycle continuous changeable), pulse width measurement, input capture

Large current output is selectable

Clock source: Any frequency of f_{osc} , f_x , f_s is divided by 1/1, 1/2, 1/4, 1/16

Timer 9 (16-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output (duty/cycle continuous changeable), event count, pulse width measurement, input capture

Large current output is selectable

Clock source: Any frequency of f_{osc} , f_x , f_s and external input (TM9IO) is divided by 1/1, 1/2, 1/4, 1/16

Timer A (16-bit timer for general-purpose)

Square wave output (timer pulse output), PWM output (duty/cycle continuous changeable), event count, pulse width measurement, input capture

Large current output selectable

Clock source: Any frequency of f_{osc} , f_x , f_s and external input (TMAIO) is divided by 1/1, 1/2, 1/4, 1/16

Watchdog timer

Processing error detection cycle is selected from $f_s/2^{16}$, $f_s/2^{18}$, $f_s/2^{20}$

When software processing error is detected, system reset is generated by the hardware.

• Remote control carrier output

Remote control carrier output (1/2 duty or 1/3 duty) is generated from timer 0 and timer 4 as the base timer.

• Serial interface

Serial 0 (Full-duplex UART / Clock synchronous serial interface)

Synchronous serial interface

Transfer clock source: $f_{osc}/2$, $f_{osc}/4$, $f_{osc}/16$, $f_{osc}/64$, $f_s/2$, $f_s/4$, external clock

Timer 0 output, Timer 1 output, Timer 2 output, Timer 3 output

MSB/LSB can be selected as the first bit to be transferred. Any size of 1 to 8 bits can be transferred.

Continuous reception, continuous transmission, and continuous reception/transmission are available.

Available for 2-wire serial

Full-duplex UART

Baud rate timer: Timer 0, Timer 1, Timer 2, Timer 3)

Parity check, overrun error/framing error detection

The transfer bits of 7 to 8 can be selected.

UART communications generate two interrupts, transmission completion interrupt, reception completion interrupt

Serial 1 (Full-duplex UART / Clock synchronous serial interface)

Synchronous serial interface

Transfer clock source: $f_{osc}/2$, $f_{osc}/4$, $f_{osc}/16$, $f_{osc}/64$, $f_s/2$, $f_s/4$, external clock

Timer 0 output, Timer 1 output, Timer 2 output, Timer 3 output

MSB/LSB can be selected as the first bit to be transferred. Any size of 1 to 8 bits can be transferred.

Continuous reception, continuous transmission, and continuous reception/transmission are available.

Available for 2-wire serial

Full-duplex UART

Baud rate timer: Timer 0, Timer 1, Timer 2, Timer 3)

Parity check, overrun error/framing error detection

The transfer bits of 7 to 8 can be selected.

UART communications generate two interrupts, transmission completion interrupt, reception completion interrupt

■ Features (continued)

- Serial interface (continued)

Serial 3 (Single master IIC / Clock synchronous serial interface)

Synchronous serial interface

Transfer clock source: $osc/2$, $fosc/4$, $fosc/16$, $fosc/32$, $fs/2$, $fs/4$, external clock

Timer 0 output, Timer 1 output, Timer 2 output, Timer 3 output

MSB/LSB can be selected as the first bit to be transferred. Any size of 1 to 8 bits can be transferred.

Continuous reception, continuous transmission, and continuous reception/transmission are available.

Available for 2-wire serial

Single master IIC

Single master-supported IIC communication available (9-bit transfer with ACK)

- Sigma-delta Analog-to-digital converter): 16-bit 1 system

Over sampling ratio : 64

Over sampling clock : $f_{osr} = 2.5 \text{ MHz}$ ($f_{osc} = 10 \text{ MHz}$, dividing ratio 1/4)

Sampling clock : $f_{smp} = 39.0625 \text{ kHz}$ ($= f_{osr}/64$)

Conversion time : $62.4 \mu\text{s}$ ($= 1/f_{smp} \times 2 + 1/f_{osr} \times 28$)

Differential voltage input : 4 channels

Offset detection channel

Internal PGA ($\times 1, 2, 4, 8, 16, 32$)

Internal Thermistor

- SAR Analog-to-digital converter): 10-bit 1 system

Minimum conversion time : $15 \mu\text{s}$

External single voltage input : 6 channels

Internal 1.8 V reference power supply voltage input : 1 channel

Internal V_{SS} power supply voltage input : 1 channel

- Internal DC magnetic field sensor (Hall element)

- Power supply select (External DC power supply voltage automatic monitor)

Buttery power supply select signal (VBATOUT) is output and external VBAT interrupt (PSELIRQ) is generated, when the voltage of VDC is dropped.

- Power supply voltage detection

Power supply voltage detection function monitors V_{DD33} and generates power supply monitor interrupt (PMONIRQ).

Detection voltage of V_{DD33} : 2.2 V to 3.1 V (programmable step: 0.1 V)

- Power-On reset

■ Features (continued)

• LCD driver

Segment output: max. 28 pins

SEG0 to SEG11 can be switched to I/O ports in 4 bits.

SEG12 to SEG27 can be switched to I/O ports in 1 bit.

Common output: 4 pins

COM0 to 3 can be switched to I/O ports in 1 bit.

Display mode selection

Static

1/2 duty, 1/2 bias

1/3 duty, 1/3 bias

1/4 duty, 1/3 bias

LCD drive clock

When the source clock is the main clock (fosc)

$1/2^{24}, 1/2^{23}, 1/2^{22}, 1/2^{21}, 1/2^{20}, 1/2^{19}, 1/2^{18}, 1/2^{17}, 1/2^{16}, 1/2^{15}, 1/2^{14}, 1/2^{13}, 1/2^{12}, 1/2^{11}$

When the source clock is the sub clock (fx)

$1/2^{14}, 1/2^{13}, 1/2^{12}, 1/2^{11}, 1/2^{10}, 1/2^9, 1/2^8, 1/2^7, 1/2^6$

LCD power supply

External supply voltage: supplied by $V_{LC3}, V_{LC2}, V_{LC1}$ ($V_{LC1} \leq V_{DD33}$)

External supply voltage is divided by internal resistors. (Available on $V_{LC1} = V_{DD33}$)

• I/O ports: 50 pins

LED driver (high current output) : 4 pins

LCD segment : 28 pins

LCD common : 4 pins

Serial interface communication : 15 pins

Timer output : 4 pins

Timer I/O : 8 pins

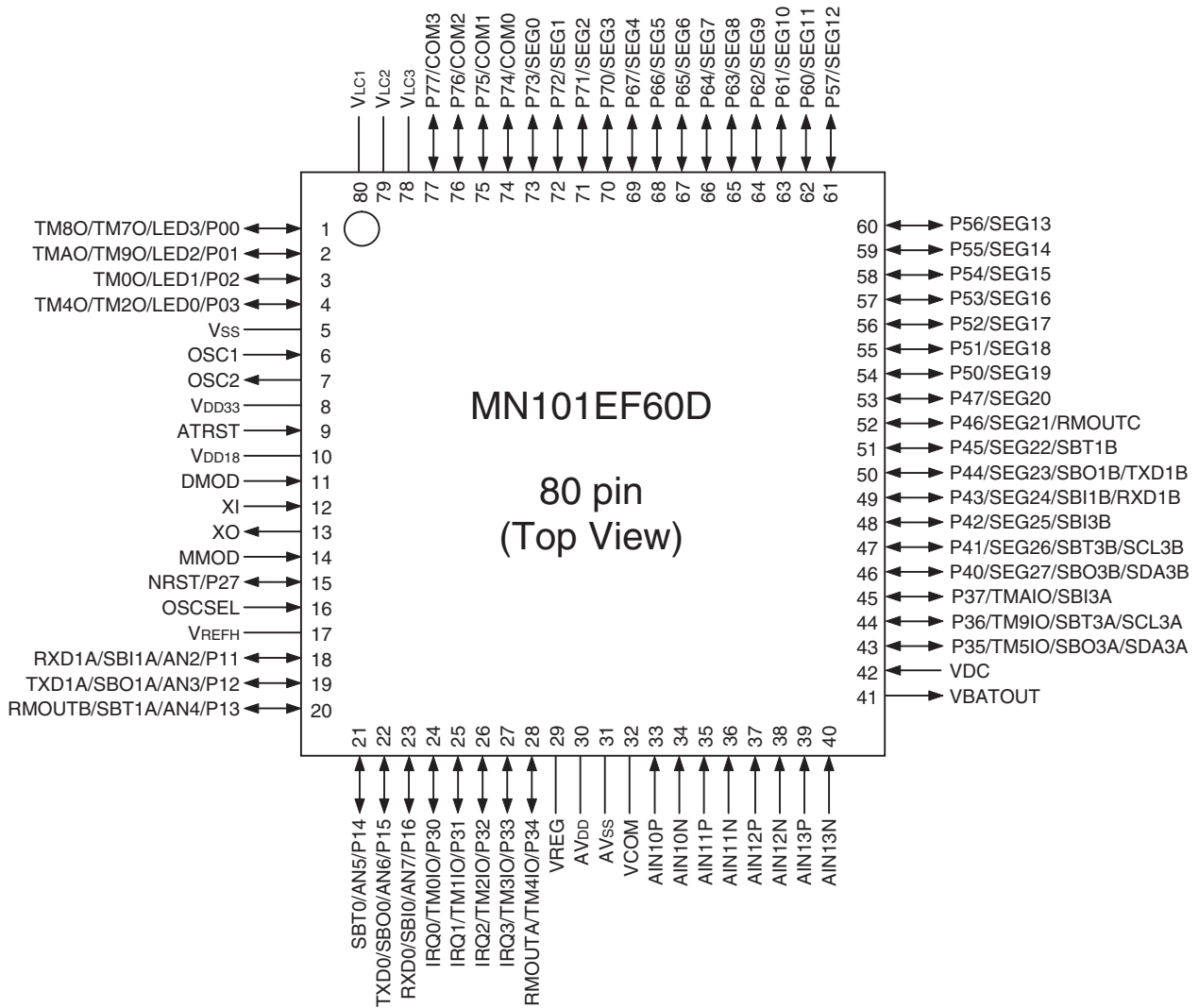
A/D 0 (SAR 10-bit ADC) input : 6 pins

External interrupt : 4 pins

Remote control carrier output : 3 pins

■ Pin Description

- LQFP080-P-1414D



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