Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

Panasonic

1.1 Overview

1.1.1 Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. The MN101E30 series have an internal 928 KB (maximum) of ROM and 8 KB (maximum) of RAM. Peripheral functions include 6 external interrupts, 30 internal interrupts including NMI, 9 timer counters, 6 sets of serial interfaces, A/D converter, D/A converter, LCD driver, watchdog timer, 2 sets of automatic data transfer, synchronous output function and buzzer output. The configuration of this microcomputer is well suited for application as a system controller in camera, timer selector for VCR, CD player, or minicomponent, and also suited for audio reproduction with a high-precision D/A converter.

With three oscillation system (high frequency: max. 20 MHz / low frequency: 32.768 kHz and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high frequency input (high speed mode), PLL input (PLL mode), or to low frequency input (low speed mode). The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software. High speed mode has the normal mode based on fpll/2 which is half clock generated from an original oscillation and PLL, and the double speed mode based on fpll which is clock generated from an original oscillation without dividing.

A machine cycle (min. instructions execution) in the normal mode is 100 ns when fosc is 20 MHz (at the time that PLL is not used). A machine cycle in the double speed mode is 50 ns when fosc is 20 MHz. A machine cycle in the PLL mode is 50 ns (maximum).The package is 100-pin QFP, LQFP.

1.1.2 Product Summary

This manual describes the following models of the MN101E30 series. These products have identical functions, and their memory capacity and type are shown below.

Table:1.1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Package
MN101E30N	508 KB	8 KB	Mask ROM version	LQFP100-P-1414C QFP100-P-1818B
MN101E30R	928 KB	8 KB	Mask ROM version	QFP100-P-1818B
MN101EF30R	928 KB	8 KB	Flash EEPROM version	LQFP100-P-1414 QFP100-P-1818B

This manual is described with a focus on MN101E30N.

1.2 Hardware Functions

■ Feature

- ROM Capacity: 508/928 KB
- RAM Capacity: 8 KB

- Package: 100pin LQFP (14 mm square, 0.5 mm pitch)
  100pin QFP (18 mm square, 0.65 mm pitch)

- Machine Cycle:
  High speed mode
  0.05 ms/ 20 MHz (2.2 V to 5.5 V)
  PLL mode
  0.05 µs/ 20 MHz (2.2 V to 5.5 V)
  Low speed mode
  62.5 µs/16 kHz (2.2 V to 5.5 V)

- Clock Gear: Operation speed of system clock is variable by changing the frequency.

- Multiplied Clock: High-speed frequency clock (fosc) can be multiplied by 2, 3, 4, 5, 6, 8 and 10.

- Memory bank:
  Data memory space is expanded by the bank system.
  - Bank for the source address/Bank for the destination address.

- ROM correction: Correcting address designation: up to 7 addresses possible

- Operation Modes:
  NORMAL mode (High speed mode)
  PLL mode
  SLOW mode (Low speed mode)
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)

- Operating Voltage: 2.2 V to 5.5 V

- Operating Temperature: -40°C to +85°C

- Interrupt: 36 levels

<Watchdog timer>

- NMI-Watchdog timer overflow

<Timer interrupts>

- TM0IRQ-Timer 0 interrupt (8-bit timer)
- TM1IRQ-Timer 1 interrupt (8-bit timer)
- TM2IRQ-Timer 2 interrupt (8-bit timer)
- TM3IRQ-Timer 3 interrupt (8-bit timer)
- TM4IRQ-Timer 4 interrupt (8-bit timer)
- TM6IRQ-Timer 6 interrupt (8-bit timer)
- TBIRQ-Clock timer interrupt
- TM7IRQ-Timer 7 interrupt (16-bit timer)
- T7OC2IRQ- Timer 7 interrupt (16-bit timer)
- TM8IRQ-Timer 8 interrupt (16-bit timer)
- T8OC2IRQ- Timer 8 interrupt (16-bit timer)
- TM9IRQ-Timer 9 interrupt (16-bit timer)
- T9OC2IRQ- Timer 9 interrupt (16-bit timer)

<Serial interrupts>

- SC0TIRQ-Serial interface 0 interrupt
- SC0RIRQ-Serial interface 0 UART reception interrupt (peripheral function group interrupt)
- SC1TIRQ-Serial interface 1 interrupt
- SC1RIRQ-Serial interface 1 UART reception interrupt (peripheral function group interrupt)
- SC2TIRQ-Serial interface 2 interrupt
- SC2RIRQ-Serial interface 2 UART reception interrupt
- SC3TIRQ-Serial interface 3 interrupt
- SC3RIRQ-Serial interface 3 UART reception interrupt (peripheral function group interrupt)
- SC4TIRQ- Serial interface 4 interrupt
- SC4SIRQ- Serial interface 4 stop condition interrupt (peripheral function group interrupt)
- SC5TIRQ- Serial interface 5 interrupt (peripheral function group interrupt)

<A/D conversion end>

- ADIRQ-AD conversion end (peripheral function group interrupt)

<Automatic Transfer Controller interrupts>

- ATC0IRQ-ATC0 interrupt (peripheral function group interrupt)
- ATC1IRQ-ATC1 interrupt (peripheral function group interrupt)

<External interrupts> Edge selectable

- IRQ0:External interrupt (AC zero-cross detector, With/Without noise filter)
- IRQ1:External interrupt (AC zero-cross detector, With/Without noise filter)
- IRQ2:External interrupt (Both edges interrupt)
- IRQ3:External interrupt (Both edges interrupt)
- IRQ4:External interrupt (Both edges interrupt)
- IRQ5:External interrupt (Key scan interrupt only)

<Audio interrupts>

- Audio reproduction end interrupt
- Audio phrase end interrupt

- Timer Counter: 11 timers All timer counters generate interrupt (10 can be operated independently)
  - 8-bit timer for general use: 5 sets
  - 8-bit free-running timer: 1 set
  - Time base timer: 1 set
  - 16-bit timer for general use: 3 sets
  - Simple 8-bit timer: 1 set

Timer 0 (8-bit timer for general use)

- Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM0IOB), event count, remote control carrier output, simple pulse with measurement
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output
- Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 1 (8-bit timer for general use)

-Square wave output (timer pulse output), event count, 16-bit cascade connected (timer0, 1) timer synchronous output event

-Clock source
fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 2 (8-bit timer for general use)

- Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM2IOB), event count, simple pulse with measurement, 24-bit cascade connected (timer0, 1) timer synchronous output event
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output
- Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; "High"-fixed, "LOW"-fixed and "Hi-Z"-fixed

Timer 3 (8-bit timer for general use)

- Square wave output (timer pulse output), event count, remote control carrier output, 16bit cascade connected (timer2), 32-bit cascade connected (timer0, 1, 2)
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 4 (8-bit timer for general use)

- Square wave output (timer pulse output), added pulse(2-bit) system PWM output, event count, serial transfer clock, simple pulse measurement
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 6 (8-bit free-running timer, Time base timer)

8-bit free-running timer

- Clock source
  fpll, fpll/2^{12}, fpll/2^{13}, fs, fx, fx/2^{12}, fx/2^{13}

Time base timer

- Interrupt generation cycle
  fpll/2^{7}, fpll/2^{8}, fpll/2^{9}, fpll/2^{10}, fpll/2^{13}, fpll/2^{15}, fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-bit timer for general use)

- Clock source
  fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16
  1/1, 1/2, 1/4, 1/16 of the external clock, TimerA output
- Hardware organization
  Compare register with double buffer: 2 sets

Input capture register: 1 set
Timer interrupt: 2 vectors

- Timer functions
  Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable), IGBT output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOB
  Timer synchronous output, event count, Input capture function (Both edges can be operated)

-Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 8 (16-bit timer for general use)

-Clock source
  fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16
  1/1, 1/2, 1/4, 1/16 of the external clock, TimerA output

-Hardware organization
  Compare register with double buffer: 2 sets
  Input capture register: 1 set
  Timer interrupt: 2 vectors

-Timer functions
  Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture (Both edge available), 32-bit cascade connected (Timer7, 8), 32-bit PWM output, Input capture is available at 32-bit cascade

Timer 9 (16-bit timer for general use)

-Clock source
  fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16, 1/1, 1/2, 1/4, 1/16 of the external clock
  TimerA output

-Hardware organization
  Compare register with double buffer: 2 sets
  Input capture register: 1 set
  Timer interrupt: 2 vectors

-Timer functions
  Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM9IOB, event count, pulse width measurement, input capture (Both edge available)

-Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

TimerA output (Simple timer counter A)

Clock output for peripheral function

- Watchdog timer

  - Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
  - On detection of errors, hard reset is done inside LSI.

- Synchronous output function

  - Timer synchronous output, interrupt synchronous output Port 8 outputs the latched data, on the event timing of the synchronous output signal of timer 1, 2, or 7, or of the external interrupt 2 (IRQ2).

- Buzzer Output/Reverse Buzzer Ouput:

  - Output frequency can be selected from $fpll/2^9$,$fpll/2^{10}$,$fpll/2^{11}$,$fpll/2^{12}$,$fpll/2^{13}$, $fpll/2^{14}$,$fx/2^3$,$fx/2^4$.

- Remote Control Carrier Output:

  - A remote control carrier output with duty cycle of 1/2 or 1/3 of timer 0 or timer 3 output are available.

- A/D Converter: 10-bit x 12 channels

- D/A Converter: 8-bit x 4 channels

- Data automatic transfer:2 systems

  ATC0

  Data is transferred automatically in all memory space

  - External request/internal event request/software request
  - Maximum transfer cycles are 255
  - Support continuous serial transmission / reception.
  - Burst transfer function (Urgent stop of interrupts is contained.)

  ATC1

  Data is transferred automatically in all memory space

  - External request/internal event request/software request
  - Maximum transfer cycles are 255
  - Support continuous serial transmission / reception.
  - Burst transfer function (Urgent stop of interrupts is contained.)

- Serial Interface: 6 channels

Serial 0 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 1 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 2 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output,external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 3 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output ,external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.

- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 4 (multi master I2C / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source
  fpll/2, fpll/4, fpll/8, fpll/32, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Multi master I2C

- 7-bit of slave address can be set.
- General call communication mode handling

Serial 5

- IIC slave interface
- IIC high-speed transfer mode (communication speed: 400 kbps)
- 7-bit or 10-bit of slave address can be set.
- General call communication mode handling

- LED Driver: 8 pins (Push-pull structure)

- Automatic Reset

- LCD Driver: LCD driver pins

Segment output max. 55 pins (SEG0 to 54)

SEG0 to 54 can be switched to I/O ports by 1 pin

[Note:At reset, SEG0 to 54 are input ports.]

Common output pins:4 pins

COM0 to 3 can be switched to I/O ports by 1 pin

Display mode selection

Static

1/2 duty, 1/2 bias

1/3 duty, 1/3 bias

1/4 duty, 1/3 bias

LCD driver clock

- When the source clock is the main clock (fpll)
  $1/2^{18}$, $1/2^{17}$, $1/2^{16}$, $1/2^{15}$, $1/2^{14}$, $1/2^{13}$, $1/2^{12}$, $1/2^{11}$
- When the source clock is the sub clock (fx)
  $1/2^{9}$, $1/2^{8}$, $1/2^{7}$, $1/2^{6}$
- Timer0, 1, 2, 3, 4 and A output

LCD power supply

Use at $V_{DD5} \geq V_{LC1}$
External supply voltage is input from V_{LC1}, V_{LC2}, V_{LC3} pins or voltage applied to V_{LC1} is divided by internal resistance and supplied to V_{LC2} and V_{LC3} pins.

- DAC for audio reproduction

Analog DAC input

PWM digital output

Continuous reproduction function

Repeat function (phrase repeat)

Volume control (2048 tone)

Sampling frequency: 8 to 44.1 kHz

- Port:

I/O ports	: 85 pins
LED (large current) driver pins	: 8 pins
LCD driver for segment	: 55 pins
LCD driver for common	: 4 pins
serial interface pin	: 34 pins
Timer I/O	: 28 pins
Buzzer output	: 4 pins
A/D input	: 12 pins
External interrupt pin	: 5 pins
LCD power	: 3 pins
XI/XO	: 2 pins
D/A output	: 4 pins
Audio output	: 2 pins

Special pins	: 10 pins
Operation mode input pins	: 3 pin
Analog reference voltage input pins	: 1 pin
Reset input pin	: 1 pin
Oscillation pins	: 2 pins
Power pins	: 6 pins

1.3 Pin Description

1.3.1 Pin configuration

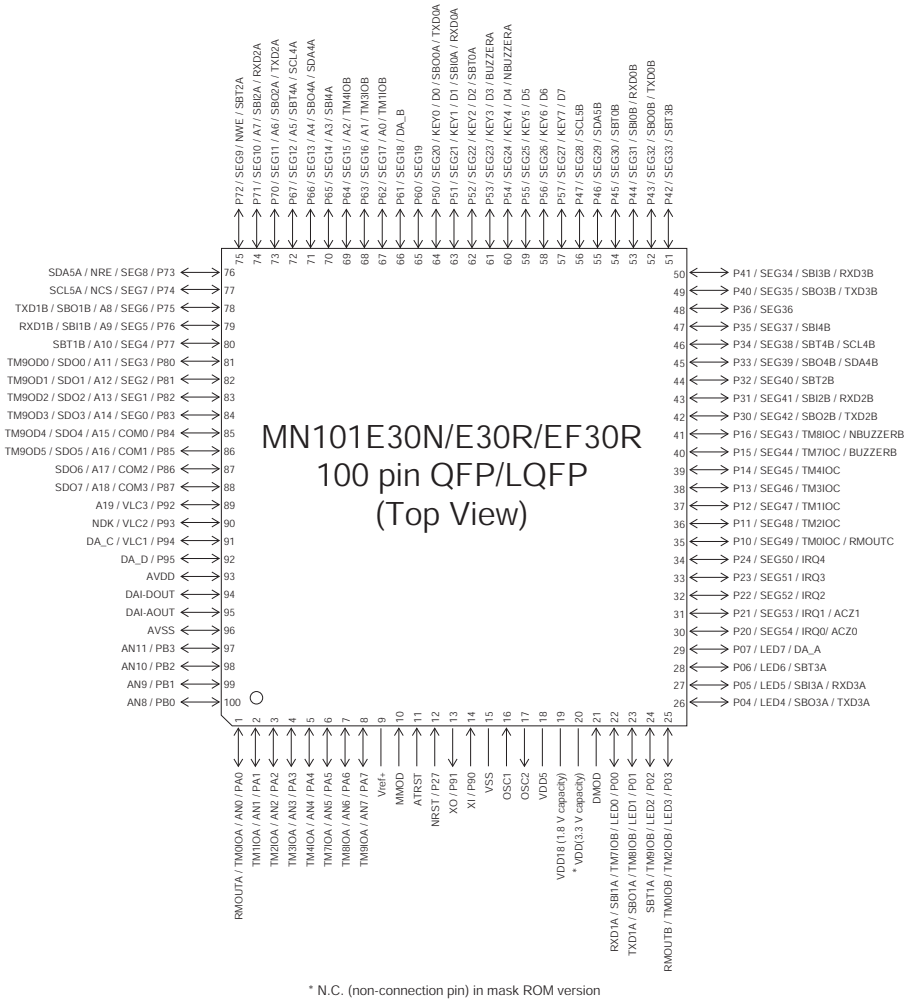

Figure:1.3.1 Pin Configuration (MN101E30N/MN101E30R/MN101EF30R)

Mode	Object microcontroller	Activation area	Pin setting						Register setting
			NRST	ATRST	DMOD	P01	P02	MMOD	EXMEM flag
Single chip mode	FLASH-ROM MASK-ROM	MAIN	(1)	L or H	H	Normal pin		L	0
Memory extend mode	FLASH-ROM MASK-ROM	MAIN	(1)	L or H	H	Normal pin		L	1
Micro controller rewriting mode (3)	FLASH-ROM	BOOT	(1)	L	H	Normal pin		H	0
D-wire communication mode(3)	FLASH-ROM	-	(2)	L	(2)	Pull up(2)	Pull up(2)	L	0

Mode	Object microcontroller	Activation area	Pin setting						Register setting
			NRST	ATRST	DMOD	P01	P02	MMOD	EXMEM flag

(1)The mode becomes fixed from the pin state in releasing NRST(L to H).
(2)This is controlled by a dedicated on-board programmer
(3)This mode becomes the rewriting mode only for Flash microcontroller.
Therefore does not exist in the Mask version (MN101E30N/E30R)

1.3.2 Pin Specification

Table:1.3.1 Pin Specification

Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P00	RXD1A	SBI1A	in/out	P0DIR0	P0PLU0	RXD1A: UART1 reception data input	SBI1A: Serial1 reception data output
	TM7IOB	LED0				TM7IOB: Timer 7 input / output	LED0: LED driver pin 0
P01	TXD1A	SBO1A	in/out	P0DIR1	P0PLUD1	TXD1A: UART1 transmission data output	SBO1A: Serial1 transmission data output
	TM8IOB	LED1				TM8IOB: Timer 8 input / output	LED1: LED driving pin 1
P02	SBT1A	TM9IOB	in/out	P0DIR2	P0PLUD2	SBT1A: Serial 1 clock input / output	TM9IOB: Timer 9 input / output
	LED2					LED2: LED driving pin 2	
P03	RMOUTB	TM0IOB	in/out	P0DIR3	P0PLUD3	RMOUTB: Remote control carrier output	TM0IOB: Timer 0 input / output
	TM2IOB	LED3				TM2IOB: Timer 2 input / output	LED3: LED driving pin 3
P04	LED4	SBO3A	in/out	P0DIR4	P0PLUD4	LED4: LED driving pin 4	SBO3A: Serial3 transmission data output
	TXD3A					TXD3A: UART3 transmission data output	
P05	LED5	SBI3A	in/out	P0DIR5	P0PLUD5	LED5: LED driving pin 5	SBI3A: Serial3 reception data output
	RXD3A					RXD3A: UART3 reception data input	
P06	LED6	SBT3A	in/out	P0DIR6	P0PLUD6	LED6: LED driving pin 6	SBT3A: Serial3 clock input / output
P07	LED7	DA_A	in/out	P0DIR7	P0PLUD7	LED7: LED driving pin 7	DA_A: Analog A output
P10	SEG49	TM0IOC	in/out	P1DIR0	P1PLUD0	SEG49: Segment49 output	TM0IOC: Timer0 input / output
	RMOUTC					RMOUTC: Remote control carrier output	
P11	SEG48	TM2IOC	in/out	P1DIR1	P1PLUD1	SEG48: Segment48 output	TM2IOC: Timer2 input / output
P12	SEG47	TM1IOC	in/out	P1DIR2	P1PLUD2	SEG47: Segment47 output	TM1IOC: Timer1 input / output
P13	SEG46	TM3IOC	in/out	P1DIR3	P1PLUD3	SEG46: Segment46 output	TM3IOC: Timer3 input / output
P14	SEG45	TM4IOC	in/out	P1DIR4	P1PLUD4	SEG45: Segment45 output	TM4IOC: Timer4 input / output
P15	SEG44	TM7IOC	in/out	P1DIR5	P1PLUD5	SEG44: Segment44 output	TM7IOC: Timer7 input / output
	BUZZERB					BUZZERB: Buzzer output	
P16	SEG43	TM8IOC	in/out	P1DIR6	P1PLUD6	SEG43: Segment43 output	TM8IOC: Timer8 input / output
	NBUZZERB					NBUZZERB: Buzzer inversion output	
P20	SEG54	IRQ0	in/out	P2DIR0	P2PLUD0	SEG54: Segment54 output	IRQ0: External interrupt0
	ACZ0					ACZ0: Zero-cross detection input	
P21	SEG53	IRQ1	in/out	P2DIR1	P2PLUD1	SEG53: Segment53 output	IRQ1: External interrupt1
	ACZ1					ACZ1: Zero-cross detection input	
P22	SEG52	IRQ2	in/out	P2DIR2	P2PLUD2	SEG52: Segment52 output	IRQ2: External interrupt2
P23	SEG51	IRQ3	in/out	P2DIR3	P2PLUD3	SEG51: Segment51 output	IRQ3: External interrupt3
P24	SEG50	IRQ4	in/out	P2DIR4	P2PLUD4	SEG50: Segment50 output	IRQ4: External interrupt4
P27	NRST		in	-	-	NRST: Reset	

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Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P30	SEG42	SBO2B	in/out	P3DIR0	P3PLUD0	SEG42: Segment42 output	SBO2B: Serial2 transmission data output
	TXD2B					TXD2B: UART2 transmission data output	
P31	SEG41	SBI2B	in/out	P3DIR1	P3PLUD1	SEG41: Segment41 output	SBI2B: Serial2 reception data output
	RXD2B					RXD2B: UART2 reception data input	
P32	SEG40	SBT2B	in/out	P3DIR2	P3PLUD2	SEG40: Segment40 output	SBT2B: Serial2 clock input / output
P33	SEG39	SBO4B	in/out	P3DIR3	P3PLUD3	SEG39: Segment39 output	SBO4B: Serial4 transmission data output
	SDA4B					SDA4B: IIC4 data input / output	
P34	SEG38	SBT4B	in/out	P3DIR4	P3PLUD4	SEG38: Segment38 output	SBT4B: Serial4 clock input / output
	SCL4B					SCL4B: IIC4 clock input / output	
P35	SEG37	SBI4B	in/out	P3DIR5	P3PLUD5	SEG37: Segment37 output	SBI4B:Serial4 reception data output
P36	SEG36		in/out	P3DIR6	P3PLUD6	SEG36: Segment36 output	
P40	SEG35	SBO3B	in/out	P4DIR0	P4PLUD0	SEG35: Segment35 output	SBO3B: Serial3 transmission data output
	TXD3B					TXD3B: UART3 transmission data output	
P41	SEG34	SBI3B	in/out	P4DIR1	P4PLUD1	SEG34: Segment34 output	SBI3B: Serial3 reception data output
	RXD3B					RXD3B: UART3 reception data input	
P42	SEG33	SBT3B	in/out	P4DIR2	P4PLUD2	SEG33: Segment33 output	SBT3B: Serial3 clock input / output
P43	SEG32	SBO0B	in/out	P4DIR3	P4PLUD3	SEG32: Segment32 output	SBO0B: Serial0 transmission data output
	TXD0B					TXD0B: UART0 transmission data output	
P44	SEG31	SBI0B	in/out	P4DIR4	P4PLUD4	SEG31: Segment31 output	SBI0B: Serial0 reception data output
	RXD0B					RXD0B: UART0 reception data input	
P45	SEG30	SBT0B	in/out	P4DIR5	P4PLUD5	SEG30: Segment30 output	SBT0B: Serial0 clock input / output
P46	SEG29	SDA5B	in/out	P4DIR6	P4PLUD6	SEG29: Segment29 output	SDA5B: IIC5 data input / output
P47	SEG28	SCL5B	in/out	P4DIR7	P4PLUD7	SEG28: Segment28 output	SCL5B: IIC5 clock input / output
P50	SEG20	KEY0	in/out	P5DIR0	P5PLUD0	SEG20: Segment20 output	KEY0: KEY interrupt input0
	D0	SBO0A				D0: Data input / output (bp0)	SBO0A: Serial0 transmission data output
	TXD0A					TXD0A: UART0 reception data input	
P51	SEG21	KEY1	in/out	P5DIR1	P5PLUD1	SEG21: Segment21 output	KEY1: KEY interrupt input1
	D1	SBI0A				D1:Data input / output (bp1)	SBI0A: Serial0 reception data output
	RXD0A					RXD0A: UART0 transmission data output	
P52	SEG22	KEY2	in/out	P5DIR2	P5PLUD2	SEG22: Segment22 output	KEY2: KEY interrupt input2
	D2	SBT0A				D2: Data input / output (bp2)	SBT0A: Serial0 clock input / output
P53	SEG23	KEY3	in/out	P5DIR3	P5PLUD3	SEG23: Segment23 output	KEY3: KEY nterrupt input3
	D3	BUZZERA				D3: Data input / output (bp3)	BUZZERA:Buzzer output
P54	SEG24	KEY4	in/out	P5DIR4	P5PLUD4	SEG24: Segment24 output	KEY4: KEY interrupt input4
	D4	NBUZZERA				D4:Data input / output (bp4)	NBUZZERA: Buzzer inversion output
P55	SEG25	KEY5	in/out	P5DIR5	P5PLUD5	SEG25: Segment25 output	KEY5: KEY interrupt input5
	D5					D5: Data input / output (bp5)	
P56	SEG26	KEY6	in/out	P5DIR6	P5PLUD6	SEG26: Segment26 output	KEY6:KEY interrupt input6
	D6					D6:Data input / output (bp6)	
P57	SEG27	KEY7	in/out	P5DIR7	P5PLUD7	SEG27: Segment27 output	KEY7: KEY interrupt input7
	D7					D7: Data input / output (bp7)	

Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P60	SEG19		in/out	P6DIR0	P6PLUD0	SEG19: Segment19 output	
P61	SEG18	DA_B	in/out	P6DIR1	P6PLUD1	SEG18: Segment18 output	DA_B: Analog B output
P62	SEG17	A0	in/out	P6DIR2	P6PLUD2	SEG17: Segment17 output	A0: Address output (bp0)
	TM1IOB					TM1IOB: Timer1 input / output	
P63	SEG16	A1	in/out	P6DIR3	P6PLUD3	SEG16: Segment16 output	A1: Address output (bp1)
	TM3IOB					TM3IOB: Timer3 input / output	
P64	SEG15	A2	in/out	P6DIR4	P6PLUD4	SEG15: Segment15 output	A2: Address output (bp2)
	TM4IOB					TM4IOB: Timer4 input / output	
P65	SEG14	A3	in/out	P6DIR5	P6PLUD5	SEG14: Segment14 output	A3: Address output (bp3)
	SBI4A					SBI4A: Serial4 reception data output	
P66	SEG13	A4	in/out	P6DIR6	P6PLUD6	SEG13: Segment13 output	A4: Address output (bp4)
	SBO4A	SDA4A				SBO4A: Serial4 transmission data output	SDA4A: IIC4 data input / output
P67	SEG12	A5	in/out	P6DIR7	P6PLUD7	SEG12: Segment12 output	A5: Address output (bp5)
	SBT4A	SCL4A				SBT4A: Serial4 clockinput / output	SCL4A: IIC4 clock input / output
P70	SEG11	A6	in/out	P7DIR0	P7PLUD0	SEG11: Segment11 output	A6: Address output (bp6)
	SBO2A	TXD2A				SBO2A: Serial2 transmission data output	TXD2A: UART2 transmission data output
P71	SEG10	A7	in/out	P7DIR1	P7PLUD1	SEG10: Segment10 output	A7: Address output (bp7)
	SBI2A	RXD2A				SBI2A: Serial2 reception data output	RXD2A: UART2 reception data input
P72	SEG9	NWE	in/out	P7DIR2	P7PLUD2	SEG9: Segment9 output	NWE: Write enable signal
	SBT2A					SBT2A: Serial2 clock input / output	
P73	SDA5A	NRE	in/out	P7DIR3	P7PLUD3	SDA5A: IIC5 data input / output	NRE: Read enable signal
	SEG8					SEG8: Segment8 output	
P74	SCL5A	NCS	in/out	P7DIR4	P7PLUD4	SCL5A: IIC5 clock input / output	NCS: Chip selection signal
	SEG7					SEG7: Segment7 output	
P75	TXD1B	SBO1B	in/out	P7DIR5	P7PLUD5	TXD1B: UART1 transmission data output	SBO1B: Serial1 transmission data output
	A8	SEG6				A8: Address output (bp8)	SEG6: Segment6 output
P76	RXD1B	SBI1B	in/out	P7DIR6	P7PLUD6	RXD1B: UART1 reception data input	SBI1B: Serial1 reception data output
	A9	SEG5				A9: Address output (bp9)	SEG5: Segment5 output
P77	SBT1B	A10	in/out	P7DIR7	P7PLUD7	SBT1B: Serial1 clock input / output	A10: Address output (bp10)
	SEG4					SEG4: Segment4 output	
P80	TM9OD0	SDO0	in/out	P8DIR0	P8PLU0	TM9OD0: Timer9 output	SDO0: Timer synchronous output0
	A11	SEG3				A11: Address output (bp11)	SEG3: Segment3 output
P81	TM9OD1	SDO1	in/out	P8DIR1	P8PLU1	TM9OD1: Timer9 output	SDO1: Timer synchronous output1
	A12	SEG2				A12: Address output (bp12)	SEG2: Segment2 output
P82	TM9OD2	SDO2	in/out	P8DIR2	P8PLU2	TM9OD2: Timer9 output	SDO2: Timer synchronous output2
	A13	SEG1				A13: Address output (bp13)	SEG1: Segment1 output
P83	TM9OD3	SDO3	in/out	P8DIR3	P8PLU3	TM9OD3: Timer9 output	SDO3: Timer synchronous output3
	A14	SEG0				A14: Address output (bp14)	SEG0: Segment0 output
P84	TM9OD4	SDO4	in/out	P8DIR4	P8PLU4	TM9OD4: Timer9 output	SDO4: Timersynchronou soutput4
	A15	COM0				A15: Address output (bp15)	COM0: LCD common output
P85	TM9OD5	SDO5	in/out	P8DIR5	P8PLU5	TM9OD5: Timer9 output	SDO5: Timer synchronous output5
	A16	COM1				A16: Address output (bp16)	COM1:LCD common output
P86	SDO6	A17	in/out	P8DIR6	P8PLU6	SDO6: Timer synchronous output6	A17: Address output (bp17)
	COM2					COM2:LCD common output	
P87	SDO7	A18	in/out	P8DIR7	P8PLU7	SDO7: Timer synchronous output7	A18: Address output (bp18)
	COM3					COM3:LCD common output	

Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P90	XI		in	P9DIR0	P9PLU0	XI: Clock input pin	
P91	XO		out	P9DIR1	P9PLU1	XO: Clock output pin	
P92	A19	V_{LC3}	in/out	P9DIR2	P9PLU2	A19: Address output (bp19)	V_{LC3}: LCD power supply
P93	NDK	V_{LC2}	in/out	P9DIR3	P9PLU3	NDK: Data acknowledge signal	V_{LC2}:LCD power supply
P94	V_{LC1}	DA_C	in/out	P9DIR4	P9PLU4	V_{LC1}:LCD power supply	DA_C: AnalogC output
P95	DA_D		in/out	P9DIR5	P9PLU5	DA_D: AnalogD output	
PA0	RMOUTA AN0	TM0IOA	in/out	PADIR0	PAPLU0	RMOUTA:Remote control carrier output AN0: Analog0 input	TM0IOA: Timer0 input / output
PA1	TM1IOA	AN1	in/out	PADIR1	PAPLU1	TM1IOA: Timer1 input / output	AN1: Analog1 input
PA2	TM2IOA	AN2	in/out	PADIR2	PAPLU2	TM2IOA: Timer2 input / output	AN2: Analog2 input
PA3	TM3IOA	AN3	in/out	PADIR3	PAPLU3	TM3IOA: Timer3 input / output	AN3: Analog3 input
PA4	TM4IOA	AN4	in/out	PADIR4	PAPLU4	TM4IOA: Timer4 input / output	AN4: Analog4 input
PA5	TM7IOA	AN5	in/out	PADIR5	PAPLU5	TM7IOA: Timer7 input / output	AN5: Analog5 input
PA6	TM8IOA	AN6	in/out	PADIR6	PAPLU6	TM8IOA: Timer8 input / output	AN6: Analog6 input
PA7	TM9IOA	AN7	in/out	PADIR7	PAPLU7	TM9IOA: Timer9 input / output	AN7: Analog7 input
PB0	AN8		in/out	PBDIR0	PBPLU0	AN8: Analog8 input	
PB1	AN9		in/out	PBDIR1	PBPLU1	AN9: Analog9 input	
PB2	AN10		in/out	PBDIR2	PBPLU2	AN10: Analog10 input	
PB3	AN11		in/out	PBDIR3	PBPLU3	AN11: Analog11 input	
DA1_ DOUT	DA1_DOUT		out	-	-	Audio digital output	
DA1_ AOUT	DA1_AOUT		out	-	-	Audio analog output	

1.3.3 Pin Functions

Table:1.3.2 Pin Functions

Name	NO	I/O	Other Function	Function	Description
V_{SS} V_{DD5} AV_{DD} AV_{SS}	15 18 93 96	-		Power connect pins	Supply 2.2 V to 5.5 V to V_{DD5}, 5.0 V to AV_{DD} and 0 V to V_{SS} and AV_{SS}.
V_{DD18} (Capacity 1.8 V)	19	-		Capacity connect pins	For internal power circuit output stability, connect at least one bypass capacitor of 1 uF or larger between V_{DD18} and V_{ss}.
V_{DD} (Capacity 3.3 V)	20	-		Capacity connect pins	For internal power circuit output stability, connect at least one bypass capacitor of 1 uF or larger between V_{DD} and V_{ss}. (Only Flash version)
OSC1 OSC2	16 17	Input Output		Clock input pins Clock output pins	Connect these oscillation pins to ceramic or crystal ocsillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
XI XO	14 13	Input Output	P90 P91	Clock input pins Clock output pins	Connect these oscillation pins to crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. the chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to V_{SS} and leave XO open.
NRST	12	Input	P27	Reset pin [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. 50 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if “0” is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between NRST and V_{SS}, it is recommended that a discharge diode be placed between NRST and V_{DD5}.
ATRST	11	input		Auto reset setting pins 2	Input “H” to enable auto reset function and “L” to disable this function
P00 P01 P02 P03 P04 P05 P06 P07	22 23 24 25 26 27 28 29	I/O	RXD1A,SBI1A,TM7IOB,LED0 TXD1A,SBO1A,TM8IOB,LED1 SBT1A,TM9IOB,LED2 RMOUTB,TM0IOB, TM2IOB,LED3 LED4,SBO3A,TXD3A LED5,SBI3A,RXD3A LED6,SBT3A LED7,DA_A	I/O port0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P0PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) Direct LED drive available at output. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).

Name	NO	I/O	Other Function	Function	Description
P10 P11 P12 P13 P14 P15 P16	35 36 37 38 39 40 41	I/O	SEG49,TM0IOC,RMOUTC SEG48,TM2IOC SEG47,TM1IOC SEG46,TM3IOC SEG45,TM4IOC SEG44,TM7IOC,BUZZERB SEG43,TM8IOC,NBUZZERB	I/O port1	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P1PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P20 P21 P22 P23 P24	30 31 32 33 34	I/O	SEG54,IRQ0,ACZ0 SEG53,IRQ1,ACZ1 SEG52,IRQ2 SEG51,IRQ3 SEG50,IRQ4	I/O port2	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P2PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P27	12	input	NRST	I/O port2	Port P27 has an N-channel open-drain configuration. When “0” is written and the reset is initiated by software, a low level will be output.
P30 P31 P32 P33 P34 P35 P36	42 43 44 45 46 47 48	I/O	SEG42,SBO2B,TXD2B SEG41,SBI2B,RXD2B SEG40,SBT2B SEG39,SBO4B,SDA4B SEG38,SBT4B,SCL4B SEG37,SBI4B SEG36	I/O port3	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P3PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P40 P41 P42 P43 P44 P45 P46 P47	49 50 51 52 53 54 55 56	I/O	SEG35,SBO3B,TXD3B SEG34,SBI3B,RXD3B SEG33,SBT3B SEG32,SBO0B,TXD0B SEG31,SBI0B,RXD0B SEG30,SBT0B SEG29,SDA5B SEG28,SCL5B	I/O port4	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P4PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P50 P51 P52 P53 P54 P55 P56 P57	64 63 62 61 60 59 58 57	I/O	SEG20,KEY0,D0,SBO0A, TXD0A SEG21,KEY1,D1,SBI0A, RXD0A SEG22,KEY2,D2,SBT0A SEG23,KEY3,D3,BUZZERA SEG24,KEY4,D4,NBUZZERA SEG25,KEY5,D5 SEG26,KEY6,D6 SEG27,KEY7,D7	I/O port5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P5PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P60 P61 P62 P63 P64 P65 P66 P67	65 66 67 68 69 70 71 72	I/O	SEG19 SEG18,DA_B SEG17,A0,TM1IOB SEG16,A1,TM3IOB SEG15,A2,TM4IOB SEG14,A3,SBI4A SEG13,A4,SBO4A,SDA4A SEG12,A5,SBT4A,SCL4A	I/O port6	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P6PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)

Name	NO	I/O	Other Function	Function	Description
P70 P71 P72 P73 P74 P75 P76 P77	73 74 75 76 77 78 79 80	I/O	SEG11,A6,SBO2A,TXD2A SEG10,A7,SBI2A,RXD2A SEG9,NWE,SBT2A SEG8,SDA5A,NRE SEG7,SCL5A,NCS SEG6,TXD1B,SBO1B,A8 SEG5,RXD1B,SBI1B,A9 SEG4,SBT1B,A10	I/O port7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P7PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P80 P81 P82 P83 P84 P85 P86 P87	81 82 83 84 85 86 87 88	I/O	TM9OD0,SDO0,A11,SEG3 TM9OD1,SDO1,A12,SEG2 TM9OD2,SDO2,A13,SEG1 TM9OD3,SDO3,A14,SEG0 TM9OD4,SDO4,A15,COM0 TM9OD5,SDO5,A16,COM1 SDO6,A17,COM2 SDO7,A18,COM3	I/O port8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P90 P91 P92 P93 P94 P95	14 13 89 90 91 92	I/O	XI XO A19,V_{LC3} NDK,V_{LC2} DA_C,V_{LC1} DA_D	I/O port9	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P8PLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	1 2 3 4 5 6 7 8	I/O	RMOUTA,TM0IOA,AN0 TM1IOA,AN1 TM2IOA,AN2 TM3IOA,AN3 TM4IOA,AN4 TM7IOA,AN5 TM8IOA,AN6 TM9IOA,AN7	I/O portA	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up resistor for each bit can be selected individually by the PAPLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
PB0 PB1 PB2 PB3	100 99 98 97	I/O	AN8 AN9 AN10 AN11	I/O portB	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PBDIR register. A pull-up resistor for each bit can be selected individually by the PBPLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
DA1_DOUT DA1_AOUT	94 95	I/O		Audio output pins	Special output pins for audio production function These output “L” at reset.
SBO0A SBO0B SBO1A SBO1B SBO2A SBO2B SBO3A SBO3B SBO4A SBO4B	64 52 23 78 73 42 26 49 71 45	I/O	P50,SEG20,KEY0,D0 P43,SEG32,TXD0B TXD1A,TM8IOB,LED1,P01 TXD1B,A8,SEG6,P75 P70,SEG11,A6,TXD2A P30,SEG42,TXD2B P04,LED4,TXD3A P40,SEG35,TXD3B P66,SEG13,A4,SDA4A P33,SEG39,SDA4B	Serial interface transmission data output pins	Transmission data output pins for serial interface 0 to 4. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.

Name	NO	I/O	Other Function	Function	Description
SBI0A	63	input	P51,SEG21,KEY1,D1	Serial interface reception data input pins	Reception data output pins for serial interface 0 to 4. A pull-up resistor can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0B	53		P44,SEG31,RXD0B		
SBI1A	22		RXD1A,TM7IOB,LED0,P00		
SBI1B	79		RXD1B,A9,SEG5,P76		
SBI2A	74		P71,SEG10,A7,RXD2A		
SBI2B	43		P31,SEG41,RXD2B		
SBI3A	27		P05,LED5,RXD3A		
SBI3B	50		P41,SEG34,RXD3B		
SBI4A	70		P65,SEG14,A3		
SBI4B	47		P35,SEG37		
SBT0A	62	I/O	P52,SEG22,KEY2,D2	Serial interface clock I/O pins	Clock I/O pins for serial interface 0 to 4. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD, P6PLUD and P7PLUD registers. Select the clock I/O with the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1) according to the communication. These can be used as normal I/O pins when the serial interface is not used.
SBT0B	54		P45,SEG30		
SBT1A	24		TM9IOB,LED2,P02		
SBT1B	80		A10,SEG4,P77		
SBT2A	75		P72,SEG9,NWE		
SBT2B	44		P32,SEG40		
SBT3A	28		P06,LED6		
SBT3B	51		P42,SEG33		
SBT4A	72		P67,SEG12,A5,SCL4A		
SBT4B	46		P34,SEG38,SCL4B		
TXD0A	64	output	P50,SEG20,KEY0,D0,SBO0A	UART transmission data output pins	In the serial interface0 to 3 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
TXD0B	52		P43,SEG32,SBO0B		
TXD1A	23		SBO1A,TM8IOB,LED1,P01		
TXD1B	78		SBO1B,A8,SEG6,P75		
TXD2A	73		P70,SEG11,A6,SBO2A		
TXD2B	42		P30,SEG42,SBO2B		
TXD3A	26		P04,LED4,SBO3A		
TXD3B	49		P40,SEG35,SBO3B		
RXD0A	63	input	P51,SEG21,KEY1,D1,SBI0A	UART reception data input pins	In the serial interface0 to 3 in UART mode, this pin is configured as the reception data output pin. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
RXD0B	53		P44,SEG31,SBI0B		
RXD1A	22		SBI1A,TM7IOB,LED0,P00		
RXD1B	79		SBI1B,A9,SEG5,P76		
RXD2A	74		P71,SEG10,A7,SBI2A		
RXD2B	43		P31,SEG41,SBI2B		
RXD3A	27		P05,LED5,SBI3A		
RXD3B	50		P41,SEG34,SBI3B		
SDA4A	71	I/O	P66,SEG13,A4,SBO4A	IIC data I/O pins	In the serial interface4, 5 in IIC mode, this pin is configured as the data input / output pin. For the output configuration, select n-channel open-drain with the P3ODC, P4ODC, P6ODC and P7ODC registers and pull-up resistors by the P3PLUD, P4PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P3DIR, P4DIR, P6DIR and P7DIR registers and serial data input / output mode by serial mode register 1 (SC4MD1, SC5MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA4B	45		P33,SEG39,SBO4B		
SDA5A	76		NRE,SEG8,P73		
SDA5B	55		P46,SEG29		

Name	NO	I/O	Other Function	Function	Description
SCL4A SCL4B SCL5A SCL5B	72 46 77 56	I/O	P67,SEG12,A5,SBT4A P34,SEG38,SBT4B NCS,SEG7,P74 P47,SEG28	IIC clock I/O pins	In the serial interface4, 5 in IIC mode, this pin is configured as the clock input / output pin. For the output configuration, select n-channel open-drain with the P3ODC, P4ODC, P6ODC and P7ODC registers and pull-up resistors by the P3PLUD, P4PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P3DIR, P4DIR, P6DIR and P7DIR registers and serial data input / output mode by serial mode register 1 (SC4MD1, SC5MD1). These can be used as normal I/O pins when the serial interface is not used
TM0IOA TM0IOB TM0IOC TM1IOA TM1IOB TM1IOC TM2IOA TM2IOB TM2IOC TM3IOA TM3IOB TM3IOC TM4IOA TM4IOB TM4IOC	1 25 35 2 67 37 3 25 36 4 68 38 5 69 39	I/O	RMOUTA,AN0,PA0 RMOUTB,TM2IOB,LED3,P03 P10,SEG49,RMOUTC AN1,PA1 P62,SEG17,A0 P12,SEG47 AN2,PA2 RMOUTB,TM0IOB,LED3,P03 P11,SEG48 AN3,PA3 P63,SEG16,A1 P13,SEG46 AN4,PA4 P64,SEG15,A2 P14,SEG45	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 4. To use this pin as event clock input, configure this as input by P0DIR register, P1DIR register, P6DIR register and PADIR register. In the input mode, pull-up resistors can be selected by the P0PLUD register, P1PLUD register, P6PLUD register and PAPLU register. For timer output, PWM signal output, select the special function pin by port 0 output mode register, port 1 output mode register, port 6 output mode register and port A output mode register ((P0OMD, P1OMD, P6OMD and PAOMD), and set to the output mode at P0DIR register, P1DIR register and PADIR register. These can be used as normal I/O pins when the timer I/O is not used.
RMOUTA RMOUTB RMOUTC	1 25 35	I/O	TM0IOA,AN0,PA0 TM0IOB,TM2IOB,LED3,P03 P10,SEG49,TM0IOC	Remote control transmission signal output pins	Output pin for remote control transmission with a carrier signal. For remote control carrier output, select the special function pin by the port 0 output mode register, port 1 output mode register and port A output mode register (P0OMD, P1OMD and PAOMD), and set to the output mode by the P0DIR register, P1DIR register and PADIR register. At the same time, select remote control carrier output by the remote control carrier output register. These can be used as normal I/O pins when the buzzer output is not used.
BUZZERA BUZZERB NBUZZERA NBUZZERB	61 40 60 41	I/O	P53,SEG23,KEY3,D3 P15,SEG44,TM7IOC P54,SEG24,KEY4,D4 P16,SEG43,TM8IOC	Buzzer output	Piezoelectric buzzer driving pin. Buzzer output available to port1, port5. The driving frequency can be selected with the DLYCTR register. To select buzzer output for porrt1, port5, select the special function pin by the port 1 output mode register and port 5 output mode register (P1OMD and P5OMD), and set to the output mode by the P1DIR register and P5DIR register. At the same time, select buzzer output by the oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when the buzzer output is not used.

Name	NO	I/O	Other Function	Function	Description
TM7IOA TM7IOB TM7IOC TM8IOA TM8IOB TM8IOC TM9IOA TM9IOB	6 22 40 7 23 41 8 24	I/O	AN5,PA5 RXD1A,SBI1A,LED0,P00 P15,SEG44,BUZZERB AN6,PA6 TXD1A,SBO1A,LED1,P01 P16,SEG43,NBUZZERB AN7,PA7 SBT1A,LED2,P02	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7 and 8. To use this pin as event clock input, configure this as input with the PADIR register. In the input mode, pull-up resistors can be selected by P0PLU register, P1PLU register and PAPLU register. For timer output, PWM signal output, select the special function pin by the port 0 output mode register, port 1 output mode register and port A output mode register (P0OMD, P1OMD and PAOMD), and set to the output mode at P0DIR register, P1DIR register and PADIR register. These can be used as normal I/O pins when not used as timer I/O pins.
TM9OD0 TM9OD1 TM9OD2 TM9OD3 TM9OD4 TM9OD5	81 82 83 84 85 86	output	SDO0,A11,SEG3,P80 SDO1,A12,SEG2,P81 SDO2,A13,SEG1,P82 SDO3,A14,SEG0,P83 SDO4,A15,COM0,P84 SDO5,A16,COM1,P85	Timer output pins	Timer output and PWM signal output pin for 16-bit timer. To select timer output and PWM signal output, select the special function pin by the P8OMD1 register, and set to the output mode at the P8DIR register. These can be used as normal I/O pins when not used as timer I/O pins.
SDO0 SDO1 SDO2 SDO3 SDO4 SDO5 SDO6 SDO7	81 82 83 84 85 86 87 88	output	TM9OD0,A11,SEG3,P80 TM9OD1,A12,SEG2,P81 TM9OD2,A13,SEG1,P82 TM9OD3,A14,SEG0,P83 TM9OD4,A15,COM0,P84 TM9OD5,A16,COM1,P85 A17,COM2,P86 A18,COM3,P87	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 8 synchronous output control register (P8SYO). Set to the output mode by the P8DIR register. These pins can be used as a normal I/O pins when not used for synchronous output pin.
V_{REF+}	100	-		+ power supply for A/D converter	Reference power supply pins for the A/D converter. Use this under the condition: 2.0 V ≤ V_{REF+} ≤ V_{DD5}
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7 AN8 AN9 AN10 AN11	1 2 3 4 5 6 7 8 100 99 98 97	input	RMOUTA,TM0IOA,PA0 TM1IOA,PA1 TM2IOA,PA2 TM3IOA,PA3 TM4IOA,PA4 TM7IOA,PA5 TM8IOA,PA6 TM9IOA,PA7 PB0 PB1 PB2 PB3	Analog input pins	Analog input pins for an 16-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
DA_A DA_B DA_C DA_D	29 66 91 92	output	P07,LED7 P61,SEG18 V_{LC1},P94 P95	Analog output pins	Analog output pins for an 4-channel, 8-bit A/D converter. When not used for analog output, these pins can be used as normal I/O pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4	30 31 32 33 34	input	P20,SEG54 P21,SEG53,ACZ1 P22,SEG52 P23,SEG51 P24,SEG50	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 4 can be selected with the IRQnICR register. IRQ1 has AC zero-cross detection function. IRQ1 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins.

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Name	NO	I/O	Other Function	Function	Description
ACZ1	31	input	P21,SEG53,IRQ1	AC zero-cross detection input pins	AC zero-cross detection input pin. AC zero-cross detection output “H” when input level is mid-level and “L” otherwise. ACZ input signal is connected to P20 input and IRQ0 interrupt circuit or P21 input and IRQ1 interrupt circuit. When not used for AC zero-cross detection, these can be used as normal input pins.
ACZ0	30		P20,SEG54,IRQ0		
KEY0	64	input	P50,SEG20,D0,SBO0A, TXD0A	Key interrupt input pins	Input pins for interrupt based on OR result of pin inputs. These can be set to key input pins by 1-bit with the key interrupt control register (KEYT3_1IMD, KEYT3_2IMD) and by 2-bit with the key interrupt control register (KEYT3_1IMD). When not used for KEY input, these pins can be used as normal I/O pins.
KEY1	63		P51,SEG21,D1,SBI0A, RXD0A		
KEY2	62		P52,SEG22,D2,SBT0A		
KEY3	61		P53,SEG23,D3,BUZZERA		
KEY4	60		P54,SEG24,D4,NBUZZERA		
KEY5	59		P55,SEG25,D5		
KEY6	58		P56,SEG26,D6		
KEY7	57		P57,SEG27,D7		
LED0	22	I/O	RXD1A,SBI1A,TM7IOB,P00	LED drive pins	Large current output pins. When not used for LED output, these pins can be used as normal I/O pins.
LED1	23		TXD1A,SBO1A,TM8IOB,P01		
LED2	24		SBT1A,TM9IOB,P02		
LED3	25		RMOUTB,TM0IOB,TM2IOB, P03		
LED4	26		P04,SBO3A,TXD3A		
LED5	27		P05,SBI3A,RXD3A		
LED6	28		P06,SBT3A		
LED7	29		P07,DA_A		
NWE	75	output	P72,SEG9,SBT2A	Write enable pins [Active low]	Memory control signal used when the memory area is expanded to the external of this LSI. NWE is the strobe signal output for the write operation of the external memory and NRE is the strobe signal output for the read operation of the external memory NCS is the chip selection signal outputs the external memory at the access. NDK is the acknowledge signal that indicates close of access to the external memory.
NRE	76		SDA5A,SEG8,P73	Read enable pins [Active low	
NCS	77		SCL5A,SEG7,P74	Chip select pins [Active low]	
NDK	90	input	V_{LC2},P93	Data acknowledge pins [Active low]	
A0	67	output	P62,SEG17,TM1IOB	Address pin	A0-A19 is the address signal to the external memory. D0-D7 is the data I/O signal to the external memory.
A1	68		P63,SEG16,TM3IOB		
A2	69		P64,SEG15,TM4IOB		
A3	70		P65,SEG14,SBI4A		
A4	71		P66,SEG13,SBO4A,SDA4A		
A5	72		P67,SEG12,SBT4A,SCL4A		
A6	73		P70,SEG11,SBO2A,TXD2A		
A7	74		P71,SEG10,SBI2A,RXD2A		
A8	78		TXD1B,SBO1B,SEG6,P75		
A9	79		RXD1B,SBI1B,SEG5,P76		
A10	80		SBT1B,SEG4,P77		
A11	81		TM9OD0,SDO0,SEG3,P80		
A12	82		TM9OD1,SDO1,SEG2,P81		
A13	83		TM9OD2,SDO2,SEG1,P82		
A14	84		TM9OD3,SDO3,SEG0,P83		
A15	85		TM9OD4,SDO4,COM0,P84		
A16	86		TM9OD5,SDO5,COM1,P85		
A17	87		SDO6,COM2,P86		
A18	88		SDO7,COM3,P87		
A19	89		V_{LC3},P92		

(Continue to next page)

Name	NO	I/O	Other Function	Function	Description
D0	64	I/O	P50,SEG20,KEY0,SBO0A, TXD0A	Data pin	(Continued from previous page)
D1	63		P51,SEG21,KEY1,SBI0A, RXD0A		
D2	62		P52,SEG22,KEY2,SBT0A		
D3	61		P53,SEG23,KEY3,BUZZERA		
D4	60		P54,SEG24,KEY4,NBUZZERA		
D5	59		P55,SEG25,KEY5		
D6	58		P56,SEG26,KEY6		
D7	57		P57,SEG27,KEY7		
COM0	85	Output	TM9OD4,SDO4,A15,P84	LCD common output pins	These pins output common signal of required timing for LCD display. Connect to the common pins of LCD display panel. When the LCD functions are not used, these pins can be used as normal I/O port by the setting the LCD output control register LCCTR0.
COM1	86		TM9OD5,SDO5,A16,P85		
COM2	87		SDO6,A17,P86		
COM3	88		SDO7,A18,P87		
V_{LC1}	91	-	SYSCLK,DA_C,P94	LCD power supply pins	Supply for LCD power. Apply 5.5 $V \geq V_{LC1} \geq V_{LC2} \geq V_{LC3} \geq 0$ V. When the internal voltage divider resistor is used, $V_{LC1}=V_{DD5}$ pin is selected as the reference voltage input pin. When LCD is not used, V_{LC1} to V_{LC3} can be used as normal I/O pins with the setting of LCD output control register0 (LCCTR0).
V_{LC2}	90		NDK,P93		
V_{LC3}	89		A19,P92		
SEG0	84	output	TM9OD3,SDO3,A14,P83	LCD segment output pinas	These pins output segment signal of required timing for LCD display. Connect to the segment pins of the LCD display panel. When LCD display is turned off, V_{ss} level is output. These pins can be used as normal I/O pins with the setting of LCD output control register LCCTR1 to 7. SEG can exchange segment pins and normal port by each bit.
SEG1	83		TM9OD2,SDO2,A13,P82		
SEG2	82		TM9OD1,SDO1,A12,P81		
SEG3	81		TM9OD0,SDO0,A11,P80		
SEG4	80		SBT1B,A10,P77		
SEG5	79		RXD1B,SBI1B,A9,P76		
SEG6	78		TXD1B,SBO1B,A8,P75		
SEG7	77		SCL5A,NCS,P74		
SEG8	76		SDA5A,NRE,P73		
SEG9	75		P72,NWE,SBT2A		
SEG10	74		P71,A7,SBI2A,RXD2A		
SEG11	73		P70,A6,SBO2A,TXD2A		
SEG12	72		P67,A5,SBT4A,SCL4A		
SEG13	71		P66,A4,SBO4A,SDA4A		
SEG14	70		P65,A3,SBI4A		
SEG15	69		P64,A2,TM4IOB		
SEG16	68		P63,A1,TM3IOB		
SEG17	67		P62,A0,TM1IOB		
SEG18	66		P61,DA_B		
SEG19	65		P60		
SEG20	64		P50,KEY0,D0,SBO0A,TXD0A		
SEG21	63		P51,KEY1,D1,SBI0A,RXD0A		
SEG22	62		P52,KEY2,D2,SBT0A		
SEG23	61		P53,KEY3,D3,BUZZERA		
SEG24	60		P54,KEY4,D4,NBUZZERA		
SEG25	59		P55,KEY5,D5		
SEG26	58		P56,KEY6,D6		
SEG27	57		P57,KEY7,D7		
SEG28	56		P47,SCL5B		
SEG29	55		P46,SDA5B		
SEG30	54		P45,SBT0B		
SEG31	53		P44,SBI0B,RXD0B		(Continue to next page)

Name	NO	I/O	Other Function	Function	Description
SEG32	52		P43,SBO0B,TXD0B		(Continued from previous page)
SEG33	51		P42,SBT3B		
SEG34	50		P41,SBI3B,RXD3B		
SEG35	49		P40,SBO3B,TXD3B		
SEG36	48		P36		
SEG37	47		P35,SBI4B		
SEG38	46		P34,SBT4B,SCL4B		
SEG39	45		P33,SBO4B,SDA4B		
SEG40	44		P32,SBT2B		
SEG41	43		P31,SBI2B,RXD2B		
SEG42	42		P30,SBO2B,TXD2B		
SEG43	41		P16,TM8IOC,NBUZZERB		
SEG44	40		P15,TM7IOC,BUZZERB		
SEG45	39		P14,TM4IOC		
SEG46	38		P13,TM3IOC		
SEG47	37		P12,TM1IOC		
SEG48	36		P11,TM2IOC		
SEG49	35		P10,TM0IOC,RMOUTC		
SEG50	34		P24,IRQ4		
SEG51	33		P23,IRQ3		
SEG52	32		P22,IRQ2		
SEG53	31		P21,IRQ1,ACZ1		
SEG54	30		P20,IRQ0		
MMOD	10	input		Memory mode switch input pins	Set always to V_{SS}.
DMOD	21	input		Mode switch input pins	Set always to V_{DD5}.

1.4 Block Diagram

1.4.1 Block Diagram

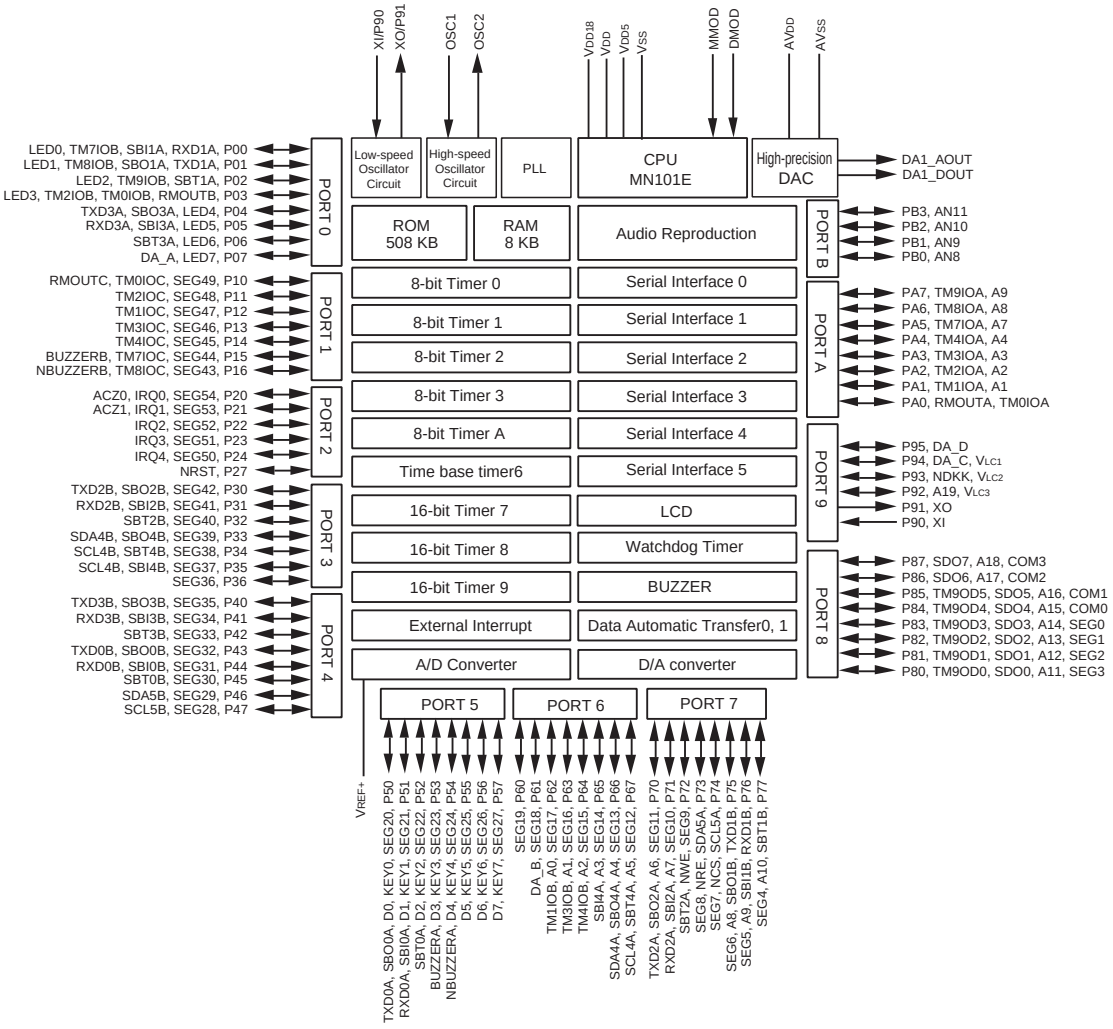

Figure:1.4.1 Block Diagram

* Depending on the models. See [[1.1.2 Product Summary]]

1.5 Electrical Characteristics

This LSI manual describes the standard specification.

Please ask our sales offices for the product specifications.

Model	MN101E30	
Contents	Structure	CMOS integrated circuit
	Application	General purpose
	Function	CMOS, 8-bit, single chip micro controller

1.5.1 Absolute Maximum Ratings *2 *3

V_{SS} = 0 V

	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD5}	-0.3 to +7.0	V
2	Capacity connection pin		V_{DD18}	-0.3 to +2.5	
3	*4		V_{DD}	-0.3 to +4.6	
4	Input clamp current (ACZ)		I_C	-500 to +500	µA
5	Input pin voltage		V_I	-0.3 to V_{DD5} + 0.3	V
6	Output pin voltage		V_O	-0.3 to V_{DD5} + 0.3	
7	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} + 0.3	
8	Peak power current	P0	I_{OL1} (peak)	30	mA
9		Other than P0	I_{OL2} (peak)	20	
10		All pins	I_{OH} (peak)	-10	
11	Average output current *1	P0	I_{OL1} (avg)	20	
12		Other than P0	I_{OL2} (avg)	15	
13		All pins	I_{OH} (avg)	-5	
14	Power dissipation		P_T	400	mW
15	Operating ambient temperature		T_{opr}	-40 to +85	°C
16	Storage temperature		T_{stg}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect approximate 1 µF capacitor between V_{DD18}/V_{DD} power supply pin and the ground, and approximate 10-times capacitor connect to V_{DD18}/V_{DD} between V_{DD5} power supply pin and the ground for the internal power supply stabilization.

*3 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

*4 Applied only in Flash version.

1.5.2 Operating Conditions

V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter		Symbol	Condition	Rating			Unit
					MIN	TYP	MAX	
Power supply voltage *4								
1	Power supply voltage	In not using PLL	V_{DD5-1}	fosc ≤ 20 MHz [Double speed mode: fs ≤ 20 MHz]	2.2		5.5	V
2		In using PLL	V_{DD5-2}	4.0 MHz ≤ fosc ≤ 10 MHz [Multiplied by 2 to 10: fs ≤ 20 MHz]	2.2		5.5	
3			V_{DD5-3}	fx=32.768 kHz [Normal mode: fs≤fx/2]	2.2		5.5	
4	Voltage to maintain RAM data		V_{DD5-4}	[During STOP mode]	1.8		5.5	
Operating speed *5								
5	Instruction execution time		t_{c1}	V_{DD5}=2.2 V to 5.5 V	0.05			µs
6			t_{c2}	V_{DD5}=2.2 V to 5.5 V	61			

*4 fosc: Input clock frequency to OSC1 pin.
fx: Input clock frequency to XI pin

*5 t_{c1}: In the case of OSC1 as CPU clock, or OSC1 multiplied by PLL as CPU clock.
t_{c2}: In the case of XI as CPU clock.

Use LCD power supply voltage with $V_{LC1} \leq V_{DD5}$.

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Condition	Rating			Unit
				MIN	TYP	MAX	
Crystal oscillator 1 Figure:1.5.1 [NORMAL mode]							
7	Crystal frequency	f_{xtal1}	V_{DD5} = within the operation power supply voltage (Refer to the reference value of power supply voltage 1 to 3.)	2.0		20	MHz
8	External capacitors	C_{11}			10		pF
9		C_{12}			10		
10	Internal feedback resistor	R_{f10}	V_{DD5}=5.0 V		950		kΩ
Crystal oscillator 2 Figure:1.5.2 [SLOW mode]							
11	Crystal frequency	f_{xtal2}	V_{DD5}=2.2 V to 5.5 V		32.768		kHz
12	External capacitors	C_{21}			4		pF
13		C_{22}			4		
14	Internal feedback resistor	R_{f20}	V_{DD5}=5.0 V		6		MΩ

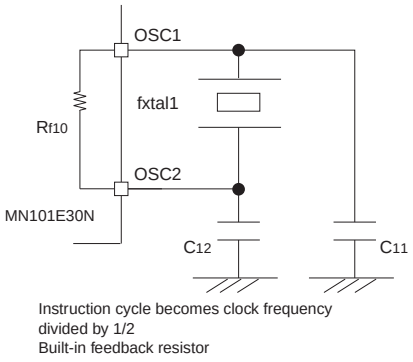

Figure:1.5.1 Crystal oscillator 1

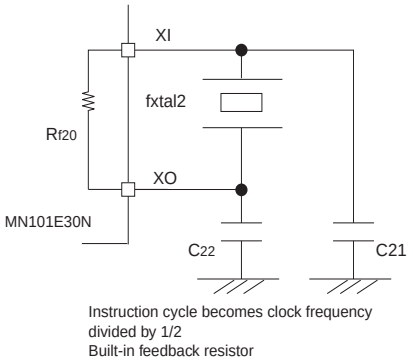

Figure:1.5.2 Crystal oscillator 2

Connect external capacitors that suits the used pin. When crystal oscillator or ceramic oscillator is used, the frequency is changed depending on the condenser rate. Therefore, consult the manufacturer of the pin for the appropriate external capacitor.

V_{DD5} = 2.2 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Condition	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
15	Clock frequency	f_{OSC1}		1.0		20.0	MHz
16	High level pulse width *6	t_{wh1}	Figure:1.5.3	22.5			ns
17	Low level pulse width *6	t_{wl1}		22.5			
18	Rising time *7	t_{wr1}	Figure:1.5.3	0		5.0	
19	Falling time *7	t_{wf1}		0		5.0	
External clock input 2 XI (XO is unconnected)							
20	Clock frequency	f_{OSC2}			32.768		kHz
21	High level pulse width *6	t_{wh2}	Figure:1.5.4		4.5		µs
22	Low level pulse width *6	t_{wl2}			4.5		
23	Rising time *7	t_{wr2}	Figure:1.5.4	0		20	ns
24	Falling time *7	t_{wf2}		0		20	

*6 The clock duty rate in the standard mode should be 45 % to 55 %

*7 Rising time and falling time differ depending on oscillation frequency.
This is noted that the maximum value is a rough value, not a specified value.
Consult the oscillator manufacturer and perform matching tests for determining appropriate values.

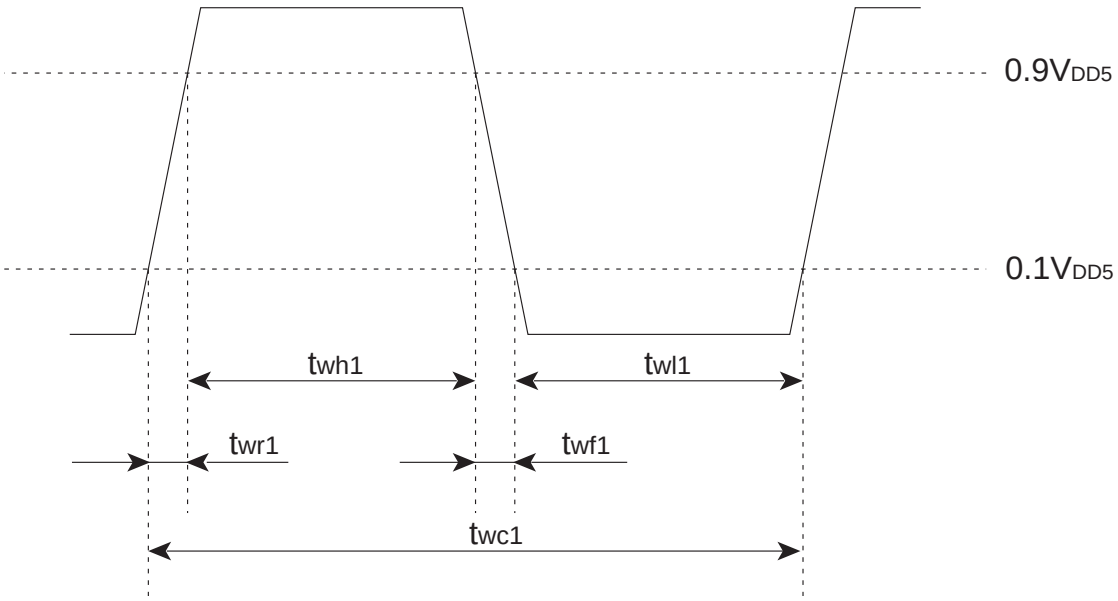

Figure:1.5.3 OSC1 Timing Chart

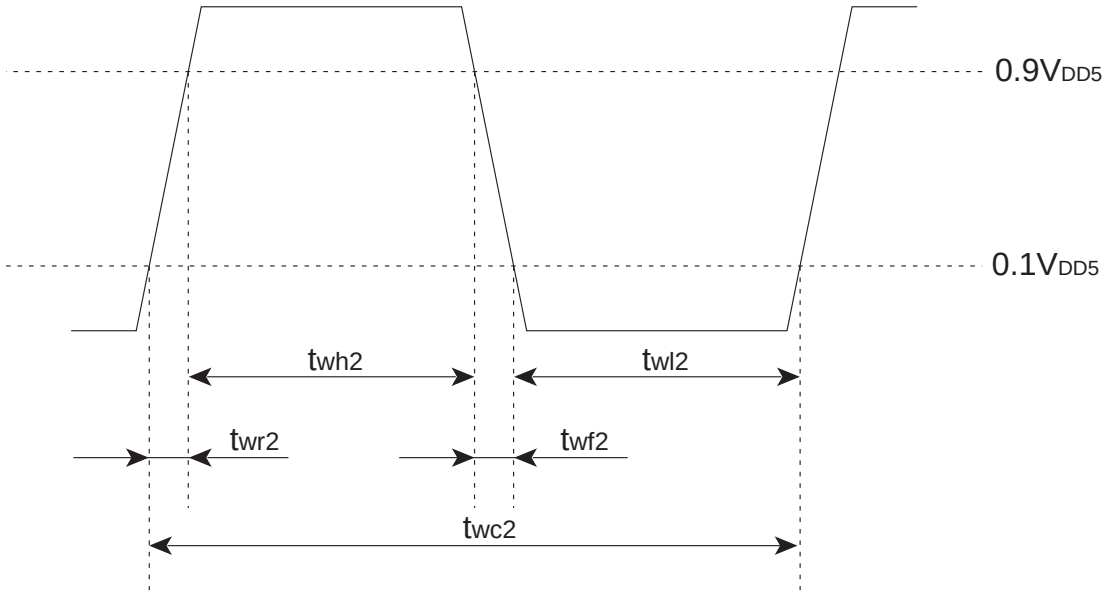

Figure:1.5.4 XI Timing Chart

1.5.3 DC Characteristics

V_{SS}=0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current *8 (NORMAL mode: fs=fosc/2 SLOW mode: fs=fx/2)							
1	Power supply current	I_{DD1}	fosc=20 MHz [Double-speed mode: fs=fosc] V_{DD5}=5 V (In not using PLL)		4 (9)	8 (18)	mA
2		I_{DD2}	fosc=4 MHz [Multiplied by 5: fs=20 MHz] V_{DD5}=5 V (In using PLL)		4 (10)	8 (20)	
3		I_{DD}	fosc=8 MHz [Double-speed mode: fs=fosc] V_{DD5}=5 V (In not using PLL)		1.5 (5)	3 (9)	
4		I_{DD4}	fosc=4 MHz [Double-speed mode: fs=fosc] V_{DD5}=5 V (In not using PLL)		1 (3)	2 (6)	
5		I_{DD5}	fx=32.768 MHz, [fs=fx/2] V_{DD5}=3 V Ta=25 °C		5 (60)	20 (120)	µA
6		I_{DD6}	fx=32.768 MHz, [fs=fx/2] V_{DD5}=3 V Ta=85 °C			75 (200)	
7	Supply current during HALT1 mode	I_{DD7}	fx=32.768 MHz V_{DD5}=3 V Ta=25 °C		4 (6)	13 (18)	
8		I_{DD8}	fx=32.768 kHz V_{DD5}=3 V Ta=85 °C			70 (80)	
9	Supply current during STOP mode	I_{DD9}	V_{DD5}=5 V Ta=25 °C		1 (2)	6 (7)	
10		I_{DD10}	V_{DD5}=5 V Ta=85 °C			60 (60)	

*8 Measured under condition without load. (pull-up / pull-down resistors are unconnected.)

- The supply current during operation, I_{DD1} to I_{DD4} are measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and a 20 MHz square wave of V_{DD5} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD5} and I_{DD6} are measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and a 32.768 kHz square wave of V_{DD5} and V_{SS} amplitudes is input to the XI pin.
- The supply current during HALT1 mode, I_{DD7} and I_{DD8} are measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <HALT1 mode>, the input pins are at V_{DD5} level, and an 32.768 kHz square wave of V_{DD5} and V_{SS} amplitudes is input to the XI pin.
- The supply current during STOP mode, I_{DD9} and I_{DD10} are measured under the following conditions:
  After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and the OSC1 and XI pins are unconnected.
- The values in parentheses are for Flash version.

V_{DD5}=2.2 V to 5.5 V V_{SS}=0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 MMOD, DMOD, ATRST							
11	Input high voltage	V_{IH1}		0.8V_{DD5}		V_{DD}	V
12	Input low voltage	V_{IL1}		0		0.2V_{DD5}	
13	Input leakage current	I_{LK1}	V_{IN}=0 V to V_{DD5}			± 2	µA
I/O pin 2 P27 (NRST)							
14	Input high voltage	V_{IH2}		0.8V_{DD5}		V_{DD5}	V
15	Input low voltage	V_{IL2}		0		0.15V_{DD5}	
16	Pull-up resistor	R_{RH1}	V_{DD5}=5.0V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
I/O pin 3 P10 to P16, P20 to P24, P30 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P77							
17	Input high voltage	V_{IH3}		0.8V_{DD5}		V_{DD5}	V
18	Input low voltage	V_{IL3}		0		0.2V_{DD5}	
19	Input leakage current	I_{LK2}	V_{IN}=0 V to V_{DD5}			± 2	µA
20	Pull-up resistor	R_{RH2}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
21	Pull-down resistor	R_{RH1}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-down resistor ON	10	50	100	
22	Output high voltage	V_{OH1}	V_{DD5}=5.0 V I_{OH}=-0.5 mA	4.5			V
23	Output low voltage	V_{OL1}	V_{DD5}=5.0 V I_{OL}=1.0 mA			0.5	

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V_{DD5}=2.2 V to 5.5 V V_{SS}=0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 4 P80 to P87, P90 to P95, PA0 to PA7, PB0 to PB3							
24	Input high voltage	V_{IH4}		0.8V_{DD5}		V_{DD5}	V
25	Input low voltage	V_{IL4}		0		0.2V_{DD5}	
26	Input leak current	I_{LK3}	V_{IN}=0 V to V_{DD5}			± 2	µA
27	Pull-up resistor	R_{RH3}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
28	Output high voltage	V_{OH2}	V_{DD5}=5.0 V I_{OH}=0.5 mA	4.5			V
29	Output low voltage	V_{OL2}	V_{DD5}=5.0 V I_{OL}=1.0 mA			0.5	
I/O pin 5 P00 to P07							
30	Input high voltage1	V_{IH5}		0.8V_{DD5}		V_{DD5}	V
31	Input low voltage1	V_{IL5}		0		0.2V_{DD5}	
32	Input leak current	I_{LK4}	V_{IN}=0 V to V_{DD5}			± 2	µA
33	Pull-up resistor	R_{RH4}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
34	Pull-down resistor	R_{RL2}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-down resistor ON	10	50	100	
35	Output high voltage	V_{OH3}	V_{DD5}=5.0 V I_{OH}=0.5 mA	4.5			V
36	Output low voltage1	V_{OL3}	V_{DD5}=5.0 V I_{OL}=1.0 mA LED output OFF			0.5	
37	Output low voltage2	V_{OL4}	V_{DD5}=5.0 V I_{OL}=15 mA LED output ON			1.0	

V_{DD5}=2.2 V to 5.5 V V_{SS}=0 V
Ta=-40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
I/O pin 6 P20 (during used as ACZ) and P21 (during used as ACZ) are regulated at 5.0 V							
38	Input high voltage1	V_{DHH}	Figure:1.5.5	4.5			V
39	Input high voltage2	V_{DHL}		1.5			
40	Input low voltage1	V_{DLH}				3.5	
41	Input low voltage2	V_{DLL}				0.5	
42	Input clamp current	I_{C3}	$V_{IN} > V_{DD5}$, $V_{IN} < 0$ V			±500	μA
Display output pin 1 COM0 to COM3 (At V_{LC1}, V_{SS} Voltage output) *9							
43	Output high voltage (In V_{LC1} voltage output)	V_{OCOMH}	V_{DD5}=V_{LC1}=5.0 V I_{COM}= -10 μA	4.4			V
44	Output low voltage (In V_{SS} voltage output)	V_{OCOML}	V_{DD5}=V_{LC1}=5.0 V I_{COM}=10 μA			0.6	
Display output pin 2 SEG0 to SEG54 (At V_{LC1}, V_{SS} Voltage output) *10							
45	Output high voltage (In V_{LC1} voltage output)	V_{OSEGH}	V_{DD5}=V_{LC1}=5.0 V I_{SEG}= -2 μA	4.4			V
46	Output low voltage (In V_{SS} voltage output)	V_{OSEGL}	V_{DD5}=V_{LC1}=5.0 V I_{SEG}=2 μA			0.6	
Display power pin 1 V_{LC1}, V_{LC2}, V_{LC3}							
47	Internal dividing resistor	R_{VL1}	Ta=+25 °C *11 (Impedance between V_{LC1} and V_{SS})	142.5	300	570	kΩ
48		R_{VL2}		15	30	60	

*9 However, COM0 to COM3 are also used as P84 to P87.

*10 However, SEG0 to SEG54 are also used as P10 to P16, P20 to P24, P30 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P77and P80 to 83.

*11 Summation of 3 resistors among V_{LC1} and V_{LC2}, V_{LC2} and V_{LC3}, V_{LC3} and V_{SS}

1.5.4 A/C Converter Characteristics

V_{DD5}=5.0 V V_{SS}=0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
ACZ1 pin							
1	Rising time	t_{rs}	Figure:1.5.5	30			µs
2	Falling time	t_{fs}		30			

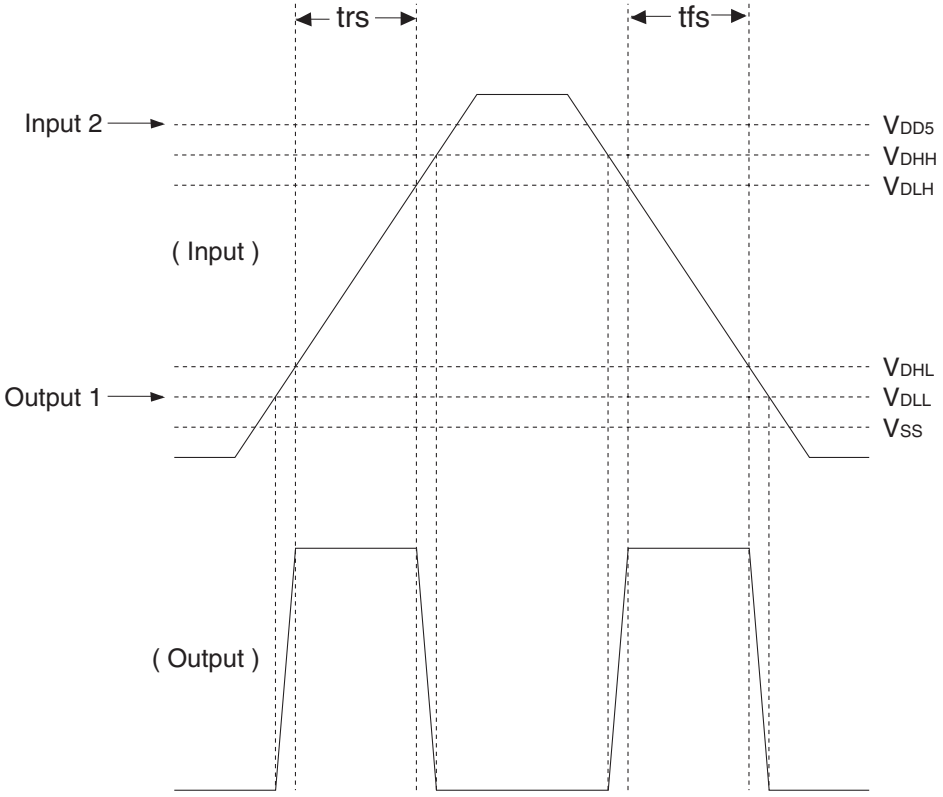

Figure:1.5.5 Operation of AC Zero-Cross Detection Circuit

1.5.5 A/D Converter Characteristics

V_{DD5}=5.0 V V_{SS}=0 V
Ta=-40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	Bits
2	Non-linearity error 1		V_{DD5}=5.0 V, V_{SS}=0 V V_{ref+}=5.0 V T_{AD}=800 ns *12			±3	LSB
3	Differential linearity error 1					±3	
4	Zero transition voltage		V_{DD5}=5.0 V, V_{SS}=0 V V_{ref+}=5.0 V T_{AD}=800 ns *12	-30	10	30	mV
5	Full-scale transition voltage			4970	4990	5030	
6	A/D conversion time		T_{AD}=800 ns *12	12.93			µs
7			fx=32.768 kHz T_{AD}=15.2 µs *12	427.25			
8	Sampling time		T_{AD}=800 ns *12	1.6			
9			fx=32.768 kHz T_{AD}=15.2 µs *12	30.52			
10	Reference voltage	V_{ref+}	Note)	2.0		V_{DD5}	V
11	Analog input voltage			V_{SS}		V_{ref+}	
12	Analog input leakage current		When channel is OFF V_{ADIN}=0 V to 5.0 V			±2	µA
13	Reference voltage pin input leakage current		When V_{REF+} is OFF $V_{ss} \leq V_{REF+} \leq V_{DD5}$			±5	
14	Ladder resistance	R_{LADD}	V_{DD5}=5.0 V	15	40	80	kΩ

*12 T_{AD} is A/D conversion clock cycle.
The values of 2 to 5 are guaranteed on the condition that V_{DD5}=V_{ref+}=5 V, V_{SS}=0 V.

Note) The voltage difference between V_{REF+} and V_{SS} should be set to more than 2 V.

The reference voltage input to V_{REF+} pin should be used on the condition of 2.0 V ≤ V_{REF+} ≤ V_{DD5} to avoid the malfunctions of microcomputer.

1.5.6 D/A Converter Characteristics

V_{DD5}=5.0 V V_{SS}=0 V
Ta=25 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution			-	-	8	Bits
2	Reference voltage low level	D_{AVSS}		V_{SS}	-		V
3	Reference voltage high level	D_{AVDD}			-	V_{DD5}	
4	Zero scale output voltage	V_{ZS}	V_{DD5}=5.0 V, V_{SS}=0 V D7 to D0=ALL "L"	-0.05	0	0.05	
5	Full scale output voltage	V_{FS}	V_{DD5}=5.0 V, V_{SS}=0 V D7 to D0=ALL "H"	4.93	4.98	5.03	
6	Analog output resistance (Minimum reference resistance)	R_{OAT}		5	10	15	kΩ
7	Non-linearity error	N_{LE}	V_{DD5}=5.0 V, V_{SS}=0 V	-	± 2.0	± 3.0	LSB
8	Differential non-linearity error	D_{NLE}	V_{DD5}=5.0 V, V_{SS}=0 V	-	± 2.0	± 3.0	
9	Settling time	T_{SET}	External capacitor CL=15 pF All bits are set to ON or OFF	-	1.5	3.0	µs

1.5.7 Auto Reset Characteristics

$V_{DD5}=V_{RST}$ to 5.5 V V_{SS}=0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
1	Operation voltage	V_{DD7}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
2	Power supply detection level	V_{RST}		3.7		4.5	V
3	Supply voltage change rate	$\Delta t/\Delta V$		250			µs/V
Power supply current							
4	Auto reset power consumption	I_{DD7}	V_{DD5}=5 V		220	330	µA

1.5.8 Audio Output Characteristics

V_{DD5}=AV_{DD}=5.5 V V_{SS}=0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Output pin 7 DA1_AOUT							
1	Power supply voltage	AV_{DD}	AV_{DD}=V_{DD5}	4.5		5.5	V
2	Signal-to-noise ratio	S/N	AV_{DD}=5 V (Note1)	80	88		dB
3	Dynamic range	D.R.	AV_{DD}=5 V (Note1)	70	78		dB
4	Total harmonic distortion ratio	THD+N	AV_{DD}=5 V (Note1)		0.16	0.26	%
5	Output impedance	R_{AOUT}	AV_{DD}=5 V	0.25		2.0	kΩ
Output pin 8 DA1_DOUT							
6	Output voltage high level	V_{OH2}	V_{DD5}=5.0 V I_{OH}=-2 mA	4.5			V
7	Output voltage low level	V_{OL2}	V_{DD5}=5.0 V I_{OL}=2.0 mA			0.5	

(Note1) This is the value sampling 1kHz SIN wave at 20kHz and recording with 16bit-PCM.

(Note2) H2,H3 and H4 are the output level at the measuring point on the audio charactoristic measuring curcuit(Figure:1.5.6).

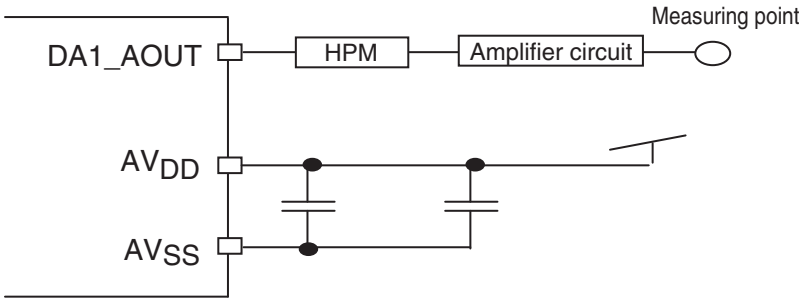

Figure:1.5.6 Audio Characteristic Measuring Circuit (a)

AV_{DD} and V_{DD5} should be at the same electric potential regardless of whether or not the audio production function is used.

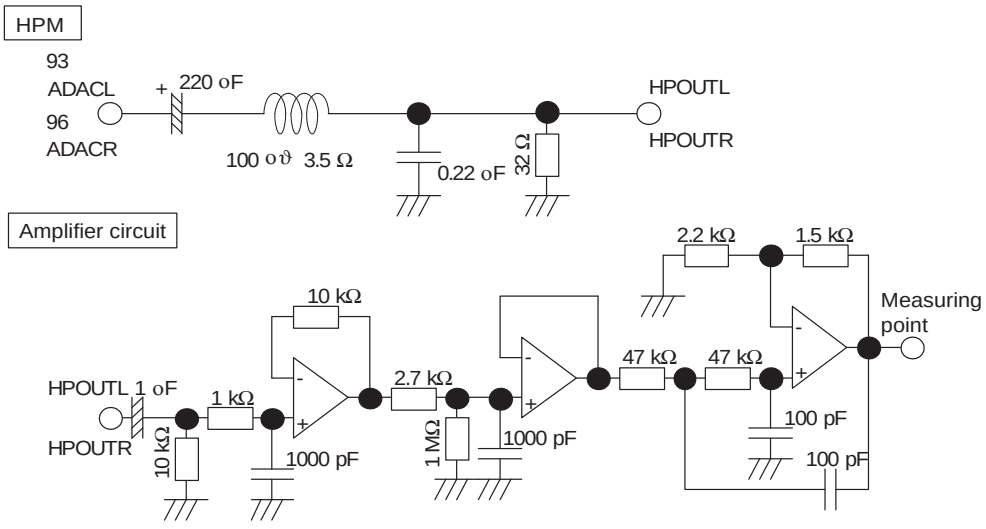

Figure:1.5.7 Audio Characteristic Measuring Circuit (b)

1.5.9 Flash EEPROM Program Condition

	Item	Symbol	Condition	Rating			Unit
				MIN	TYP	MAX	
1	Programming voltage level	V_{DD5-6}		2.7		5.5	V
2	Data retention period	Thold		10			Years
3	Programming guarantee number times	E_{MAX}				1000	Times

1.6 Package Dimension

Units: mm

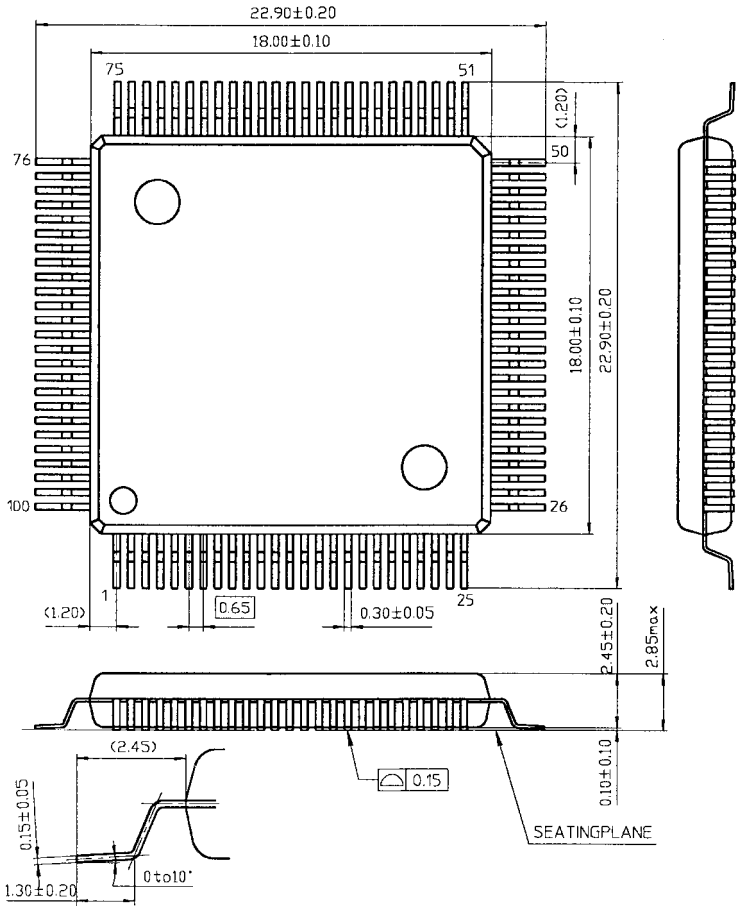

Figure:1.6.1 Package Dimension (QFP100-P-1818B)

Sealing material:	EPOXY resin
Lead material :	Cu alloy
Lead surface processing :	Pd plating

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

Units: mm

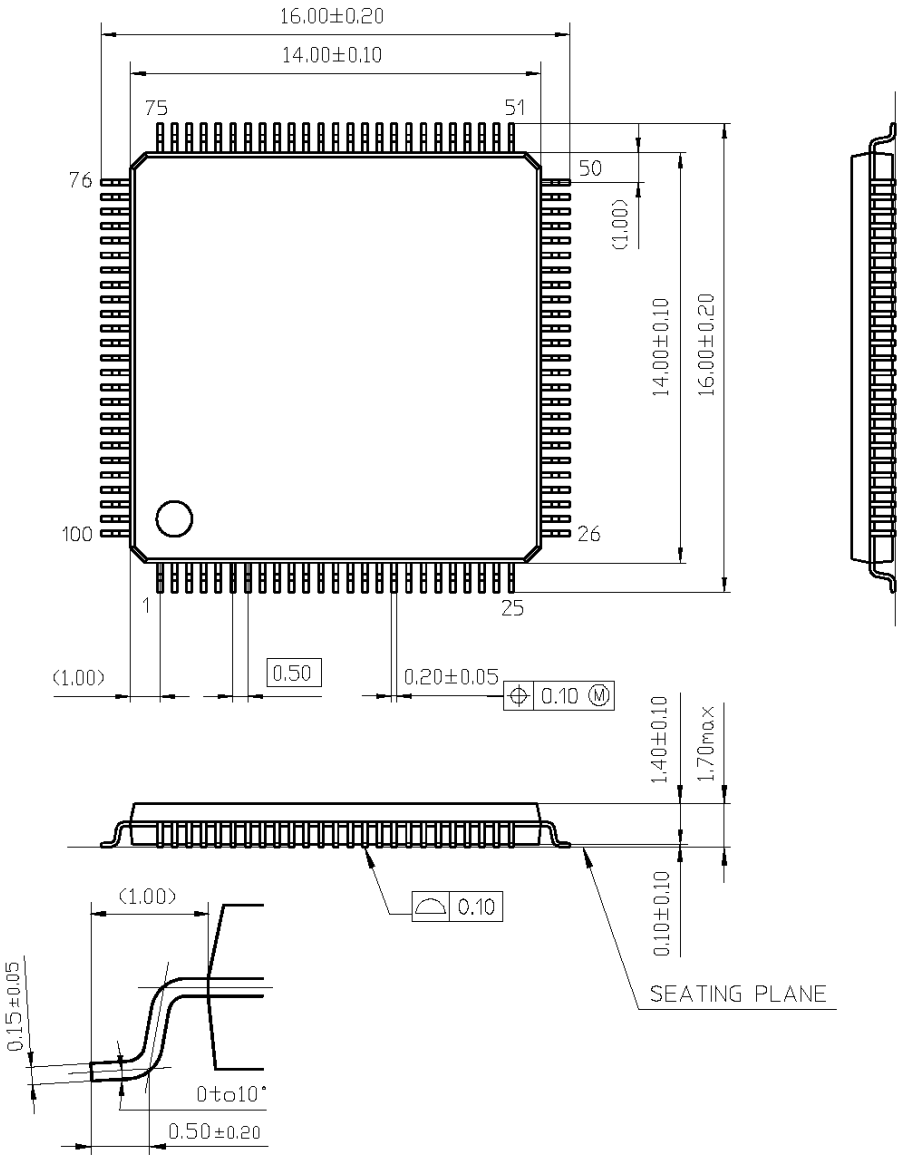

Figure:1.6.2 Package Dimension (LQFP100)

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

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