

Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

※ Except below description page

"Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan

| | | | |
|-----------------------|----------------------------------------|---------|--------|
| Type | Silicon MOSFET type Integrated Circuit | | |
| Application | For Switching Power Supply Control | | |
| Structure | CMOS type | | |
| Circuit Block Diagram | Figure 8 | | |
| Out Line | DIP7-A1-B | Marking | MIP2M2 |

A. ABSOLUTE MAXIMUM RATINGS (Ta=25°C±3°C)

| NO. | Item | Symbol | Ratings | Unit | Note |
|-----|-----------------------------------|--------|------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | DRAIN Voltage | VD | -0.3 ~ 700 | V | VFB is guaranteed at VDD=6 V. VSO is guaranteed at VSO=VDD. ※ 1: IDP is guaranteed at the pulse width narrower than ton(BLK) + td(OCL) |
| 2 | VCC Voltage | VCC | -0.3 ~ 45 | V | |
| 3 | VDD Voltage | VDD | -0.3 ~ 9 | V | |
| 4 | FB Voltage | VFB | -0.3 ~ 6.4 | V | |
| 5 | FB Current | IFB | -500 | μA | |
| 6 | LS Voltage | VLS | -0.3 ~ 9 | V | |
| 7 | SO Voltage | VSO | -0.3 ~ 9 | V | |
| 8 | Output Peak Current | IDP | 0.76(※1) | A | |
| 9 | Recommended Operating Temperature | Tj | -30 ~ +125 | °C | |
| 10 | Channel Temperature | Tch | 150 | °C | |
| 11 | Storage Temperature | Tstg | -55 ~ +150 | °C | |



B. ELECTRICAL CHARACTERISTICS Measure condition (TC=25°C±3°C)

| No. | Item | Symbol | Measure Condition (Figure 1) | Typ | Min | Max | Unit |
|-----|------|--------|---------------------------------|-----|-----|-----|------|
|-----|------|--------|---------------------------------|-----|-----|-----|------|

【CONTROL FUNCTIONS】 *Design guaranteed item

| | | | | | | | |
|----|--------------------------------------|----------|----------------------------------------------------|------|------|------|-----|
| 1 | Output Frequency | fosc | ※Figure 7 V4=15 V, V3=2 V, I2=-20 μA, V5=5 V | 67.0 | 60.3 | 73.7 | kHz |
| 2 | Jitter Frequency Deviation | d_fosc | ※Figure 7 V4=15 V, V3=2 V, I2=-20 μA, V5=5 V | 5.0 | 2.4 | 7.6 | kHz |
| *3 | Jitter Frequency Modulation Rate | fM | ※Figure 7 V4=15 V, V3=2 V, I2=-20 μA, V5=5 V | 360 | - | - | Hz |
| 4 | Maximum Duty Cycle | MAXDC | V4=15 V, V3=2 V, I2=-20 μA, V5=5 V | 54 | 50 | 58 | % |
| 5 | VDD Voltage | VDD | V4=15 V, V3=6 V, I2=-20 μA, V5=5 V, V6=1 V | 5.9 | 5.4 | 6.4 | V |
| 6 | VCC Start Voltage | VCC(ON) | V3=6 V, I2=-20 μA, V5=5 V, V6=1 V | 12 | 11 | 13 | V |
| 7 | VCC Stop Voltage | VCC(OFF) | V3=6 V, I2=-20 μA, V5=5 V, V6=1 V | 8.20 | 7.45 | 8.95 | V |
| 8 | VCC start/stop Hysteresis | VCC(HYS) | VCC(ON) - VCC(OFF) | 3.8 | 3.1 | 4.5 | V |
| 9 | Feedback Threshold Current | IFB1 | ON→OFF V4=15 V, V3=6 V, V5=5 V, V6=1 V | -57 | -81 | -34 | μA |
| 10 | Feedback Current Hysteresis | IFB(HYS) | OFF→ON V4=15 V, V3=6 V, V5=5 V, V6=1 V | 1.5 | - | - | μA |
| 11 | FB Pin Voltage | VFB1 | V4=15 V, V3=6 V, I2= IFB1, V5=5 V, V6=1 V | 1.9 | 1.6 | 2.2 | V |
| 12 | Circuit Current before start | ICC (SB) | V4=6.5 V, V3=6 V, I2=-20 μA, V5=5 V, V6=1 V | 0.25 | 0.20 | 0.30 | mA |
| 13 | Circuit Current | ICC | V4=15 V, V3=6 V, I2=-20 μA, V5=5 V, V6=1 V | 0.36 | 0.23 | 0.49 | mA |
| 14 | VDD Charging Current | Ich1 | V1=0 V, V5=40 V | -2.2 | -3.3 | -1.1 | mA |
| | | Ich2 | V1=4 V, V5=40 V | -1.3 | -2.1 | -0.6 | mA |
| 15 | LS start voltage | VLSH | V4=VCC(OFF)→VCC(ON), V3=6 V, I2=-20 μA, V5=5 V | 540 | 486 | 594 | mV |
| 16 | LS stop voltage | VLSL | V4=15 V, V3=6 V, I2=-20 μA, V5=5 V | 395 | 355 | 435 | mV |
| 17 | LS detect Hysteresis | VLS(HYS) | VLSH - VLSL | 145 | - | - | mV |
| 18 | LS start/stop mode filter time | TLStop | V4=15 V, V3=6 V, I2=-20 μA, V5=5 V V6=VLSH→VLSL | 5.85 | 4.20 | 7.50 | ms |
| 19 | LS detect SO signal mode filter time | TLSSO | V4=15 V, V3=6 V, I2=-20 μA, V5=5 V | 3.15 | 1.85 | 4.45 | ms |
| 20 | SO output voltage | VSO | V4=15 V, I2=-20 μA, V5=5 V V6=VLSH→VLSL | 4.2 | 3.2 | 5.2 | V |
| 21 | SO output current | ISO | V4=15 V, V3=1 V, I2=-20 μA, V5=5 V V6=0 V | -0.8 | -1.2 | -0.4 | mA |

| No. | Item | Symbol | Measure Condition (Figure 1) | Typ | Min | Max | Unit |
|-----|-----------------------------|----------|---------------------------------------------------------------------|-----|-----|------|---------|
| 22 | SO Disable Threshold | VSOTH | V4=15 V, I2=-20 μ A, V5=5 V, V6=0 V | 5.2 | 4.6 | 5.8 | V |
| 23 | SO Disable Threshold margin | D_VSO | VSOTH-VSO | 1.0 | 0.7 | 1.3 | V |
| 24 | SO pull down current | ISO_down | V4=15 V, V3=1 V, I2=-20 μ A, V5=5 V, V6=0 V | 0.7 | 0.3 | 1.1 | μ A |
| 25 | Soft start time | Tsoft | V4=VCC(OFF) \rightarrow VCC(ON) I2=-20 μ A, V5=5 V, V6=1 V | 8.5 | 5.0 | 12.0 | ms |

【CIRCUIT PROTECTIONS】

| | | | | | | | |
|-----|-----------------------------------------------|-----------|------------------------------------------------------------------------------------------------------------|-------|-------|-------|----------------|
| 26 | Self Protection Current Limit | ILIMIT | ※Figure 5 Duty=30 % V4=15 V, V3=2 V, V2=2.6 V, V5=adjusted | 0.350 | 0.315 | 0.385 | A |
| 27 | ILIMIT Compensation slope | R_slope | ※Figure 5 Duty=10 % V4=15 V, V3=2 V, V2=2.6 V, V5=adjusted | 10 | - | - | mA/ μ s |
| *28 | Drain Current at Light Load | ID(OFF) | Ton=4.5 μ sec, V4=15 V, V3=2 V, I2=IFB1+2 μ A, V5=adjusted | 100 | 40 | 160 | mA |
| 29 | FB current at heavy load | IFBOLP | V5=ILIMIT condition V4=15 V, V3=2 V, V2=3 V, V6=1 V | -10 | -13 | -7 | μ A |
| 30 | FB Over Load Protection detect voltage | VFBOLP | V5=ILIMIT condition V4=15 V, V3=2 V, V6=1 V | 3.85 | 3.50 | 4.20 | V |
| 31 | FB Over Load Protection Hysteresis | HYSVFBOLP | | 0.65 | - | - | V |
| 32 | FB discharge current at timer intermittent | IFBOLPP | V5=ILIMIT condition, V4=VCC(OFF) V3=2 V, V2=25 V, V6=1 V | 1.0 | 0.6 | 1.4 | mA |
| 33 | FB current at MAXDC detect | IFBMAXDC | V4=15 V, V3=6 V, V2=3 V, V5=5 V, V6=1 V | - | - | 0.2 | μ A |
| 34 | Timer intermittent function | TIMER | ※Figure 3 V4=VCC(ON) \leftrightarrow VCC(OFF), V5=ILIMIT condition, V3=6 V, I2=-20 μ A, V6=1 V | 4 | | | - |
| 35 | Timer intermittent function disabled at MAXDC | TIMER2 | ※Figure 4 V4=VCC(ON) \leftrightarrow VCC(OFF), V5=5 V, V3=6 V, I2=-20 μ A, V6=1 V | 1 | | | - |
| *36 | Leading Edge Blanking Delay | ton(BLK) | | 290 | 230 | 350 | ns |
| *37 | Current Limit Delay | td(OCL) | | 150 | 100 | 200 | ns |
| 38 | VCC Over Voltage Protection | VCC(OV) | V3=6 V, I2=-20 μ A, V5=5 V, V6=1 V | 29 | 26 | 32 | V |
| 39 | VDD Latch Voltage | VDD(OV) | V4=15 V, I1=IDD(OV), V3=0 V, I2=-20 μ A, V5=5 V, V6=6 V | 7.00 | 6.40 | 7.50 | V |
| 40 | VDD Latch Current | IDD(OV) | V4=15 V, V3=0 V, I2=-20 μ A, V5=5 V, V6=6 V | 3.5 | 2.4 | 4.6 | mA |
| 41 | VDD Latch Voltage margin | D_VDDOV | VDD(OV)-VDD | 0.9 | 0.4 | 1.5 | V |
| *42 | Thermal Shutdown Temperature | TOTP | | 140 | 130 | 150 | $^{\circ}$ C |
| 43 | Latch Reset VDD Threshold | VDDreset | | 2.7 | 1.8 | 3.5 | V |

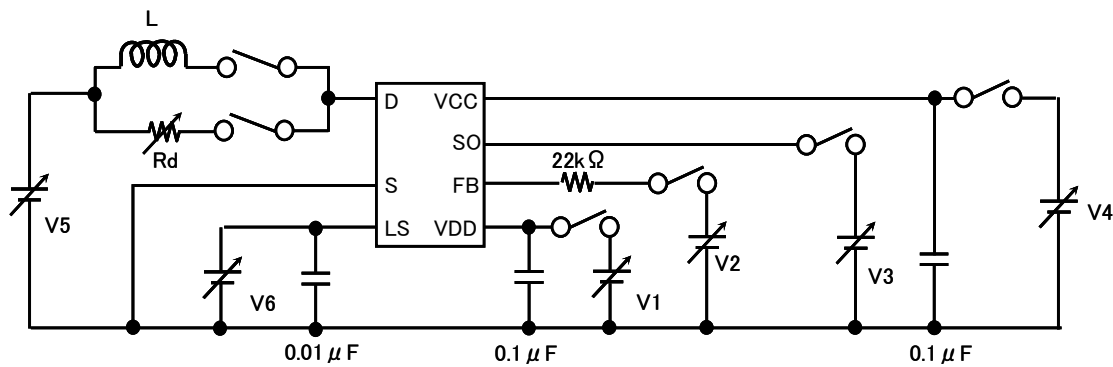
【OUTPUT】

| No. | Item | Symbol | Measure Condition (Figure 1) | Typ | Min | Max | Unit |
|-----|---------------------------|---------|------------------------------------------------------------|-----|-----|-----|----------|
| 44 | ON-State Resistance | RDS(ON) | V4=15 V, V3=2 V I5=100 mA, I2=-20 μ A, V6=1 V | 16 | - | 21 | Ω |
| 45 | OFF-State leakage Current | IDSS | V4=35 V, I2=-20 μ A, V3=6 V, V5=650 V, V6=1 V | 10 | - | 20 | μ A |
| 46 | Breakdown Voltage | VDSS | V4=35 V, I2=-20 μ A, V3=6 V, I5=100 μ A, V6=1 V | - | 700 | - | V |
| *47 | Rise Time | tr | ※Figure 6 V4=15 V, V3=1 V, I2=-20 μ A, V5=5 V | 70 | - | - | ns |
| *48 | Fall Time | tf | ※Figure 6 V4=15 V, V3=1 V, I2=-20 μ A, V5=5 V | 35 | - | - | ns |

【SUPPLY VOLTAGE】

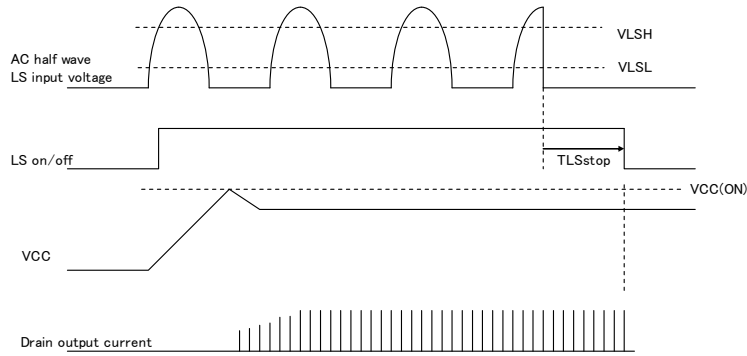
| | | | | | | | |
|----|----------------------|---------|--|---|----|---|---|
| 49 | Drain Supply Voltage | VD(MIN) | | - | 50 | - | V |
|----|----------------------|---------|--|---|----|---|---|

【Figure 1: Measure circuit】

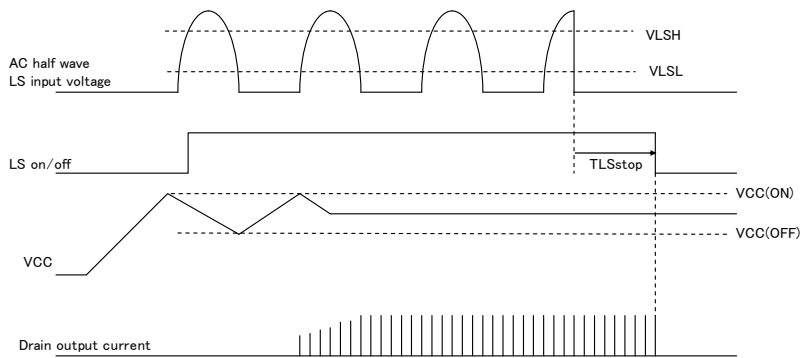


【Figure 2: Start up and Stop diagram】

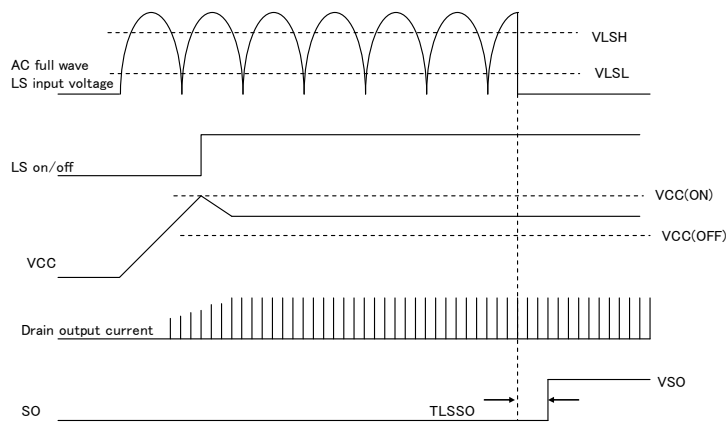
(A) Normal start and stop of LS start/stop mode (SO is connected to VDD)



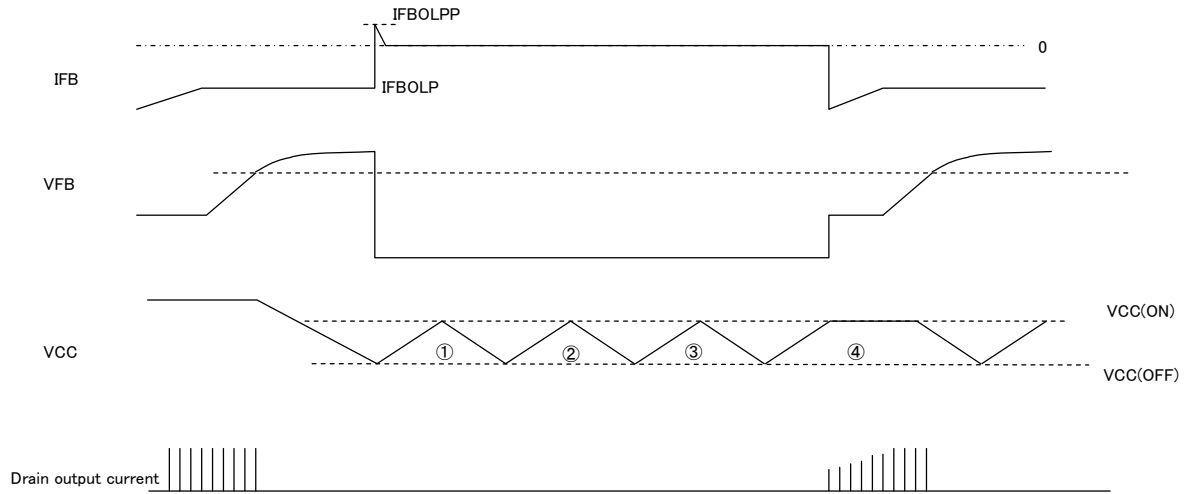
(B) Slow start and stop of LS start/stop mode (SO is connected to VDD)



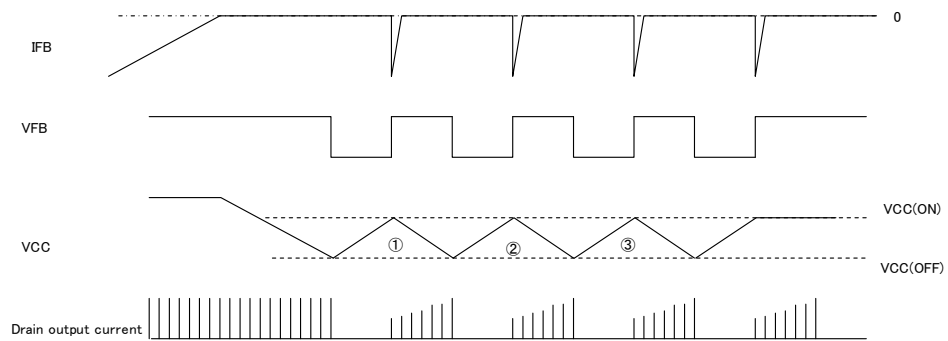
(C) Normal start and stop of LS detect SO signal mode (SO is connected to external parts)



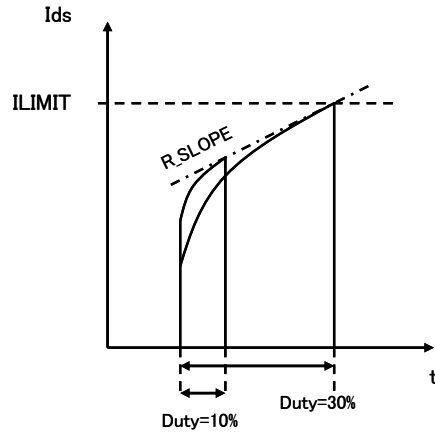
【Figure 3: Timer intermittent Over load protection diagram】



【Figure 4: OLP is disabled when MAXDC operation】

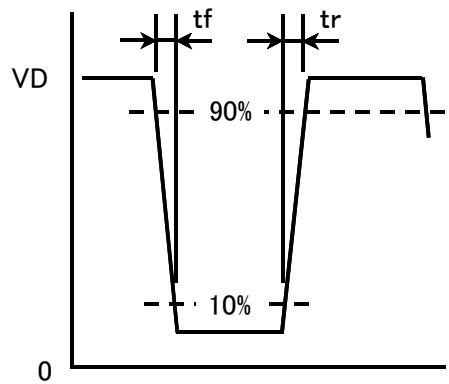


【Figure 5: I_{LIMIT}, R_{Slope} measurement】

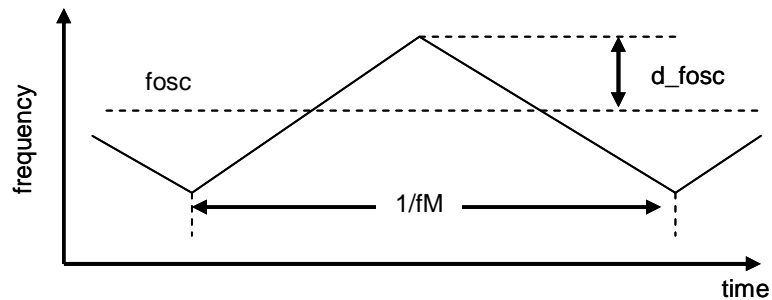


$$R_{slope} ; \{ (I_{LIMIT} \text{ at Duty}=30\%) - (I_{LIMIT} \text{ at Duty}=10\%) \} / \{ (T_{on} \text{ at Duty}=30\%) - (T_{on} \text{ at Duty}=10\%) \}$$

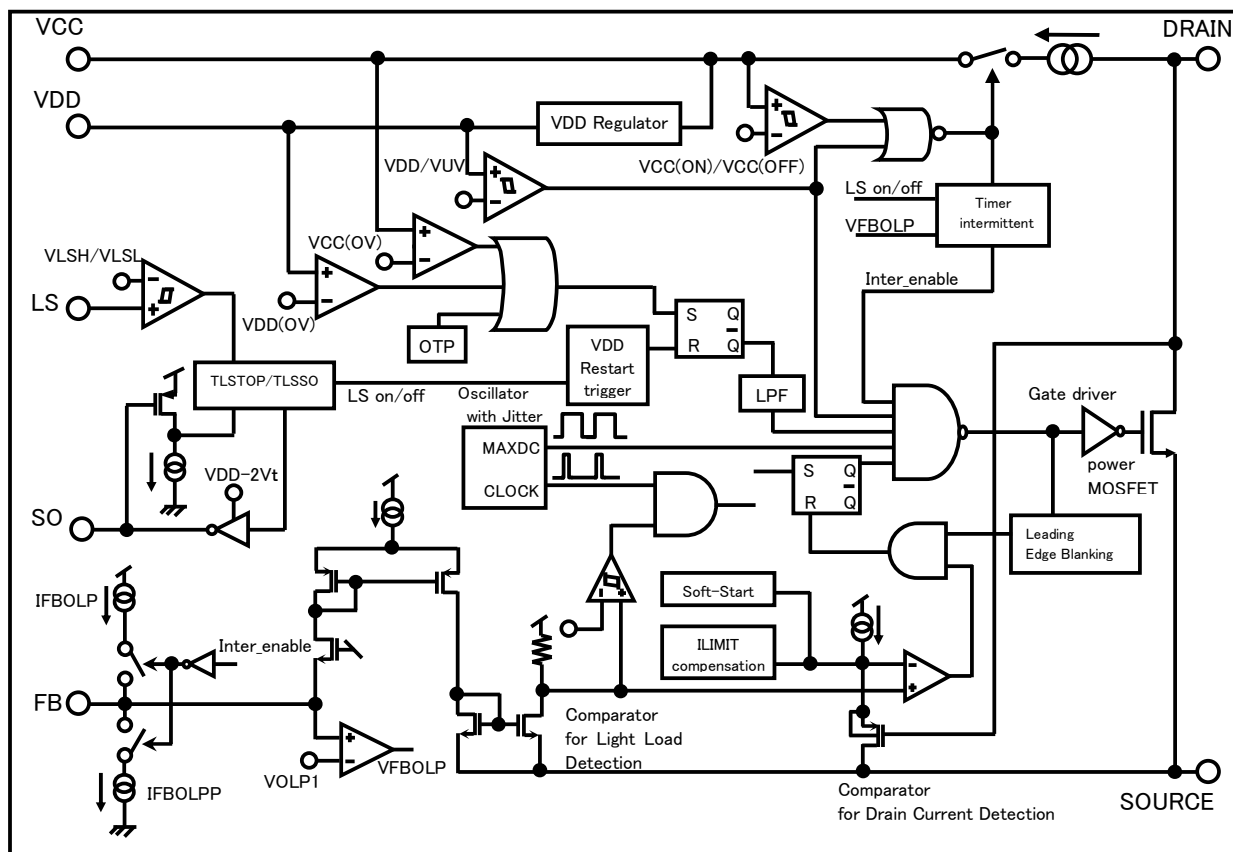
【Figure 6: t_r, t_f measurement】



【Figure 7: d_{fosc}, f_M measurement】

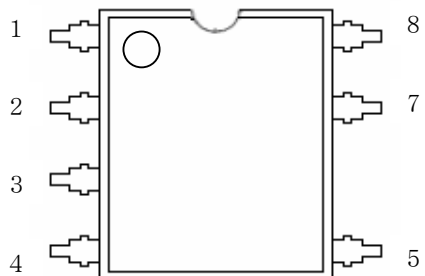


【Figure 8: Circuit Block Diagram】



2010.02.17

【Figure 9: Pin Layout】



| Pin No. | Terminal Name |
|---------|---------------|
| 1 | VDD |
| 2 | FB |
| 3 | SO |
| 4 | VCC |
| 5 | Drain |
| 6 | — |
| 7 | Source |
| 8 | LS |

【Precautions for Use 1】

Connect a ceramic capacitor with value $>0.1 \mu\text{F}$ between VDD pin and GND.

【Precautions for Use 2】

The IPD has risks for break-down or burst or giving off smoke in following conditions. Avoid the following use.
Fuse should be added at the input side or connect zener diode between control pin and GND, etc as a countermeasure to pass regulatory Safety Standard. Concrete countermeasure could be provided individually. However, customer should make the final judgment.

- (1) Reverse the DRAIN pin and VDD pin connection to the power supply board.
- (2) DRAIN pin short to VDD pin.
- (3) DRAIN pin short to FB pin.
- (4) DRAIN pin short to SO pin.
- (5) DRAIN pin short to VCC pin.
- (6) DRAIN pin short to LS pin.
- (7) VCC pin short to VDD pin.
- (8) VCC pin short to FB pin.
- (9) VCC pin short to SO pin.
- (10) VCC pin short to LS pin.

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