Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.
If you would find description “Panasonic” or “Panasonic semiconductor solutions”, please replace it with NTCJ.

※ Except below description page
“Request for your special attention and precautions in using the technical information and semiconductors described in this book”

Nuvoton Technology Corporation Japan

MIP2L40MY

Silicon MOS FET type integrated circuit

■ Features

- Reducing the average noise
  Adding a frequency jitter function to MIP2E/3E* series to dramatically reduce the average noise and simplify EMI parts
- Stabilization of maximum electric power by input correction
  Correcting the input voltage dependency of I LIMIT reduces the input voltage dependency of maximum output current
- Overheating protection function
  Changed from stopping in latch mode to self reset type
- Protecting function
  Overload protection, overheat protection

■ Package

- Code
  TO-220-A2
- Pin Name
  1. CONTROL
  2. SOURCE
  3. DRAIN

■ Marking Symbol: MIP2L4MY

■ Applications

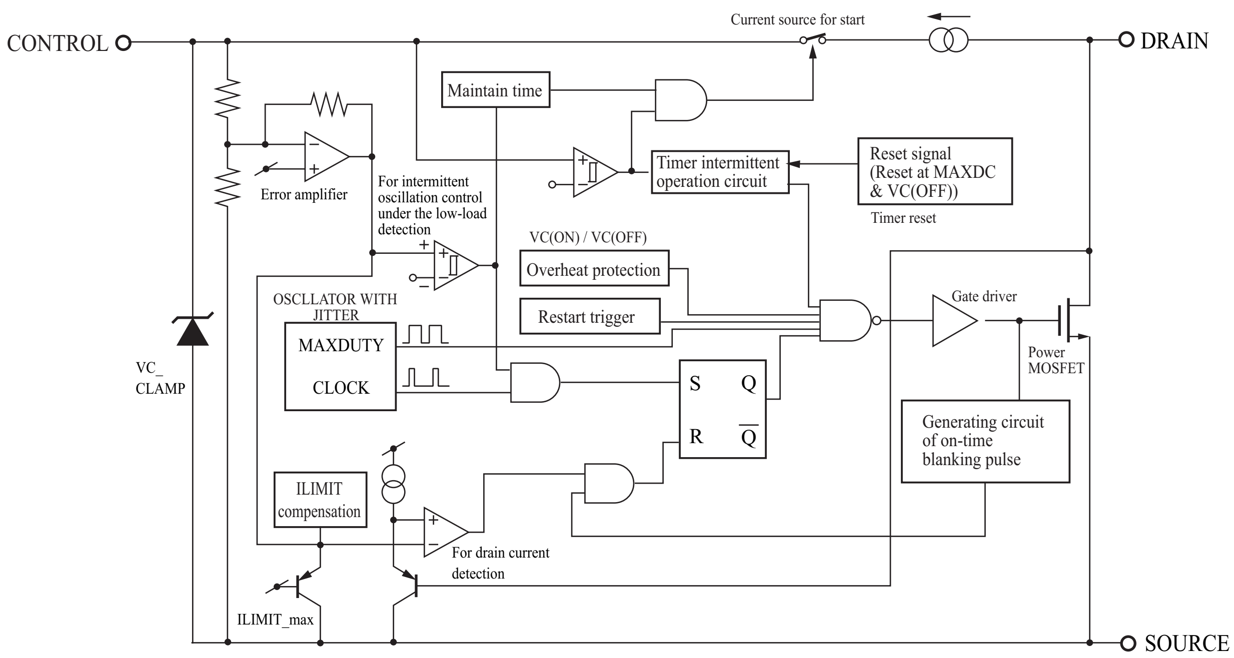
- Flat-screen TV, audio and others

■ Absolute Maximum Ratings $T_a = 25°C \pm 3°C$

Parameter	Symbol	Rating	Unit
DRAIN voltage	VD	− 0.3 to +700	V
CONTROL voltage	VC	− 0.3 to +8	V
Output peak current *	IDP	2.7	A
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Note) *: The guarantee within the following pulse width.
Leading edge blanking delay + Current limit delay ton(BLK) + td(OCL)

■ Block Diagram



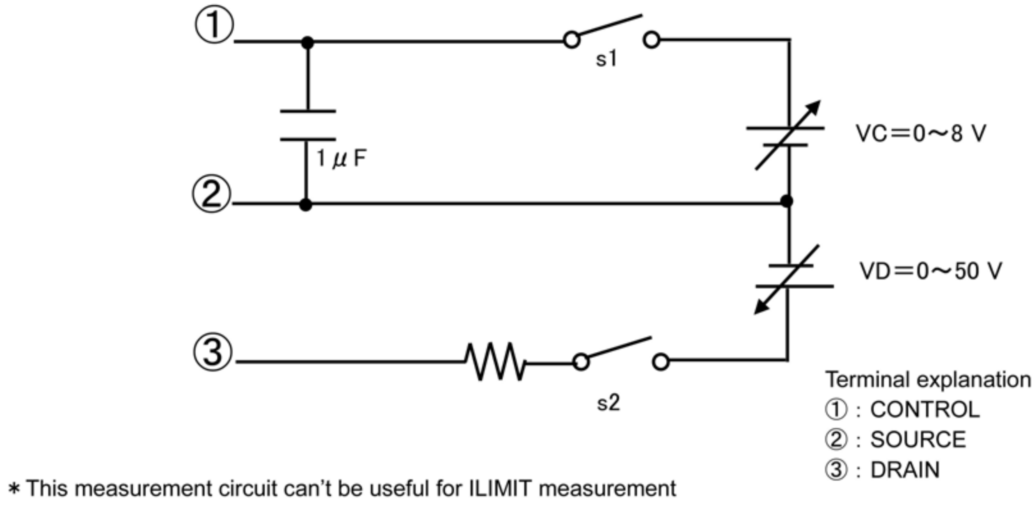
■ Electrical Characteristics T_C = 25°C±3°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Control functions						
Output frequency	fosc	VC = VC(CNT) – 0.2 V, VD = 5V	92	100	108	kHz
Jitter frequency deviation	Δf	VC = VC(CNT) – 0.2 V, VD = 5V * Fig. 5		5.5		kHz
Jitter frequency modulation rate *	fM	VC = VC(CNT) – 0.2 V, VD = 5V * Fig. 5		270		Hz
Maximum duty cycle	MAXDC	VC = VC(CNT) – 0.2 V, VD = 5V	50	53	56	%
PWM gain *	GPWM	VC = VC(CNT)		12.5		dB
Before auto-restart current	IC(SB)1	VC < VC(ON), VD = 5 V	0.2	0.5	0.8	mA
After off-state current	IC(SB)2	VC > VC(CNT), VD = 5 V	0.2	0.5	0.8	mA
Operating current	IC(OP)	VC = VC(CNT) – 0.2 V, VD = 5V	0.25	0.7	1.15	mA
Auto-restart threshold voltage	VC(ON)	VD = 5V	5.75	6.25	6.75	V
UV lockout threshold voltage	VC(OFF)	VD = 5V	4.35	4.8	5.25	V
Auto-restart maintain voltage	VC_m	S1 = OPEN	4.95	5.45	5.95	V
Auto-restart maintain time	Tm	S1 = OPEN		45		ms
Auto-restart hysteresis voltage	ΔVC	VC(ON) – VC(OFF)	1.05	1.45	1.85	V
Control clamp voltage	VC(CLP)	IC = 3 mA	6.2	6.8	7.4	V
Auto-restart duty cycle	TSW/TTIM	S1 = OPEN * Fig. 4		12		%
Auto-restart frequency	fTIM	S1 = OPEN * Fig. 4		2.6		Hz
Control pin charging current	IC(CHG)1	VC = 0 V, VD = 50 V	–14	–9	–6	mA
	IC(CHG)2	VC = 5 V, VD = 50 V	–11.2	–5.7	–2.4	mA
Control pin voltage	VC(CNT)	VD = 5 V	5.3	5.9	6.5	V
Control pin voltage hysteresis *	ΔVC(CNT)	VD = 5 V		10		mV
Circuit protections						
Self protection current limit	ILIMIT	Duty = 30% * Fig. 1, 2	1.24	1.35	1.46	A
ILIMIT modified coefficient	R_slope	VC = VC(CNT) – 0.2 V * Fig. 1, 2		37		mA/µs
Leading edge blanking delay *	ton(BLK)		240	300	360	ns
Current limit delay *	td(OCL)		140	210	280	ns
Thermal shutdown temperature *	TOTP		130	140	150	°C
Thermal shutdown temperature hysteresis *	ΔTOTP			70		°C
Output						
Power-up reset theshold voltage *	VCreset		1.8	2.6	3.5	V
ON-state resistance	RDS(ON)	ID = 0.2 A		5.2	6.7	Ω
OFF-state leakage current	IDSS	VD = 650 V, VC = 6.5 V		10	20	µA
Breakdown voltage	VDSS	ID = 100 µA, VC = 6.5 V	700			V
Rise time	tr	VC = VC(CNT) – 0.2 V, VD = 5 V * Fig. 3		95		ns
Fall time	tf	VC = VC(CNT) – 0.2 V, VD = 5 V * Fig. 3		30		ns
Supply voltage characteristics						
Drain supply voltage	VD(MIN)	S1 = OPEN	36			V

Note) *: Design guaranteed item

■ Electrical Characteristics (continued) $T_C = 25°C±3°C$

1. Measurement circuit



2. Figure 1. Measurement circuit 2

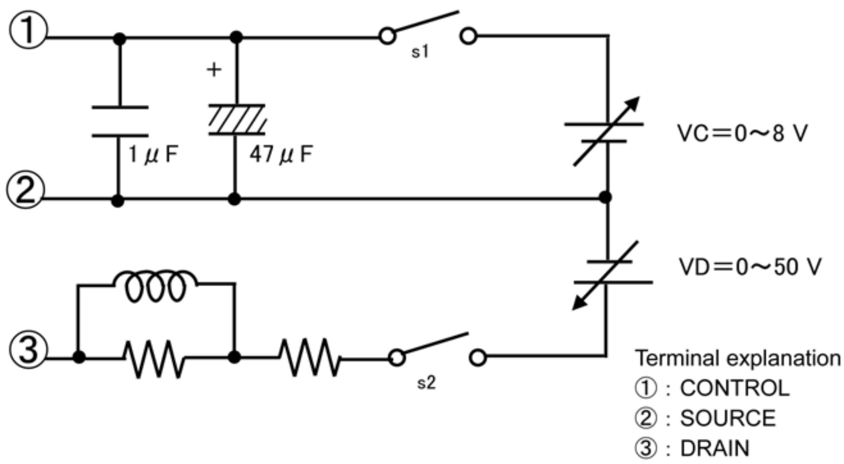
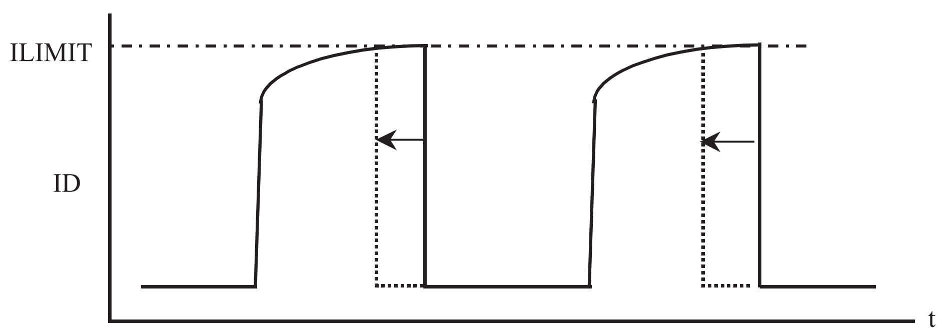


Figure 2. ILIMIT measurement



R_slope = {(ILIMIT at Duty = 30%) – (ILIMIT at Duty = 20%)} / {(Ton at Duty = 30%) – (Ton at Duty = 20%)}

■ Electrical Characteristics (continued) T_C = 25°C±3°C

2. Figure 3. tr, tf measurement

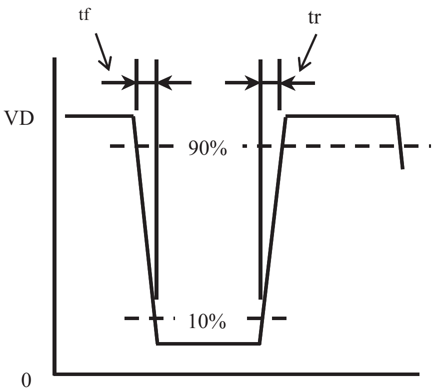


Figure 4. VC_m, Tm, TTSW. TTIM, FTIM measurement

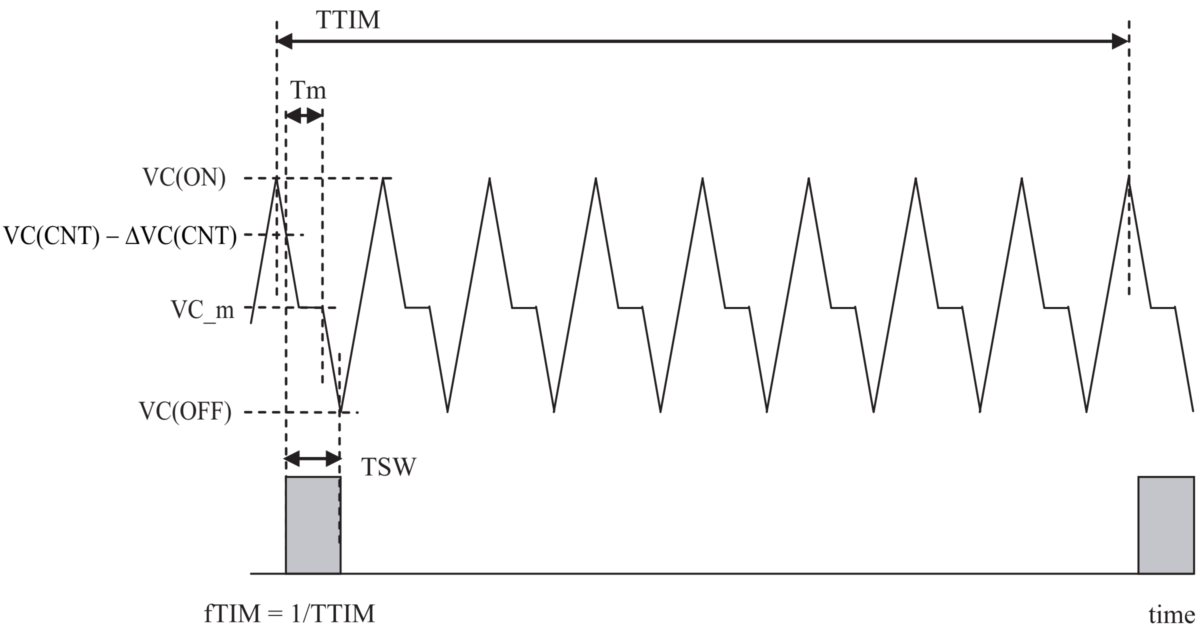
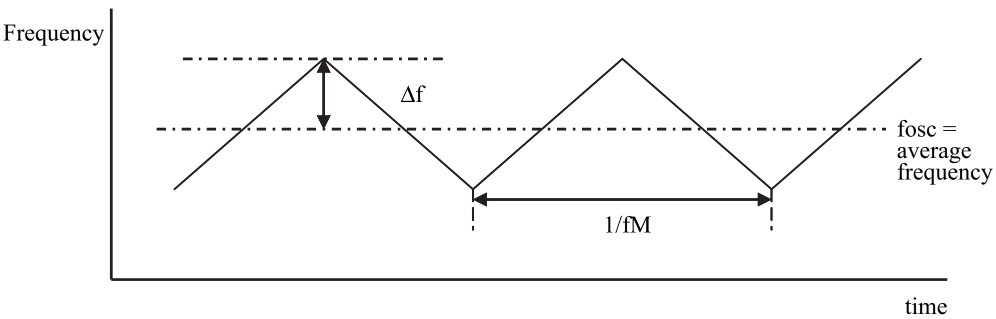


Figure 5. Δf, fM measurement



■ Usage Notes

Connect a Ceramic Capacitor (over 0.1 μF) between CONTROL and SOURCE.

The IPD has risks for break-down or burst or giving off smoke in following conditions. Avoid the following use.
Fuse should be added at the input side or connect zener diode between control pin and GND, etc as a countermeasure to pass regulatory Safety Standard. Concrete countermeasure could be provided individually. However, customer should make the final judgment.

(1) Reverse the DRAIN pin and SOURCE pin connection to the power supply board.
(2) DRAIN pin short to CONTROL pin.
(3) DRAIN pin short to SOURCE pin.

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