MOS FET

FK8V06060L
Single N-channel MOS FET
For lithium-ion secondary battery protection circuits
For load switching

Features
• Low drain-source ON resistance: RDS(on) typ. = 70 mΩ (VGS = 4.5 V)
• Halogen-free / RoHS compliant
  (EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

Marking Symbol: M1

Packaging
Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

Absolute Maximum Ratings  Ta = 25 °C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage</td>
<td>VDS</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source Voltage</td>
<td>VGS</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current (DC)*1</td>
<td>ID</td>
<td>3</td>
<td>A</td>
</tr>
<tr>
<td>Drain Current (Pulsed)*1,*2</td>
<td>IDp</td>
<td>9</td>
<td>A</td>
</tr>
<tr>
<td>Total Power Dissipation*1 (Steady State)</td>
<td>PD</td>
<td>1.3</td>
<td>W</td>
</tr>
<tr>
<td>Channel Temperature</td>
<td>Tch</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Tstg</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note
*1 Device mounted on a glass-epoxy board coated Copper (see Fig. 1)
*2 Ensure that the channel temperature does not exceed 150°C

(Fig. 1) Glass-Epoxy Board coated Copper
FR-4 25.4 × 25.4 × 0.8 (Unit: mm)
### Electrical Characteristics  \( Ta = 25 \, ^\circ C \pm 3 \, ^\circ C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Breakdown Voltage</td>
<td>VDSS</td>
<td>ID = 1 mA, VGS = 0 V</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Source Current</td>
<td>IDSS</td>
<td>VDS = 60 V, VGS = 0 V</td>
<td>10</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source Leakage Current</td>
<td>IGSS</td>
<td>VGS = ( \pm 16 ) V, VDS = 0 V</td>
<td>( \pm 10 )</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source Threshold Voltage</td>
<td>Vth</td>
<td>ID = 480 ( \mu A ), VDS = 10 V</td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Drain-source On-state Resistance</td>
<td>RDS(on)1</td>
<td>ID = 1.5 A, VGS = 10 V</td>
<td>-</td>
<td>60</td>
<td>85</td>
<td>m( \Omega )</td>
</tr>
<tr>
<td></td>
<td>RDS(on)2</td>
<td>ID = 1.5 A, VGS = 4.5 V</td>
<td>-</td>
<td>70</td>
<td>100</td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>Input Capacitance (^1)</td>
<td>Ciss</td>
<td>VDS = 10 V, VGS = 0 V, f = 1 MHz</td>
<td></td>
<td></td>
<td>50</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance (^1)</td>
<td>Coss</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Transfer Capacitance (^1)</td>
<td>Crss</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-on delay Time (^1,,2)</td>
<td>td(on)</td>
<td>VDD = 30 V, VGS = 0 to 10 V</td>
<td>9</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time (^1,,2)</td>
<td>tr</td>
<td>ID = 3.0 A</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-off delay Time (^1,,2)</td>
<td>td(off)</td>
<td>VDD = 30 V, VGS = 10 to 0 V</td>
<td>38</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time (^1,,2)</td>
<td>tf</td>
<td>ID = 3.0 A</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge (^1)</td>
<td>Qg</td>
<td>VDD = 30 V</td>
<td>7.0</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Gate-source Charge (^1)</td>
<td>Qgs</td>
<td>VGS = 0 to 10 V,</td>
<td>1.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-drain Charge (^1)</td>
<td>Qgd</td>
<td>ID = 3.0 A</td>
<td>1.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Body Diode Forward Voltage</td>
<td>VSD</td>
<td>IF = 1.5 A, VGS = 0 V</td>
<td>0.8</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**Note**

Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\(^1\) Assured by design

\(^2\) Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time
**Measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time**

- **Vin**
  - 10 V
  - 0 V

- **Vout**
  - PW = 10 μs
  - D.C. ≤ 1 %

- **VDD = 30 V**
- **ID = 3.0 A**

- **td(on)**
- **tr**
- **td(off)**
- **tf**
Technical Data (reference)

**ID - VDS**

- **VGS = 10 V**
- **4.5 V**
- **3.5 V**
- **3.0 V**

**RDS(on) - ID**

- **VGS = 4.5 V**
- **10 V**

**ID - VGS**

- **Ta = 125 °C**
- **85 °C**
- **25 °C**
- **-30 °C**

**RDS(on) - VGS**

- **Ta = 125 °C**
- **85 °C**
- **25 °C**
- **-30 °C**

**IF - VF**

- **Ta = 125 °C**
- **85 °C**
- **25 °C**
- **-30 °C**

**Capacitance - VDS**

- **Ciss**
- **Coss**
- **Crss**
Technical Data (reference)

**Rth - tsw Safe Operating Area**

- **Operation in this area is limited by RDS(on) (4.5 V)**
- **Ta = 25°C,** Mounted on FR4 board (25.4 × 25.4 × 0.8 mm) coated with copper foil.

**Vth - Ta**

- **ID = 480 μA**

**RDS(on) - Ta**

- **ID = 1.5 A**
  - **VGS = 4.5 V**
  - **10 V**

**Dynamic Input/Output Characteristics**

- **ID = 3.0 A**
- **VDS = 30 V**
MOS FET

FK8V06060L

WMini8-F1

Unit: mm

- Land Pattern (Reference) (Unit: mm)

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