FK6K02010L
Silicon N-channel MOS FET

For switching

- **Features**
  - Low drain-source On-state Resistance: $R_{DS(on)} = 13 \, \text{m} \Omega \, (V_{GS} = 4.5 \, \text{V})$
  - Low drive voltage: 2.5 V drive
  - Halogen-free / RoHS compliant
    (EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

- **Marking Symbol**: TA

- **Packaging**
  Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

### Absolute Maximum Ratings  $T_a = 25 \, ^\circ\text{C}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source surrender voltage</td>
<td>VDSS</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source surrender voltage</td>
<td>VGSS</td>
<td>±10</td>
<td>V</td>
</tr>
<tr>
<td>Drain current</td>
<td>ID</td>
<td>4.5</td>
<td>A</td>
</tr>
<tr>
<td>Peak drain current $^1$</td>
<td>IDp</td>
<td>18</td>
<td>A</td>
</tr>
<tr>
<td>Power dissipation $^2$</td>
<td>PD</td>
<td>700</td>
<td>mW</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>Tch</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>Topr</td>
<td>-40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:**

|$^1 t = 10 \, \mu\text{s, Duty Cycle < 1%}$

|$^2$ Measuring on Glass epoxy board (25.4 × 25.4 × 0.8 mm)
coated with copper foil, which has more than 300 mm$^2$
Absolute maximum rating without heat sink for PD is 150 mW.
## Electrical Characteristics  \( Ta = 25 ^\circ C \pm 3 ^\circ C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source surrender voltage</td>
<td>( VDSS ) ( ID = 1 \ mA, \ VGS = 0 )</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Drain-source cutoff current</td>
<td>( IDSS ) ( VDS = 20 \ V, \ VGS = 0 )</td>
<td></td>
<td>1.0</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source cutoff current</td>
<td>( IGSS ) ( VGS = \pm 8 \ V, \ VDS = 0 )</td>
<td></td>
<td>( \pm 10 )</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate threshold voltage</td>
<td>( Vth ) ( ID = 1.0 \ mA, \ VDS = 10.0 \ V )</td>
<td>0.4</td>
<td>0.85</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>Drain-source ON resistance</td>
<td>( RDS(ON1) ) ( ID = 2.0 \ A, \ VGS = 4.5 \ V )</td>
<td>13</td>
<td>17.5</td>
<td></td>
<td>m( \Omega )</td>
</tr>
<tr>
<td></td>
<td>( RDS(ON2) ) ( ID = 1.0 \ A, \ VGS = 2.5 \ V )</td>
<td>16</td>
<td>28</td>
<td></td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td>(</td>
<td>Yfs</td>
<td>) ( ID = 1.0 \ A, \ VDS = 10 \ V )</td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td>Short-circuit input capacitance (Common source)</td>
<td>( Ciss ) ( VDS = 10 \ V, \ VGS = 0, \ f = 1 \ MHz )</td>
<td></td>
<td>1.730</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Short-circuit output capacitance (Common source)</td>
<td>( Coss ) ( VDSS )</td>
<td>155</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Reverse transfer capacitance (Common source)</td>
<td>( Crss ) ( ID = 2.0 \ A, \ VGS = 4.5 \ V )</td>
<td>1.65</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Turn-on delay time ( ^{\dagger} )</td>
<td>( td(on) ) ( VDD = 10 \ V )</td>
<td>19</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise time ( ^{\dagger} )</td>
<td>( tr ) ( VGS = 0 ) to 4 \ V )</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Turn-off delay time ( ^{\dagger} )</td>
<td>( td(off) ) ( ID = 1.0 \ A )</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Fall time ( ^{\dagger} )</td>
<td>( tf ) ( ID = 2.0 \ A )</td>
<td>75</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note:**

1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
2. *1 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time
*1 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

VDD = 10 V
ID = 1.0 A
RL = 10 Ω

PW = 10 μs
D.C. ≦ 1 %

Vin
G

50 Ω

D
S

Vout

90%

10%

10

Vout

90%

td(on)
tr
tf
td(off)
Technical Data (reference)

**ID - VDS**

- Drain current ID (A) vs. Drain-source voltage VDS (V)

**ID - VGS**

- Drain current ID (A) vs. Gate-source voltage VGS (V)

**VDS - VGS**

- Drain-source voltage VDS (V) vs. Gate-source voltage VGS (V)

**RDS(on) - ID**

- Drain source On-resistance RDS(on) (mΩ) vs. Drain current ID (A)

**Capacitance - VDS**

- Capacitance C (pF) vs. Drain-source voltage VDS (V)
**Technical Data (reference)**

### Gate-source Threshold Voltage $V_{th}$ (V) vs. Temperature ($^\circ$C)

- **VGS = 2.5 V**
- **VGS = 4.5 V**

### Drain-source On-resistance $R_{DS(on)}$ (m$\Omega$) vs. Temperature ($^\circ$C)

- $VGS = 2.5 V$
- $VGS = 4.5 V$

### Total Power Dissipation (W) vs. Temperature $Ta$ ($^\circ$C)

- Mounted on glass-epoxy board
- (25.4 x 25.4 x 0.8 mm)

### Drainsource Voltage $VDS$ (V) vs. Drain Current $ID$ (A)

- $IDp = 18 A$
- Operation in this area is limited by $R_{DS(on)}$

### Safe Operating Area

- $Ta = 25^\circ$C, Glass epoxy board coated with copper foil, which has more than 300mm$^2$. 
- Operation limited by $R_{DS(on)}$

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**Established**: 2010-06-07  
**Revised**: 2013-07-01
WSMini6-F1-B

**MOS FET**

**FK6K02010L**

**Unit: mm**

- 2.0 ± 0.1
- 1.7 ± 0.1
- 0.20 ± 0.02
- 0.13 ± 0.03
- 0.7 ± 0.1
- 2.1 ± 0.1
- 1.3 ± 0.1
- 0 ± 0.1

**Land Pattern (Reference) (Unit: mm)**

- 0.65 × 0.65
- 2.0
- 0.45
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