FG6543010R
Silicon N-channel MOSFET (FET1)
Silicon P-channel MOSFET (FET2)

For switching

- Features
  - Low drive voltage: 2.5 V drive
  - Halogen-free / RoHS compliant
    (EU RoHS / UL-94 V-0 / MSL: Level 1 compliant)

- Marking Symbol: V7

- Basic Part Number
  FJ330301 + FK330301 (Individual)

- Packaging
  FG6543010R Embossed type (Thermo-compression sealing):
  3,000 pcs/reel (standard)

### Absolute Maximum Ratings Ta = 25 °C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Voltage</td>
<td>VDS</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source Voltage</td>
<td>VGS</td>
<td>±12</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current</td>
<td>ID</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>Drain Current (Pulsed)</td>
<td>IDp</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Drain-source Voltage</td>
<td>VDS</td>
<td>-30</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source Voltage</td>
<td>VGS</td>
<td>±12</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current</td>
<td>ID</td>
<td>-100</td>
<td>mA</td>
</tr>
<tr>
<td>Drain Current (Pulsed)</td>
<td>IDp</td>
<td>-200</td>
<td>mA</td>
</tr>
<tr>
<td>Total Power Dissipation</td>
<td>PD</td>
<td>150</td>
<td>mW</td>
</tr>
<tr>
<td>Channel Temperature</td>
<td>Tch</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

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Publication date: October 2012  Ver. CED
### Electrical Characteristics \( T_a = 25 \ ^\circ C \pm 3 \ ^\circ C \)

#### FET1(Nch.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Breakdown Voltage</td>
<td>VDSS</td>
<td>ID = 1 mA, VGS = 0 V</td>
<td>30</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>IDSS</td>
<td>VDS = 30 V, VGS = 0 V</td>
<td></td>
<td>1.0</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source Leakage Current</td>
<td>IGSS</td>
<td>VGS = ±10 V, VDS = 0 V</td>
<td></td>
<td>±10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source Threshold Voltage</td>
<td>Vth</td>
<td>ID = -1 mA, VDS = 3.0 V</td>
<td>0.5</td>
<td>1.0</td>
<td>1.5</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Drain-source On-state Resistance</td>
<td>RDS(on)1</td>
<td>ID = 10 mA, VGS = 2.5 V</td>
<td>3</td>
<td>6</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td>RDS(on)2</td>
<td>ID = 10 mA, VGS = 4.0 V</td>
<td>2</td>
<td>3</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td>(</td>
<td>Yfs</td>
<td>)</td>
<td>ID = 10 mA, VDS = 3.0 V</td>
<td>20</td>
<td>55</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Ciss</td>
<td>VDS = 3 V, VGS = 0 V, f = 1 MHz</td>
<td>7</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>Coss</td>
<td>VDS = 3 V, VGS = 0 V, f = 1 MHz</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>Crss</td>
<td>VDS = 3 V, VGS = 0 V, f = 1 MHz</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Turn-on Time (^1)</td>
<td>ton</td>
<td>VDD = 3 V, VGS = 0 V to 3 V</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID = 10 mA</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Turn-off Time (^1)</td>
<td>ton</td>
<td>VDD = 3 V, VGS = 3 V to 0 V</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID = 10 mA</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

*Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.*

\(^1\) See FET1 Test circuit.

#### FET2(Pch.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Breakdown Voltage</td>
<td>VDSS</td>
<td>ID = 1 mA, VGS = 0 V</td>
<td>-30</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>IDSS</td>
<td>VDS = -30 V, VGS = 0 V</td>
<td></td>
<td>-1.0</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source Leakage Current</td>
<td>IGSS</td>
<td>VGS = ±10 V, VDS = 0 V</td>
<td></td>
<td>±10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source Threshold Voltage</td>
<td>Vth</td>
<td>ID = -1 mA, VDS = -3.0 V</td>
<td>-0.5</td>
<td>-1.0</td>
<td>-1.5</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Drain-source On-state Resistance</td>
<td>RDS(on)</td>
<td>ID = -10 mA, VGS = -2.5 V</td>
<td>7</td>
<td>17</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td>RDS(on)2</td>
<td>ID = -10 mA, VGS = -4.0 V</td>
<td>4</td>
<td>7</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td>(</td>
<td>Yfs</td>
<td>)</td>
<td>ID = -10 mA, VDS = -3.0 V</td>
<td>20</td>
<td>40</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Ciss</td>
<td>VDS = -3 V, VGS = 0 V, f = 1 MHz</td>
<td>7</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>Coss</td>
<td>VDS = -3 V, VGS = 0 V, f = 1 MHz</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>Crss</td>
<td>VDS = 3 V, VGS = 0 V, f = 1 MHz</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Turn-on Time (^2)</td>
<td>ton</td>
<td>VDD = -3 V, VGS = 0 V to -3 V,</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID = -10 mA</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Turn-off Time (^2)</td>
<td>ton</td>
<td>VDD = -3 V, VGS = -3 V to 0 V,</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID = -10 mA</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

*Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.*

\(^2\) See FET2 Test circuit.
*1 FET1 Test circuit

FET1(Nch.)

Vin

PG = 10 \mu s
D.C. \leq 1 \%

VDD = 3 V

ID = 10 mA
RL = 300 \Omega

Vin

G

S

Vout

90 %

10 %

ton

toff

10 %

90 %
*2 FET2 Test circuit

FET2(Pch.)

VDD = -3 V
ID = -10 mA
RL = 300 Ω

0 V
VDD
Vin
50 Ω
G
S
D
VDD
Vin

PW = 10μs
D.C. ≤ 1 %

10 %
90 %
10 %
90 %

ton
toff

Vin
Vout
FET1(Nch.)

Ver. CED

FG6543010R

Safe Operating Area

Drain-source Voltage $V_{DS} (V)$
Drain Current $I_D (A)$

$ID_p = 0.2 \ A$

Operation in this area is limited by $R_{DS(on)}$.

$Ta = 25 °C$
Glass epoxy board (25.4 $\times$ 25.4 $\times$ t0.8mm) coated with copper foil, which has more than 300mm$^2$.

Gate-source Threshold Voltage $V_{th} (V)$

$V_{th} - Ta$

Drain-source On-state Resistance $R_{DS(on)} (\Omega)$

$R_{DS(on)} - Ta$

Total Power Dissipation $P_D (W)$

$P_D - Ta$

Thermal Resistance $R_{th} (\degree C/W)$

$R_{th} - tsW$

Temperature $Ta (°C)$

$-50$ $0$ $50$ $100$ $150$

$0$ $1$ $2$ $3$ $4$

$-50$ $0$ $50$ $100$ $150$ $200$

$0$ $1$ $10$ $100$

$0.001$ $0.01$ $0.1$ $1$ $10$

$0.0001$ $0.001$ $0.01$ $0.1$ $1$ $10$

$-50$ $0$ $50$ $100$ $150$

$0$ $1$ $2$ $3$ $4$

$0$ $0.1$ $1$ $10$ $100$ $1000$

$0.001$ $0.01$ $0.1$ $1$ $10$ $100$ $1000$
Drain Current $I_D$ vs. Drain-source Voltage $V_{DS}$

Gate-source Voltage $V_{GS}$ vs. Drain Current $I_D$

Drain-source On-state Resistance $R_{DS(on)}$ vs. Drain Current $I_D$

Capacitance vs. Drain-source Voltage $V_{DS}$

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FET2(Pch.)

**Safe Operating Area**

- **Gate-source Threshold Voltage** ($V_{th}$) vs. Temperature ($T_a$)
- **Drain-source On-state Resistance** ($R_{DS(on)}$) vs. Temperature ($T_a$)
- **Total Power Dissipation** ($P_D$) vs. Temperature ($T_a$)
- **Thermal Resistance** ($R_{th}$) vs. Pulse Width ($t_{sw}$)

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**Gate-source Threshold Voltage ($V_{th}$)**

- $V_{th}$ vs. $T_a$ graph

**Drain-source On-state Resistance ($R_{DS(on)}$)**

- $R_{DS(on)}$ vs. $T_a$ graph

**Total Power Dissipation ($P_D$)**

- $P_D$ vs. $T_a$ graph

**Thermal Resistance ($R_{th}$)**

- $R_{th}$ vs. $t_{sw}$ graph

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**Operation in this area is limited by $R_{DS(on)}$**

- Glass epoxy board ($25.4 \times 25.4 \times 0.8$ mm) coated with copper foil, which has more than 300 mm$^2$. 

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**Drain-source Voltage ($V_{DS}$)**

- $V_{DS}$ vs. Drain Current ($I_D$) graph

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**Pulse Width ($t_{sw}$)**

- $t_{sw}$ vs. $R_{th}$ graph
SMini6-F3-B

Unit: mm

Land Pattern (Reference) (Unit: mm)
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