**Panasonic**

**FC8V33030L**

Dual N-channel MOSFET

For switching
For DC-DC Converter

- **Features**
  - Low drain-source On-state Resistance:
    \[ R_{DS(on)} \text{typ} = 22 \, \text{m\Omega} \text{ (VGS = 4.5 V)} \]
  - High-speed switching:
    \[ Q_g = 3.8 \, \text{nC} \]
  - Halogen-free / RoHS compliant
    (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

- **Marking Symbol:** 6A

- **Basic Part Number:** Dual Nch MOS 33V (Individual)

- **Packaging**
  Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

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**Absolute Maximum Ratings** \( T_a = 25 \, ^\circ\text{C} \)  

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Voltage</td>
<td>VDS</td>
<td>33</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source Voltage</td>
<td>VGS</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current (Steady State) (^{1})</td>
<td>ID</td>
<td>6.5</td>
<td>A</td>
</tr>
<tr>
<td>Drain Current (t = 10 s) (^{1})</td>
<td></td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Drain Current (Pulsed) (^{1,2})</td>
<td>IDp</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>Source Current (Pulsed) (Body Diode) (^{1,2})</td>
<td>ISp(BD)</td>
<td>6.5</td>
<td></td>
</tr>
<tr>
<td>Total Power Dissipation (Steady State) (^{1})</td>
<td>PD</td>
<td>1</td>
<td>W</td>
</tr>
<tr>
<td>Total Power Dissipation (t = 10 s) (^{1})</td>
<td></td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>Channel Temperature</td>
<td>Tch</td>
<td>150</td>
<td>^\circ\text{C}</td>
</tr>
<tr>
<td>Operating Ambient Temperature</td>
<td>Topr</td>
<td>-40 to +85</td>
<td>^\circ\text{C}</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Tstg</td>
<td>-55 to +150</td>
<td>^\circ\text{C}</td>
</tr>
</tbody>
</table>

**Note:**
- \(^{1}\) Device mounted on a glass-epoxy board (See Figure 1)
- \(^{2}\) Pulse test: Ensure that the channel temperature does not exceed 150^\circ\text{C}.

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**Internal Connection**

**Pin Name**

1. Tr.1 Source  5. Tr.2 Drain
2. Tr.1 Gate    6. Tr.2 Drain
3. Tr.2 Source  7. Tr.1 Drain
4. Tr.2 Gate    8. Tr.1 Drain

**Figure 1:** FR4 Glass-Epoxy Board
25.4 mm x 25.4 mm x 0.8 mm
### Electrical Characteristics  
\( \text{Ta} = 25^\circ \text{C} \pm 3^\circ \text{C} \)  
Tr.1, Tr.2

#### Static Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Breakdown Voltage</td>
<td>VDSS</td>
<td>ID = 1 mA, VGS = 0 V</td>
<td>33</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>IDSS</td>
<td>VDS = 33 V, VGS = 0 V</td>
<td></td>
<td>10</td>
<td></td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>Gate-source Leakage Current</td>
<td>IGSS</td>
<td>VGS = ( \pm 16 ) V, VDS = 0 V</td>
<td></td>
<td>( \pm 10 )</td>
<td></td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>Gate-source Threshold Voltage</td>
<td>Vth</td>
<td>ID = 0.48 mA, VDS = 10 V</td>
<td>1</td>
<td></td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>Drain-source On-state Resistance (^{*1})</td>
<td>RDS(on)(^{1})</td>
<td>ID = 3.3 A, VGS = 10 V</td>
<td>15</td>
<td>20</td>
<td></td>
<td>( \text{m}\Omega )</td>
</tr>
<tr>
<td></td>
<td>RDS(on)(^{2})</td>
<td>ID = 3.3 A, VGS = 4.5 V</td>
<td>22</td>
<td>35</td>
<td></td>
<td>( \text{m}\Omega )</td>
</tr>
</tbody>
</table>

#### Dynamic Characteristics

| Input Capacitance                                     | Ciss   | VDS = 10 V, VGS = 0 V f = 1 MHz | 360   |       |       | pF   |
| Reverse Transfer Capacitance                         | Coss   | f = 1 MHz                       | 70    |       |       |      |
| Turn-on Delay Time \(^{*2}\)                         | td(on) | VDD = 15 V, VGS = 0 to 10 V     | 8     |       |       | ns   |
| Rise Time \(^{*2}\)                                  | tr     | ID = 3.3 A                      | 3     |       |       |      |
| Turn-off Delay Time \(^{*2}\)                        | td(off)| VDD = 15 V, VGS = 10 to 0 V     | 24    |       |       |      |
| Fall Time \(^{*2}\)                                  | tf     | ID = 3.3 A                      | 9     |       |       |      |
| Total Gate Charge                                     | Qg     | VDD = 15 V, VGS = 0 to 4.5 V, f | 3.8   |       |       | nC   |
|                                                       | Qgs    | = 1 MHz                        | 1.4   |       |       |      |
| Gate-drain Charge                                     | Qgd    | ID = 6.5 A                      | 1.6   |       |       |      |

#### Body Diode Characteristic

| Diode Forward Voltage \(^{*1}\)                         | VSD | IS = 3.3 A, VGS = 0 V | 0.8  | 1.2   |       | V    |

Note:
1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
2. \(^{*1}\) Pulse test: Ensure that the channel temperature does not exceed 150°C.
3. \(^{*2}\) Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time
*2 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

![Circuit Diagram]

- **VDD = 15 V**
- **ID = 3.3 A**
- **PW = 10μs**
- **D.C. ≤ 1%**

![Waveform Diagram]

- **Vin**
- **Vout**
- **td(on)**
- **tr**
- **td(off)**
- **tf**
Capacitance - VDS

Dynamic Input/Output Characteristics

ID - VDS

ID - VGS

VDS - VGS

RDS(on) - ID

Capacitance  C (pF)

VDD = 15 V

VDD = 15 V
MOS FET

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**Vth - Ta**

![Graph showing Gate-source Threshold Voltage (V) vs Temperature (°C)](image1)

**RDS(on) - Ta**

![Graph showing Drain-source On-state Resistance (mΩ) vs Temperature (°C)](image2)

**PD - Ta**

![Graph showing Total Power Dissipation (W) vs Temperature Ta (°C)](image3)

**Rth - tsww**

![Graph showing Thermal Resistance (°C/W) vs Pulse Width tsww (s)](image4)

**Safe Operating Area**

![Graph showing Operation in this area is limited by RDS(on)](image5)

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**Established**: 2011-04-20

**Revised**: 2013-07-31

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**Notes**:
- Operation in this area is limited by RDS(on).
- Ta = 25 °C. Glass epoxy board (25.4 × 25.4 × 0.8 mm) coated with copper foil which has more than 300 mm².
**MOS FET**

**FC8V33030L**

**WMini8-F1**

**Unit: mm**

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**Land Pattern (Reference) (Unit: mm)**

- 0.65
- 0.65
- 0.65
- 0.4
- 2.4

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Established: 2011-04-20
Revised: 2013-07-31
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