FC5516010R
Dual N-channel MOSFET

For switching

Features
- Low drive voltage: 2.5 V drive
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

Marking Symbol: V5

Basic Part Number
Dual FK350601 (Source Common type)

Packaging
FC5516010R Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

Absolute Maximum Ratings  Ta = 25 °C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Voltage</td>
<td>VDS</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source Voltage</td>
<td>VGS</td>
<td>±12</td>
<td>V</td>
</tr>
<tr>
<td>Drain current (DC)</td>
<td>ID</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>Drain current (Pulsed)</td>
<td>IDp</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Total power dissipation</td>
<td>PD</td>
<td>150</td>
<td>mW</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>Tch</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin name</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Gate(FET1)</td>
<td>4. Drain(FET2)</td>
</tr>
<tr>
<td>2. Source(FET1,2)</td>
<td>5. Drain(FET1)</td>
</tr>
<tr>
<td>3. Gate(FET2)</td>
<td></td>
</tr>
</tbody>
</table>

Panasonic
Packaging:
- SC-113CB

Code:
- SOT-353

Features
- Low drive voltage: 2.5 V drive
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

Publication date: October 2012 Ver. BED
## Electrical Characteristics  \( Ta = 25 \, ^\circ C \pm 3 \, ^\circ C \)

**FET1, FET2**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Breakdown Voltage</td>
<td>VDSS</td>
<td>ID = 1.0 mA, VGS = 0 V</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>IDSS</td>
<td>VDS = 60 V, VGS = 0 V</td>
<td></td>
<td>1.0</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source Leakage Current</td>
<td>IGSS</td>
<td>VGS = ±10 V, VDS = 0 V</td>
<td></td>
<td>±10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate-source Threshold Voltage</td>
<td>Vth</td>
<td>ID = 1.0 ( \mu A ), VDS = 3.0 V</td>
<td>0.9</td>
<td>1.2</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>Drain-source On-state Resistance</td>
<td>RDS((\text{on}))1</td>
<td>ID = 10 mA, VGS = 2.5 V</td>
<td>8</td>
<td>15</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td>RDS((\text{on}))2</td>
<td>ID = 10 mA, VGS = 4.0 V</td>
<td>6</td>
<td>12</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td>[Yfs]</td>
<td>ID = 10 mA, VDS = 3.0 V</td>
<td>20</td>
<td>60</td>
<td></td>
<td>mS</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Ciss</td>
<td>VDS = 3 V, VGS = 0 V, f = 1 MHz</td>
<td></td>
<td>12</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>Coss</td>
<td>VDS = 3 V, VGS = 0 V</td>
<td></td>
<td>7</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>Crss</td>
<td>VDS = 3 V, VGS = 0 V</td>
<td></td>
<td>3</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Turn-on time (^1)</td>
<td>ton</td>
<td>VDD = 3 V, VGS = 0 V to 3 V</td>
<td></td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID = 10 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-off time (^1)</td>
<td>toff</td>
<td>VDD = 3 V, VGS = 3 V to 0 V</td>
<td></td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID = 10 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\(^1\) See Test circuit
*1 Test circuit

Vin

VDD = 3 V

ID = 10 mA
RL = 300 Ω

Vout

PW = 10 μs
D.C. ≤ 1 %

D

S

50 Ω

10 %

90 %

VDD

0 V

3 V

Vin

10 %

90 %

Vout

ton

toff

ID = 10 mA

RL = 300 Ω

VIN = 50 Ω
Safe Operating Area

- **Gate-source Threshold Voltage** $V_{th}$ (V)
  - $V_{th} = 0.8 - 0.6$ V
  - $V_{th} = 0.5 - 0.3$ V
  - $V_{th} = 0.2 - 0.1$ V

- **Total Power Dissipation** $P_D$ (W)
  - $P_D = 1 - 2$ W
  - $P_D = 0.5 - 1$ W
  - $P_D = 0.1 - 0.5$ W

- **Drain Current** $I_D$ (A)
  - $I_D = 0.2 - 1$ A
  - $I_D = 0.1 - 0.2$ A
  - $I_D = 0.01 - 0.1$ A

- **Drain-source Voltage** $V_{DS}$ (V)
  - $V_{DS} = 2.5 - 10$ V
  - $V_{DS} = 1 - 2.5$ V
  - $V_{DS} = 0.1 - 1$ V

- **Operation in this area is limited by** $R_{DS(on)}$
  - $Ta = 25$ °C
  - Glass epoxy board (25.4 × 25.4 × 0.8 mm) coated with copper foil, which has more than 300 mm².

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**Diagram 1:** Gate-source Threshold Voltage $V_{th}$ vs. Temperature $Ta$ (°C)

**Diagram 2:** Drain-source On-state Resistance $R_{DS(on)}$ vs. Temperature $Ta$ (°C)

**Diagram 3:** Total Power Dissipation $P_D$ vs. Temperature $Ta$ (°C)

**Diagram 4:** Drain Current $I_D$ vs. Drain-source Voltage $V_{DS}$ (V)

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Ver. BED 5
SMini5-F3-B

Unit: mm

- Land Pattern (Reference) (Unit: mm)
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