

# DATA SHEET

Part No.	AN12949A
Package Code No.	HQFP048-P-0707

Maintenance/Discontinued

Maintenance/Discontinued includes following four Product lifecycle stage  
(planned maintenance type, maintenance type, planned discontinued type, discontinued type)

Contents

■ Overview ..... 3

■ Features ..... 3

■ Applications ..... 3

■ Package ..... 3

■ Type ..... 3

■ Application Circuit Example (Block Diagram) ..... 4

■ Pin Descriptions ..... 5

■ Absolute Maximum Ratings ..... 7

■ Operating Supply Voltage Range ..... 7

■ Electrical Characteristics ..... 8

■ Electrical Characteristics (Reference values for design) ..... 9

■ Control Pin Mode Table ..... 10

■ Technical Data ..... 11

■ Usage Notes ..... 27

Maintenance/Discontinued  
(planned maintenance type, maintenance type, planned discontinued type, discontinued type)

Maintenance/Discontinued includes following four Product lifecycle stage.

# AN12949A

## Audio Power IC for Note PC

### ■ Overview

AN12949A is the stereo BTL amplifier which contained the AGC circuit for clip prevention of a speaker output. This IC performs a mode change by parallel control system. (Standby function ON/OFF change etc.)

### ■ Features

- In order to realize high efficiency of output power, it adopts CMOS power amplifier circuit.
- Max. Power: 1.4 W ( $V_{CCSP} = 5\text{ V}$ ,  $R_L = 8\ \Omega$ , THD = 10%)  
2.2 W ( $V_{CCSP} = 5\text{ V}$ ,  $R_L = 4\ \Omega$ , THD = 10%)
- The resistance and the capacitor of a detector circuit which were being used for the conventional AGC.
- The filter circuit for the frequency response decision can be composed of the input circuit.
- STBY function (countermeasure pop noise)  
The standby terminal of the speaker amplifier is prepared by each of two terminals.  
When either of two terminals becomes " Low ", it is standby OFF.
- AGC ON/OFF function
- AGC ON level select function
- AGC attack time select function
- AGC recovery time select function
- Cellular phone measures  
RF noise prevention
- Built-in over current protection

### ■ Applications

- For the notebook personal computer

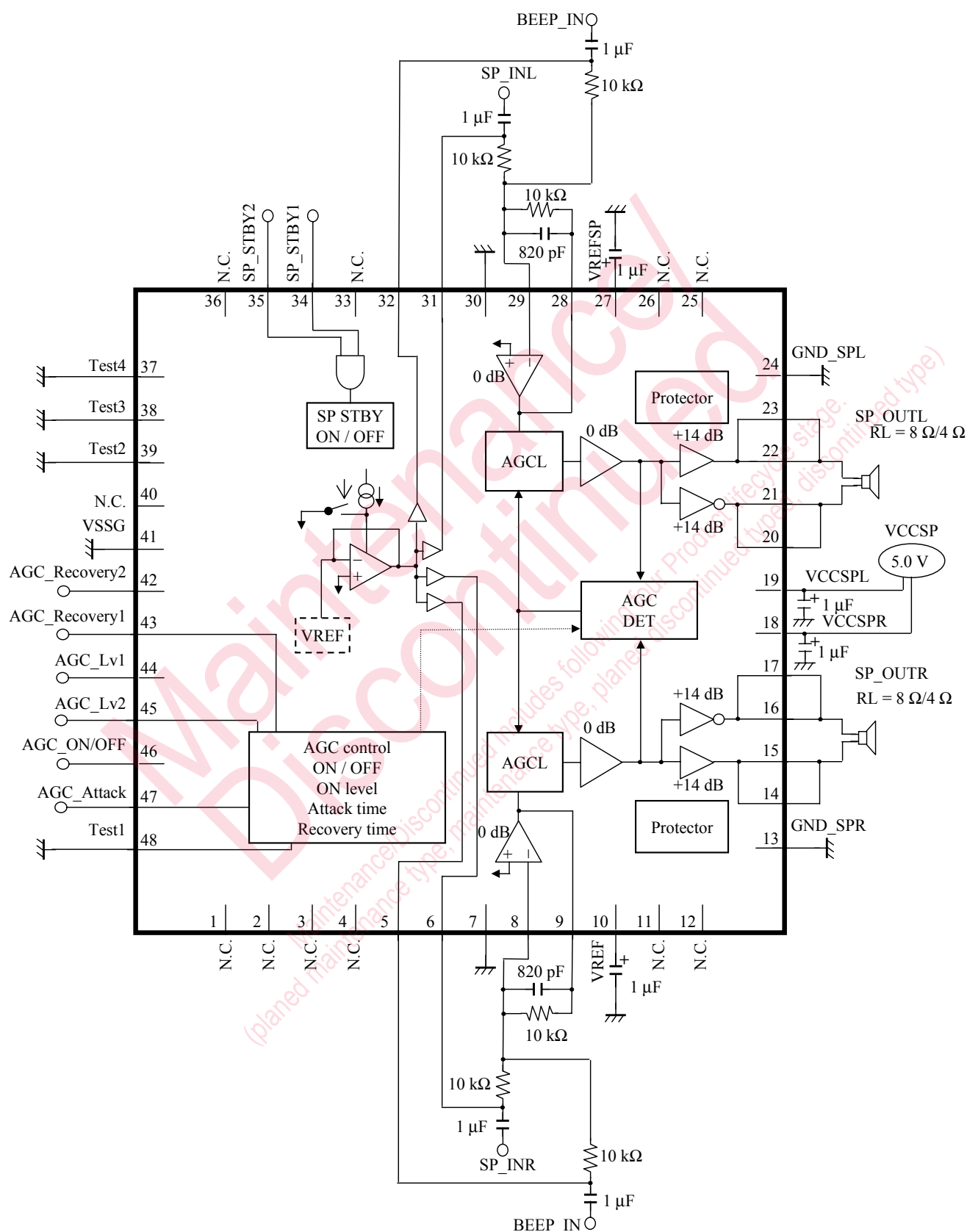
### ■ Package

- 48-pin plastic quad flat package with heat slug (QFP type)

### ■ Type

- Silicon monolithic BI-CMOS IC

## ■ Application Circuit Example (Block Diagram)



Note) This circuit and these circuit constants show an example and do not guarantee the design as a mass-production set.

## ■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	N.C.	—	—
2	N.C.	—	—
3	N.C.	—	—
4	N.C.	—	—
5	PC1	Output	Pre-charge 1
6	PC2	Output	Pre-charge 2
7	GND	Ground	Ground
8	SP_INR	Input	Right channel speaker signal input
9	PREOUT_R	Output	Right channel speaker signal Pre Amp output
10	VREF	Output	Reference voltage
11	N.C.	—	—
12	N.C.	—	—
13	GND_SPR	Ground	Ground
14	SPOUTR – VE	Output	Right channel speaker negative output
15	SPOUTR – VE	Output	Right channel speaker negative output
16	SPOUTR +VE	Output	Right channel speaker positive output
17	SPOUTR +VE	Output	Right channel speaker positive output
18	VCCSPR	Power Supply	Power supply for right speaker
19	VCCSPL	Power Supply	Power supply for left speaker
20	SPOUTL +VE	Output	Left channel speaker positive output
21	SPOUTL +VE	Output	Left channel speaker positive output
22	SPOUTL – VE	Output	Left channel speaker negative output
23	SPOUTL – VE	Output	Left channel speaker negative output
24	GND_SPL	Ground	Ground
25	N.C.	—	—
26	N.C.	—	—
27	VREFSP	Output	Speaker reference voltage
28	PREOUT_L	Output	Left channel speaker signal Pre Amp output
29	SP_INL	Input	Left channel speaker signal input
30	GND	Ground	Ground
31	PC3	Output	Pre-charge 3
32	PC4	Output	Pre-charge 4

## ■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
33	N.C.	—	—
34	SP_STBY1	Input	Speaker standby control 1
35	SP_STBY2	Input	Speaker standby control 2
36	N.C.	—	—
37	Test4	Input	Test 4
38	Test3	Input	Test 3
39	Test2	Input	Test 2
40	N.C.	—	—
41	VSSG	Ground	Ground
42	AGC_Recovery2	Input	AGC recovery time control 2
43	AGC_Recovery1	Input	AGC recovery time control 1
44	AGC_Lv1	Input	AGC level selection 1
45	AGC_Lv2	Input	AGC level selection 2
46	AGC_ON/OFF	Input	AGC on/off control
47	AGC_Attack	Input	AGC attack time control
48	Test1	Input	Test 1

### ■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage	VCCSPL VCCSPR	5.75	V	*1
2	Supply current	I <sub>CC</sub>	—	A	
3	Power dissipation	P <sub>D</sub>	307	mW	*2
4	Operating ambient temperature	T <sub>opr</sub>	−40 to +85	°C	*3
5	Storage temperature	T <sub>stg</sub>	−55 to +150	°C	*3

Note) \*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

\*2: The power dissipation shown is the value at T<sub>a</sub> = 85°C for the independent (unmounted) IC package with a heat sink.

When using this IC, refer to the • P<sub>D</sub> – T<sub>a</sub> diagram in the ■ Technical Data and use under the condition not exceeding the allowable value.

\*3: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T<sub>a</sub> = 25°C.

### ■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	VCCSPL VCCSPR	4.5 to 5.5	V	*

Note) \*: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

# ■ Electrical Characteristics at VCCSPL = VCCSPR = 5.0 V

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	No te
				Min	Typ	Max		
Circuit current								
1	Circuit current 1 at non-signal (VCCSP system)	IVCC	VCCSP = 5.0 V, Non-signal, SPSTBY = OFF, RL = 8 Ω	6	15	25	mA	*
2	Circuit current 1B at non-signal (VCCSP system)	IVCCB	VCCSP = 5.0 V, Non-signal, SPSTBY = ON, RL = 8 Ω	—	33	100	μA	*
Speaker amplifier characteristics								
3	SP reference output level	VSPOL VSPOR	Vin = −16.0 dBV, f = 1 kHz RL = 8 Ω	2.0	4.0	6.0	dBV	—
4	SP reference output distortion	THSPOL THSPOR	Vin = −16.0 dBV, f = 1 kHz RL = 8 Ω, to THD 5th	—	0.05	0.1	%	—
5	SP output noise voltage	VNSPOL VNSPOR	Non-Signal A-curve filter	—	−79	−73	dBV	—
6	SP maximum rating output 1	VMSP01L VMSP01R	THD = 10%, f = 1 kHz RL = 8 Ω, AGC = OFF	1.0	1.4	—	W	—
7	SP maximum rating output 2	VMSP02L VMSP02R	THD = 10%, f = 1 kHz RL = 4 Ω, AGC = OFF	1.8	2.3	—	W	—
8	SP channel balance	CHBS	Vin = −16.0 dBV, f = 1 kHz RL = 8 Ω	−1.0	0	1.0	dB	—
9	SP cross talk	VCTSPL VCTSPR	Vin = −16.0 dBV, f = 1 kHz RL = 8 Ω, A-curve filter	70	80	—	dB	—
10	SP output level at standby	VSSPOL VSSPOR	Vin = −16.0 dBV, f = 1 kHz RL = 8 Ω, A-curve filter	—	−100	−86	dBV	—
11	SP output DC offset voltage	VDCSPL VDCSPR	Non-signal	—	±0	±35	mV	—
12	SP AGC output level 1	VSPOA1L VSPOA1R	Vin = −6.0 dBV, f = 1 kHz RL = 8 Ω, AGC = 9 dBV	8.0	9.0	10.0	dBV	—
13	SP AGC output level 2	VSPOA2L VSPOA2R	Vin = −6.0 dBV, f = 1 kHz RL = 8 Ω, AGC = 6 dBV	5.0	6.0	7.0	dBV	—
14	SP AGC output level 3	VSPOA3L VSPOA3R	Vin = −6.0 dBV, f = 1 kHz RL = 4 Ω, AGC = 8.1 dBV	7.0	8.1	9.2	dBV	—
15	SP AGC output level 4	VSPOA4L VSPOA4R	Vin = −6.0 dBV, f = 1 kHz RL = 4 Ω, AGC = 6 dBV	5.0	6.0	7.0	dBV	—

Note) \*: VCCSP = VCCSPL and VCCSPR



# ■ Electrical Characteristics (Reference values for design) at VCCSPL = VCCSPR = 5.0 V

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
Other part								
16	SP power supply rejection ratio	SPSRRL1 SPSRRL1	f = 1 kHz, Vripple = 0.1 V[rms] DIN audio ON	—	60	—	dB	*
17	SP power supply rejection ratio	SPSRRL2 SPSRRL2	f = 10 kHz, Vripple = 0.1 V[rms] DIN audio ON	—	58	—	dB	*
Switch switching-over voltage level								
18	SPSTBY Low	SPSTL	—	0.0	—	0.8	V	—
19	SPSTBY High	SPSTH	—	2.5	—	5.5	V	—
20	AGC Lv Low	AGLVL	—	0.0	—	0.3	V	—
21	AGC Lv High	AGLVH	—	VCCSP − 0.3	—	5.5	V	—
22	AGC attack Low	AGATL	—	0.0	—	0.3	V	—
23	AGC attack High	AGATH	—	VCCSP − 0.3	—	5.5	V	—
24	AGC recovery Low	AGREL	—	0.0	—	0.3	V	—
25	AGC recovery High	AGREH	—	VCCSP − 0.3	—	5.5	V	—

Note) \*:  $V_{in} = VCCSPL$  and  $VCCSPR$  at DC 5 V

## ■ Control Pin Mode Table

### 1. AGC control

#### (a) AGC attack time selection

Pin voltage	Attack time
Pin 47	
Low	1 ms
High	2 ms

#### (b) AGC recovery time selection

Pin voltage		Recovery time
Pin 42	Pin 43	
Low	Low	1.0 s
Low	High	2.0 s
High	Low	4.0 s
High	High	8.0 s

#### (c) AGC ON level selection

Pin voltage		AGC ON level	Output Po (RL = 8 Ω)	Output Po (RL = 4 Ω)
Pin 44	Pin 45			
Low	Low	9.0 dBV	1.0 W	1.9 W
Low	High	8.1 dBV	0.8 W	1.5 W
High	Low	6.8 dBV	0.6 W	1.2 W
High	High	6.0 dBV	0.5 W	1.0 W

#### (d) AGC ON/OFF selection

Pin voltage	AGC ON/OFF
Pin 46	
Low	ON
High	OFF

### 2. SPSTBY-ON/OFF control

Pin voltage		SP_STBY ON / OFF
Pin 34 (SPSTBY1)	Pin 35 (SPSTBY2)	
Low	Low	OFF
Low	High	OFF
High	Low	OFF
High	High	ON

## ■ Technical Data

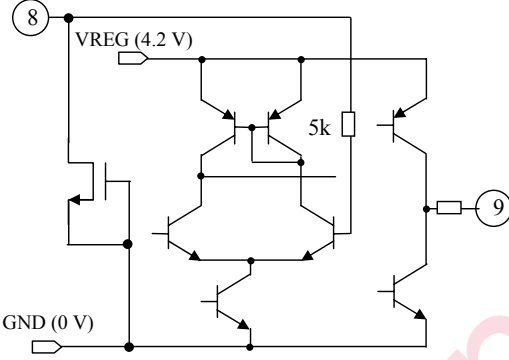

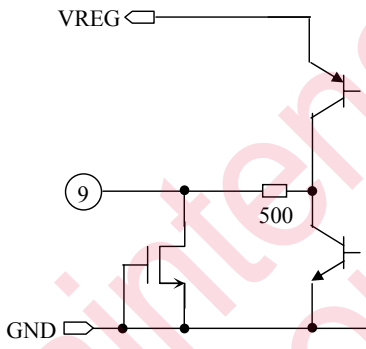
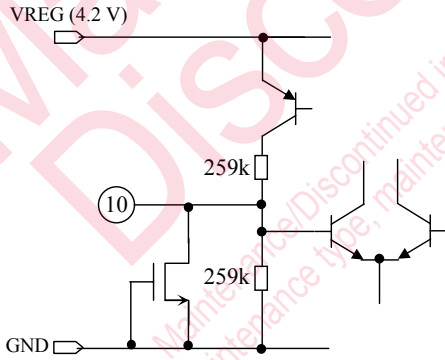
- I/O block circuit diagrams and pin function descriptions

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
1	N.C.	—	—	N.C. You can use it as other pattern.
2	N.C.	—	—	N.C. You can use it as other pattern.
3	N.C.	—	—	N.C. You can use it as other pattern.
4	N.C.	—	—	N.C. You can use it as other pattern.
5	PC1		Output impedance = Equal to or less than 1 k $\Omega$	Pre-charge 1. The pre-charge circuit will be ON for 50 ms and below and OFF. Once OFF, output will be Hi-Z.
6	PC2		Output impedance = Equal to or less than 1 k $\Omega$	Pre-charge 2. The pre-charge circuit will be ON for 50 ms and below and OFF. Once OFF, output will be Hi-Z.
7	GND DC 0 V	—	—	Signal terminal GND. The terminal GND of Pin7, Pin30, and Pin41 is connected in IC.

■ Technical Data (continued)


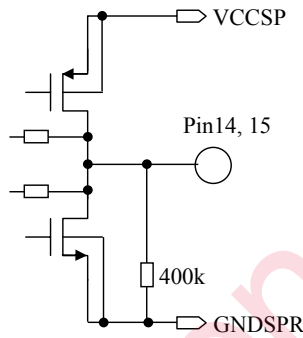

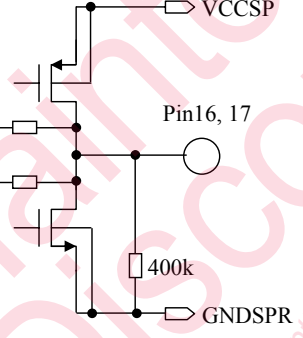
- I/O block circuit diagrams and pin function descriptions (continued)
- Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
8	SP_INR DC 2 V		Input impedance = Hi-Z	Feedback terminal of Rch input amplifier of speaker amplifier system.  The gain of the Rch input amplifier can be set by connecting external resistance with Pin8 and Pin9.
9	PREOUT_R  DC 2 V AC -16 dBV		Output impedance = Equal to or less than 10 Ω	Output terminal of Rch input amplifier of speaker amplifier system.  Please connect external resistance for the gain setting.
10	VREF		Input impedance = About 130 kΩ	The reference voltage terminal for determining DC bias of the output stage of a speaker amplifier system.  Please connect an external capacitor to remove a ripple.
11	N.C.	—	—	N.C. You can use it as other pattern.
12	N.C.	—	—	N.C. You can use it as other pattern.

# ■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)


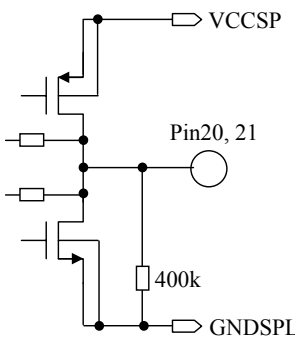

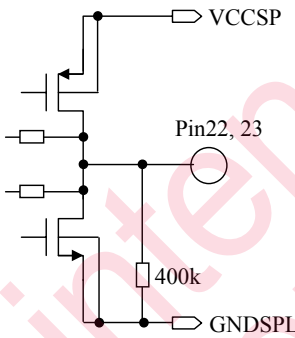
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
13	GND_SPR DC 0 V	—	—	Because a large current flows, it is preferable to separate the GND line to terminal GND (Pin13, Pin24) for the speaker amplifier and other terminals GND as much as possible on P board pattern.
14, 15	SP_OUTR-  DC 2.5 V AC -2 dBV		Output impedance = Equal to or less than 1 $\Omega$	Output terminal of Rch speaker amplifier. It is BTL output.  Rch positive aspect output pin: Pin16, Pin17  Rch reverse-aspect output pin: Pin14, Pin15
16, 17	SP_OUTR+  DC 2.5 V AC -2 dBV		Output impedance = Equal to or less than 1 $\Omega$	To decrease the voltage loss by the wire resistance when maximum outputting it, the output is made two terminals. Please connect Pin14 to Pin15 and Pin16 to Pin17 respectively on P board pattern.
18	VCCSPR DC 5 V	—	—	Terminal VCC to supply voltage to speaker amplifier of Rch.
19	VCCSPL DC 5 V	—	—	Terminal VCC to supply voltage to speaker amplifier of Lch.

# ■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
20, 21	SP_OUTL+  DC 2.5 V AC -2 dBV		Output impedance = Equal to or less than 1 $\Omega$	Output terminal of Lch speaker amplifier. It is BTL output.  Lch positive aspect output pin: Pin20, Pin21  Lch reverse-aspect output pin: Pin22, Pin23
22, 23	SP_OUTL-  DC 2.5 V AC -2 dBV		Output impedance = Equal to or less than 1 $\Omega$	To decrease the voltage loss by the wire resistance when maximum outputting it the output is made two terminals. Please connect Pin 20 to Pin 21 and Pin 22 to Pin 23 respectively on P board pattern.
24	GND_SPL DC 0 V	—	—	Because a large current flows, it is preferable to separate the GND line to terminal GND (Pin13, Pin24) for the speaker amplifier and other terminals GND as much as possible on P board pattern.
25	N.C.	—	—	N.C. You can use it as other pattern.
26	N.C.	—	—	N.C. You can use it as other pattern.

# ■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
27	VREFSP DC 2.5 V		Input impedance = About 125 k $\Omega$	<p>The reference voltage terminal for determining DC bias of the output stage of a speaker amplifier system.</p> <p>Please connect an external capacitor to remove a ripple.</p>
28	PREOUT_L  DC 2 V AC -16 dBV		Output impedance = Equal to or less than 10 $\Omega$	<p>Output terminal of Lch input amplifier of speaker amplifier system.</p> <p>Please connect external resistance for the gain setting.</p>
29	SP_INL DC 2 V		Input impedance = Hi-Z	<p>Feedback terminal of Lch input amplifier of speaker amplifier system.</p> <p>The gain of the Lch input amplifier can be set by connecting external resistance with Pin28 and Pin29.</p>
30	GND	—	—	<p>Signal terminal GND.</p> <p>The terminal GND of Pin7, Pin30, and Pin41 is connected in IC.</p>
31	PC3		Output impedance = Equal to or less than 1 k $\Omega$	<p>Pre-charge 3.</p> <p>The pre-charge circuit will be ON for 50 ms and below and OFF.</p> <p>Once OFF, output will be Hi-Z.</p>

# ■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
32	PC4		Output impedance = Equal to or less than 1 k $\Omega$	Pre-charge 4. The pre-charge circuit will be ON for 50 ms and below and OFF. Once OFF, output will be Hi-Z.
33	N.C.	—	—	N.C. You can use it as other pattern.
34	SP_STBY1		Input impedance = About 80 k $\Omega$	It is a control terminal that switches whether to put the speaker amplifier system into the state of operation or to put it into the state of the standby.  Pin34 or Pin35 operates and the speaker amplifier system operates at Low.
35	SP_STBY2		Input impedance = About 80 k $\Omega$	When Pin34 and Pin35 all are High, it completely enters the state of the standby, and most circuit currents are 0 in this IC.  Please refer to the ■ Control Pin Mode Table for the mode setting.
36	N.C.	—	—	N.C. You can use it as other pattern.
37	Test4		—	Terminal for testing. Please connect to Ground.
38	Test3		—	Terminal for testing. Please connect to Ground.



# ■ Technical Data (continued)

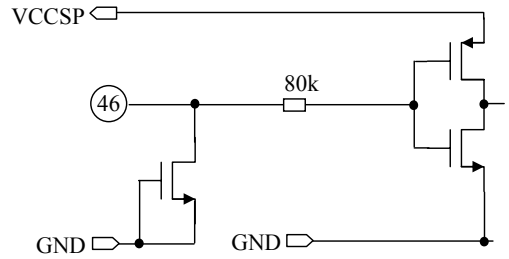
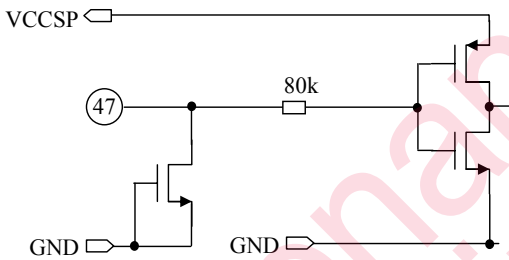
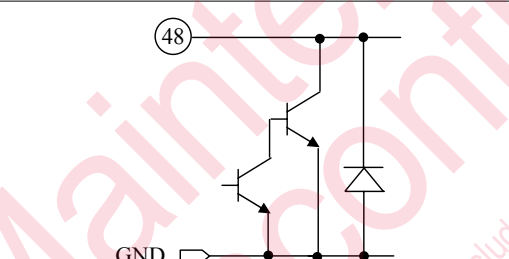
- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
39	Test2		—	Terminal for testing. Please connect to Ground.
40	N.C.	—	—	N.C. You can use it as other pattern.
41	VSSG	—	—	GND
42	AGC_Recovery2		Input impedance = Hi-Z	It is a control terminal that switches the recovery time of AGC.  The recovery time of four values can be selected by the High/Low setting of Pin42 and Pin43.
43	AGC_Recovery1		Input impedance = Hi-Z	Please refer to the ■ Control Pin Mode Table for the mode setting.
44	AGC_Lv1		Input impedance = Hi-Z	It is a control terminal that switches the turning on level at the AGC-ON.  The turning on level of four values can be selected by the High/Low setting of Pin44 and Pin45.
45	AGC_Lv2		Input impedance = Hi-Z	Please refer to the ■ Control Pin Mode Table for the mode setting.

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)
- Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

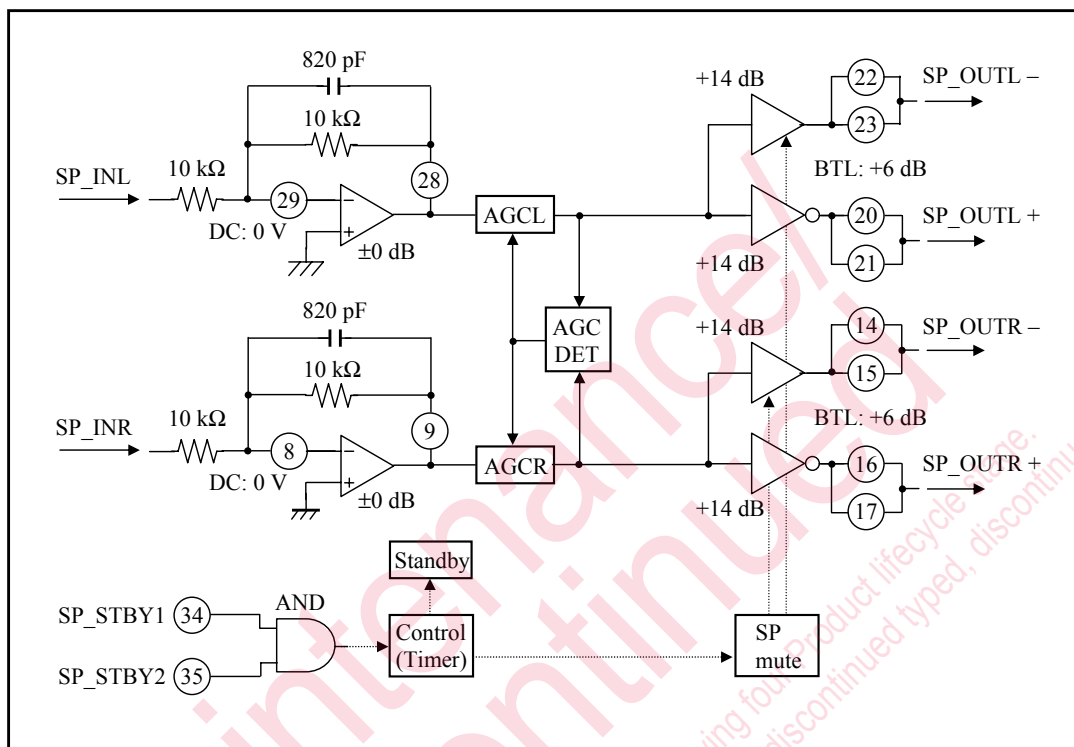
Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
46	AGC_ON/OFF		Input impedance = Hi-Z	It is a control terminal that switches the AGC function for the clip prevention of the speaker output in ON/OFF.  High: AGC-OFF Low: AGC-ON
47	AGC_Attack		Input impedance = Hi-Z	It is a control terminal that switches the attack time of AGC.  Binary attack time can be selected by the High/Low setting of Pin47.  High: 2 ms Low: 1 ms
48	Test1			Terminal for testing. Please connect to Ground.

## ■ Technical Data (continued)

- The explanation of the function for mainly

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

### 1. Speaker amplifier

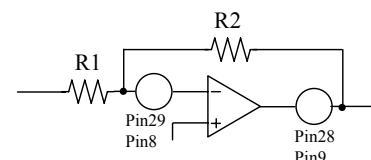


- 1) Gain of amplifier and input impedance can be set up by the external resistance.  
Total gain of the speaker amplifier is +20 dB when gain of the input amplifier is set up in  $\pm 0$  dB.

External resistance is made R1, R2.

$$\text{Gain} = 20\log(R2/R1)$$

$$Z_{in} = R1$$



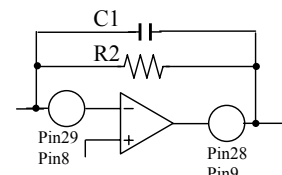
They are gain =  $\pm 0$  dB, input impedance = 10 k $\Omega$  in the case of R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$ .  
Use R1 and R2 in more than 10 k $\Omega$ .

- 2) LPF to remove the high frequency element for that to be unnecessary by giving the capacity of C1 can compose it.

External resistor is made R2. Capacity is made C1. Cutoff frequency is  $f_c$ .

$$f_c = 1/(2\pi \times R2 \times C1)$$

$f_c$  is about 19.4 kHz in the case of R2 = 10 k $\Omega$ , C1 = 820 pF.



## ■ Technical Data (continued)

- The explanation of the function for mainly (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

### 1. Speaker amplifier (continued)

- 3) As for the standby control by Pin34 and Pin35, an inside circuit is an AND form.  
A speaker amplifier starts when either of Pin34 or Pin35 is made Low. (Refer to the ■ Control Pin Mode Table.)
- 4) Off of speaker mute is delayed with the timer circuit from a standby release.  
This is for power supply on pop sound countermeasure.  
(Refer to the • The power supply and logic sequence in the ■ Technical Data and use.)
- 5) An input amplifier is the composition that it moves based on 0 V.  
A inside circuit can be started quickly after a standby release by this composition.  
Before it is outputted, I have 0 V shifted from the standard to 2.5 V as for the speaker amplifier output.

- Design reference value of speaker amplifier

Parameter	Design reference value	Note
Input / output gain	+20.0 dB	A setup by external resistance is possible for the gain of input amplifier.
Input impedance	10 k $\Omega$	A setup by external resistance is possible.
Output impedance	Equal to or less than 1 $\Omega$	But, it limits into the sound band range of equal to or less than 50 kHz.
Maximum input level	0 dBV	The maximum output level of input amplifier. The time of the warp ( to 5th of THD ) of 1% of output.
Maximum output level	1.4 W: RL = 8 $\Omega$ 2.2 W: RL = 4 $\Omega$	The time of the warp ( to 5th of THD ) of 10% of output.
Ability of the output drive	Equal to or more than 4 $\Omega$ of loads	—

- Protection circuit for speaker amplifier

- 1) Thermal protection circuit  
The thermal protection circuit operates at a Tj of approximately 150°C.  
The thermal protection circuit is reset automatically when the temperature drops.
- 2) Output pin short protection circuit
  - Output pin-power supply line short protection
  - Output-to-output pin short protection
  - Output pin-GND line short protection
 If short-circuit is no longer detected, it will return automatically.

Note) Operation is not guaranteed although the protection circuit is built in. Moreover, hundred percent inspection is not guaranteed.

## ■ Technical Data (continued)

- The explanation of the function for mainly (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

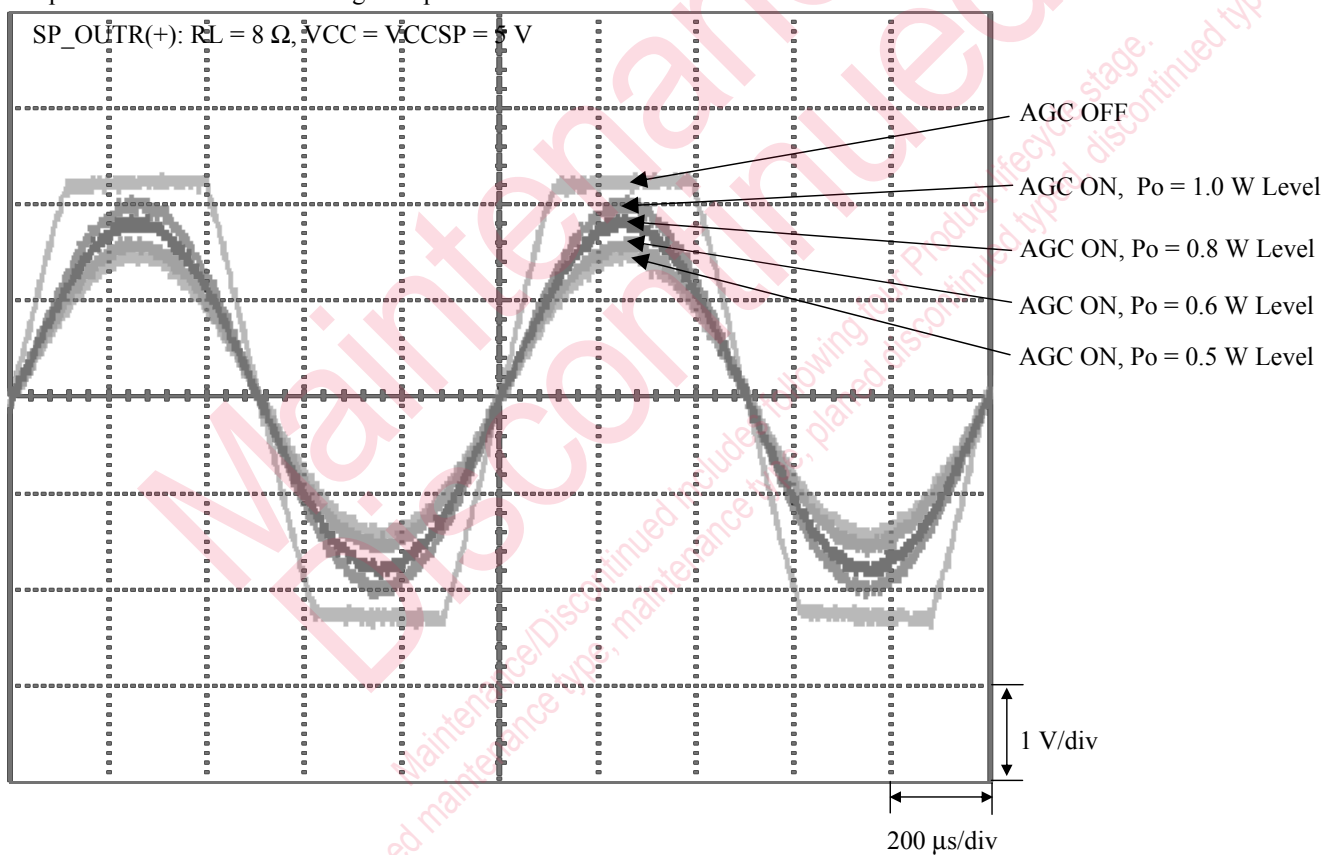
### 2. Operation of AGC

- The AGC circuitry can activate to minimize distortion, raising the average volume level and it can prevent speaker from breaking when an input level is too high.
- A speaker can protect it even if doesn't change the establishment of the input signal level by setting up an AGC on level in accordance with the allowable input value of the speaker.

#### 1) AGC ON level

AGC On level can be chosen from  $P_o = 1.2\text{ W}$ ,  $1.0\text{ W}$ ,  $0.8\text{ W}$ ,  $0.5\text{ W}$  ( $R_L = 8\ \Omega$ ).

Output waveform at sine wave signal input



Note) Four evaluation boards were used, and the same signal was inputted at the same time, and output wave shape was taken.

■ Technical Data (continued)

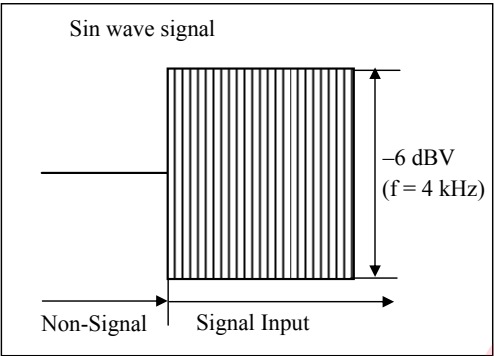
- The explanation of the function for mainly (continued)  
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

2. AGC attack time (continued)

2) AGC attack time

"AGC Attack Time" can set up for 1 ms and for 2 ms.

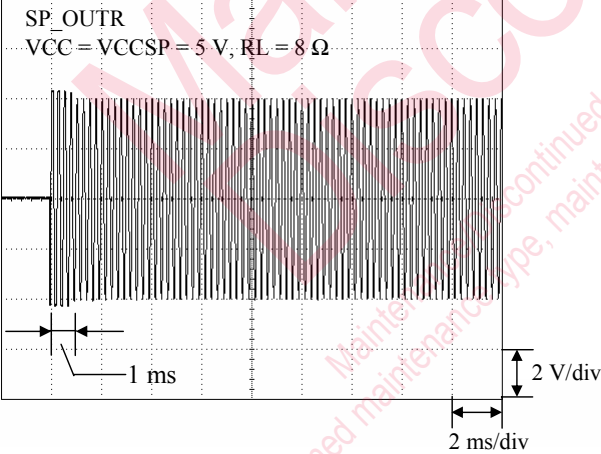
- Input waveform for AGC attack time observation



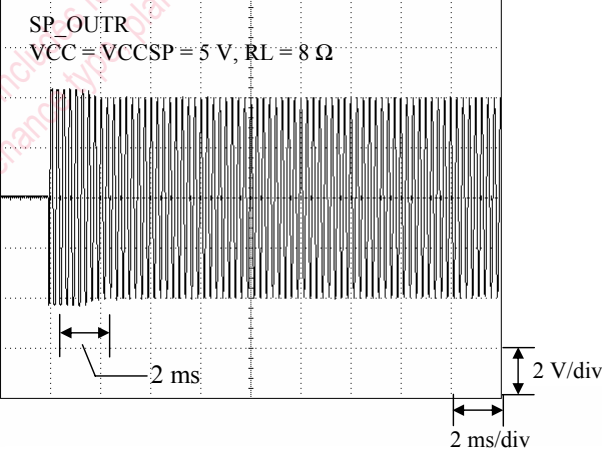
Set up the establishment of "Attack time" in the point which a sense of incongruity is scarce in. Confirm it by using the speaker mounted on the set at the signal such as music.

- Output waveform at AGC attack time (BTL output waveform)

- Attack time: 1 ms  
( AGC\_Attack: Pin 47 = Low )



- Attack time: 2 ms  
( AGC\_Attack: Pin47 = High )



■ Technical Data (continued)

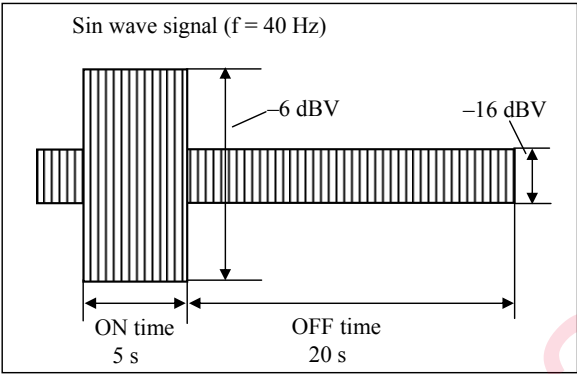
- The explanation of the function for mainly (continued)  
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

2. AGC attack time (continued)

3) AGC recovery time

"AGC Recovery Time" can be set up from 1 s, 2 s, 4 s, 8 s.

- Input waveform for AGC recovery time observation

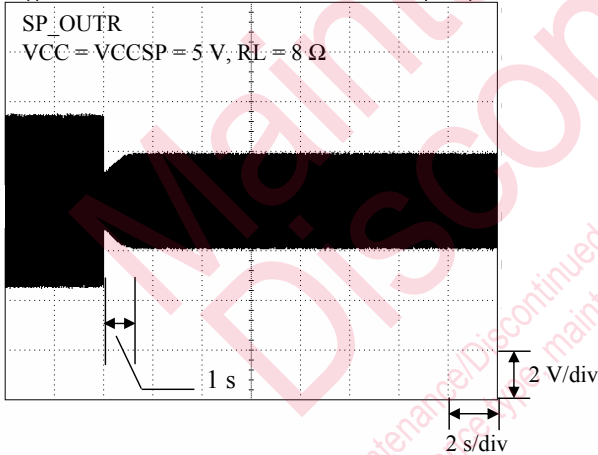


It is the test wave shape which the signal input that a thing in such cases as the music signal continued was presumed. Output amplitude is enlarged gradually at the time when it is decided by a setup of AGC recovery time.

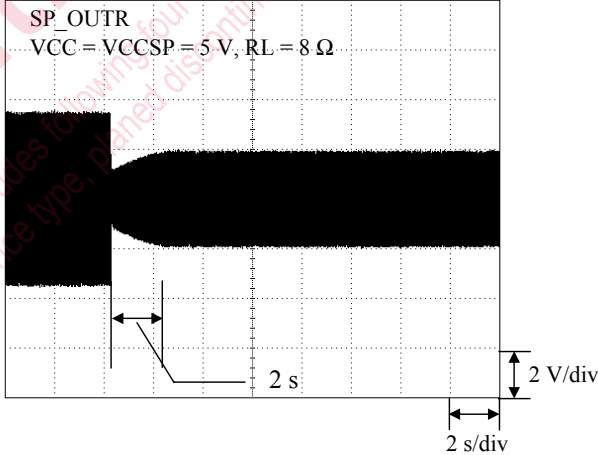
Set up the establishment of "Attack time" in the point which a sense of incongruity is scarce in. Confirm it by using the speaker mounted on the set at the signal such as music.

- Output waveform at AGC recovery time (BTL output waveform)

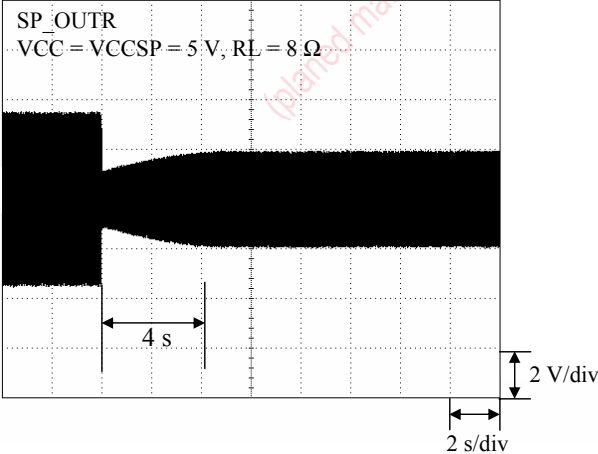
- Recovery time: 1.0 s  
( AGC\_Recovery 1, 2: Pin 43, 42 = Low, Low )



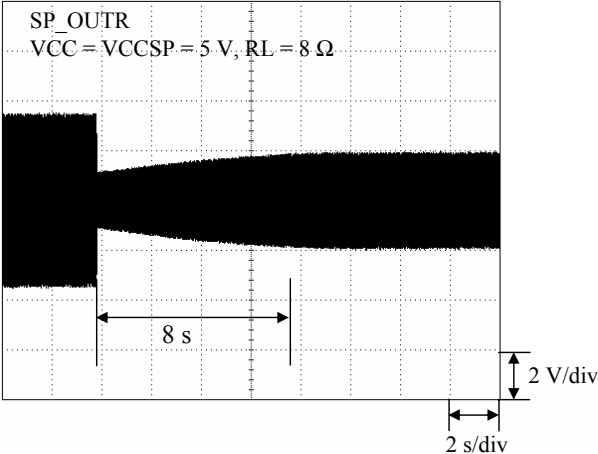
- Recovery time: 2.0 s  
( AGC\_Recovery 1, 2: Pin 43, 42 = Low, High )



- Recovery time: 4.0 s  
( AGC\_Recovery 1, 2: Pin 43, 42 = High, Low )



- Recovery time: 8.0 s  
( AGC\_Recovery 1, 2: Pin 43, 42 = High, High )



■ Technical Data (continued)

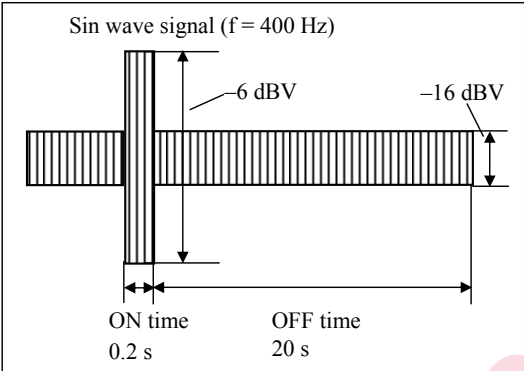
- The explanation of the function for mainly (continued)  
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

2. AGC attack time (continued)

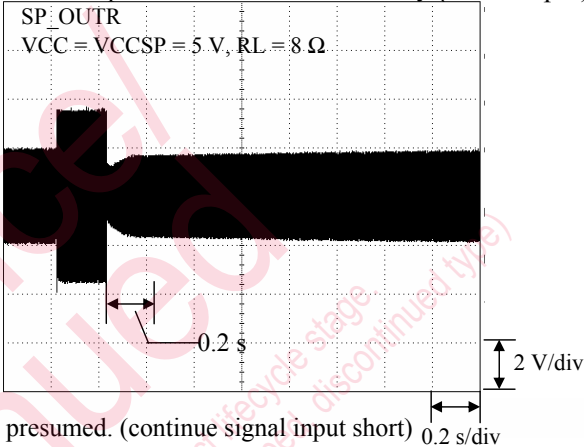
4) AGC short time Recovery

It is 0.2 s when the signal input time of the level that AGC moves is short.

Test wave shape of AGC short time recovery.

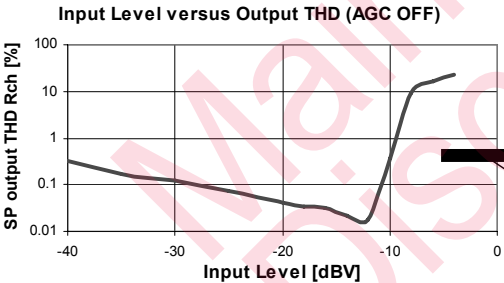


It is the output wave shape of AGC short time recovery (BTL output)



It is the test wave shape which a person's conversation and so on was presumed. (continue signal input short) Establishment time is being decided inside the IC, and it can't be changed.

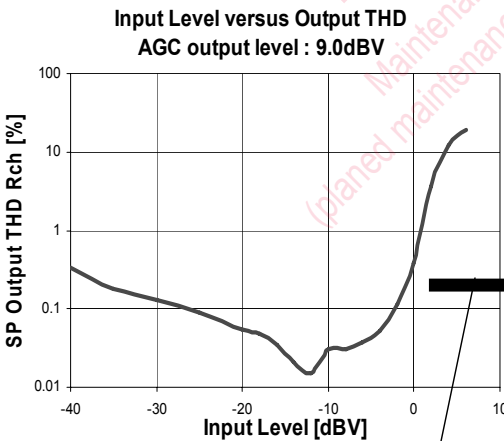
5) Output THD at AGC ON



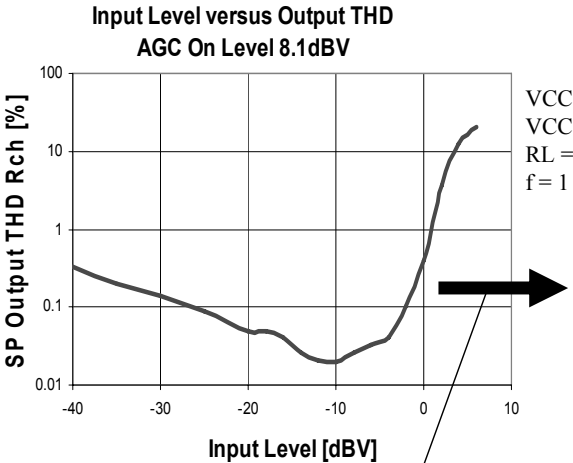
VCCSP = 5 V  
RL = 8 Ω  
f = 1 kHz

It can get the output which distortion is scarce in because there is "AGC" even if an input level is too big.

Output does a clip if it is not the input level which made the one for Amp. gain low from the output level of the amplifier.



VCCSP = 5 V  
RL = 8 Ω  
f = 1 kHz



VCC = 3.3 V  
VCCSP = 5 V  
RL = 8 Ω  
f = 1 kHz

It can get the output which distortion is scarce in because there is "AGC" even if an input level is too big.



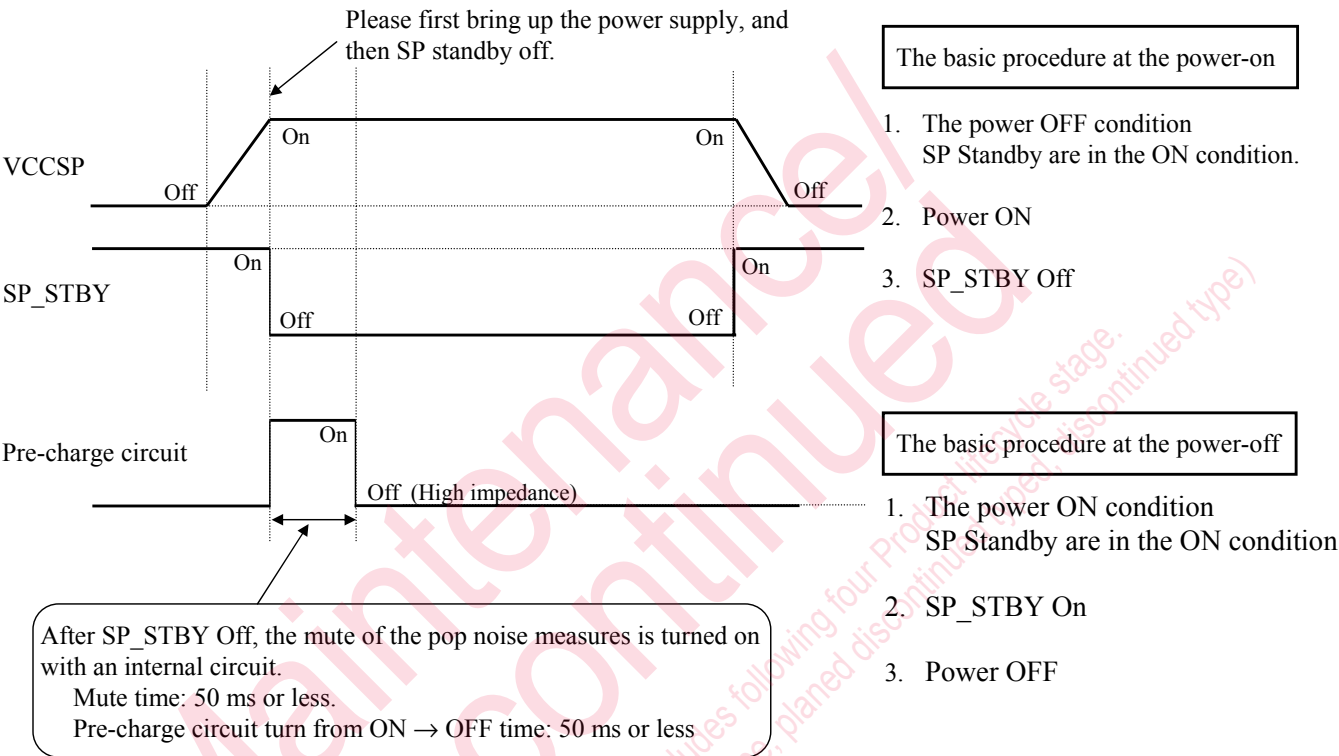
■ Technical Data (continued)

- The power supply and logic sequence

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

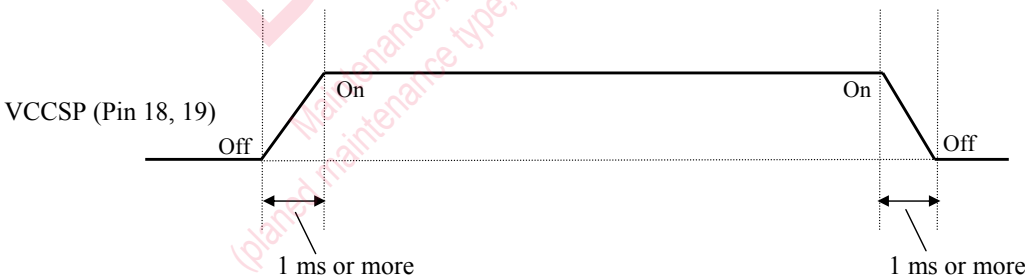
- The timing control of power-ON/OFF and each logic according to the procedure below should be recommended for the best pop performance caused in switching.

1) The sequence of the power supply and each logic



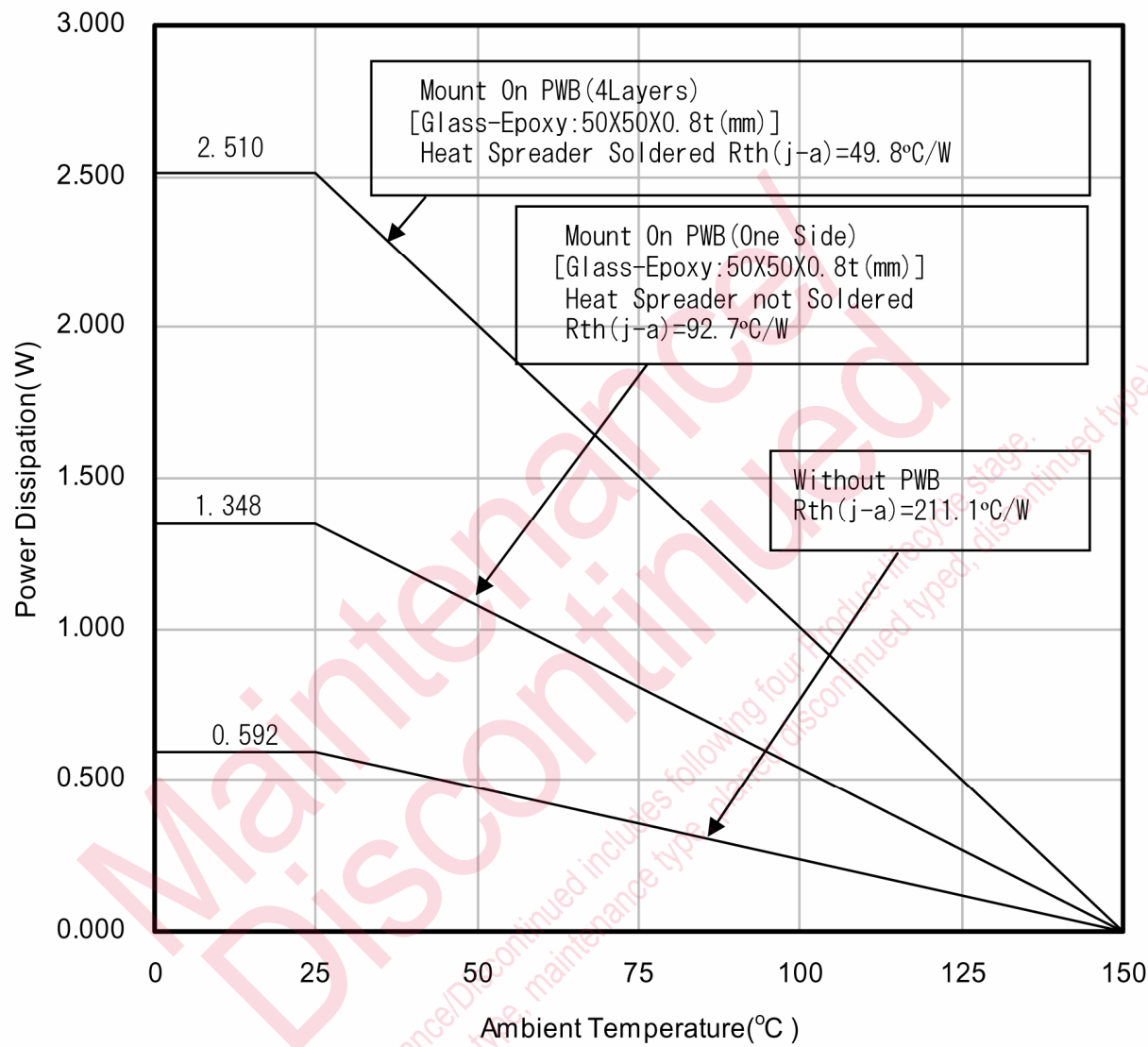
2) The sequence of VCCSP

A standup and falling time of VCCSP recommend 1 ms more.



■ Technical Data (continued)

•  $P_D - T_a$  diagram



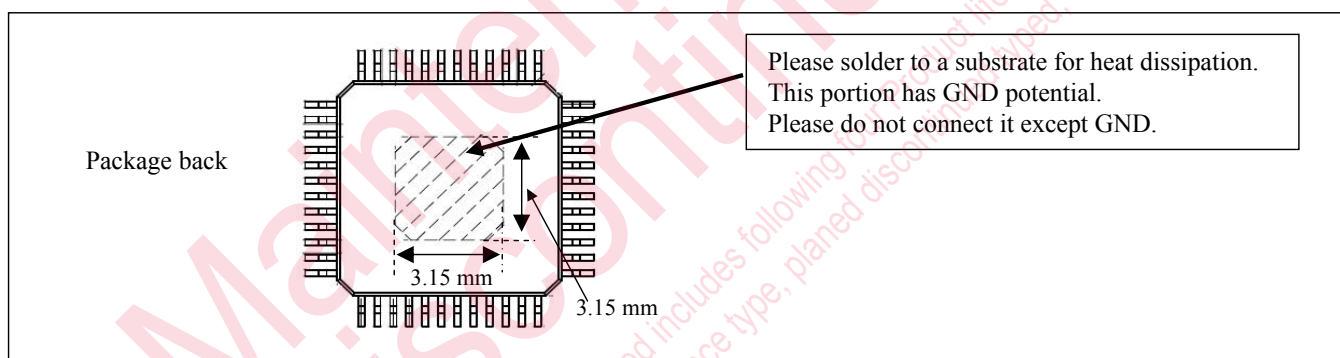
## ■ Usage Notes

1. Please carry out the thermal design with sufficient margin such that the power dissipation will not be exceeded, based on the conditions of power supply, load and surrounding temperature.

Although indicated also in the column of the maximum rating, the maximum rating becomes an instant and the marginal value which must not exceed. It sufficiently evaluates, and I use-wish-do so that it may not exceed certainly.

Moreover, don't impress neither voltage nor current to Pin which is not indicated. It may destroy in both cases.

2. Please pay attention in the pattern layout in order to prevent damage due to short circuit between pins.  
In addition, for the pin configuration, please refer to the ■ Pin Descriptions.
3. Please absolutely do not mount the LSI in the reverse direction on to the printed-circuit-board.  
It might be damaged when the electricity is turned on.
4. Please do a visual inspection on the printed-circuit-board before turning on the power supply, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device.  
Also perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. When using the LSI for model deployment or new products, perform fully the safety verification including the long-turn reliability for each product.
6. Note of soldering for heat dissipation



**Request for your special attention and precautions in using the technical information and semiconductors described in this book**

- (1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.
- (2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products, and no license is granted under any intellectual property right or other right owned by our company or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.
- (3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).  
Consult our sales staff in advance for information on the following applications:
  - Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
  - Any applications other than the standard applications intended.
- (4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.
- (5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
  - Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
- (6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
- (7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of Matsushita Electric Industrial Co., Ltd.